December 19, 2005 - Final Exam

Name: SOLUTIONS

Recitation: _____

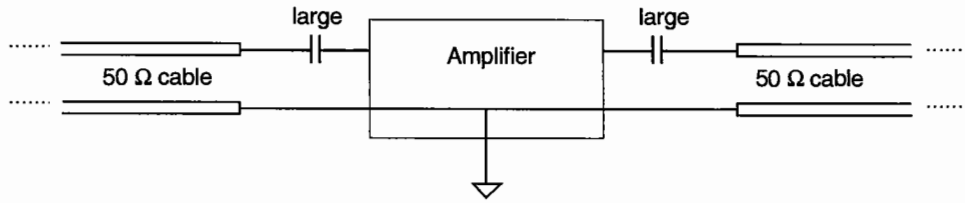
problem	grade
1	
2	
3	
4	
total	

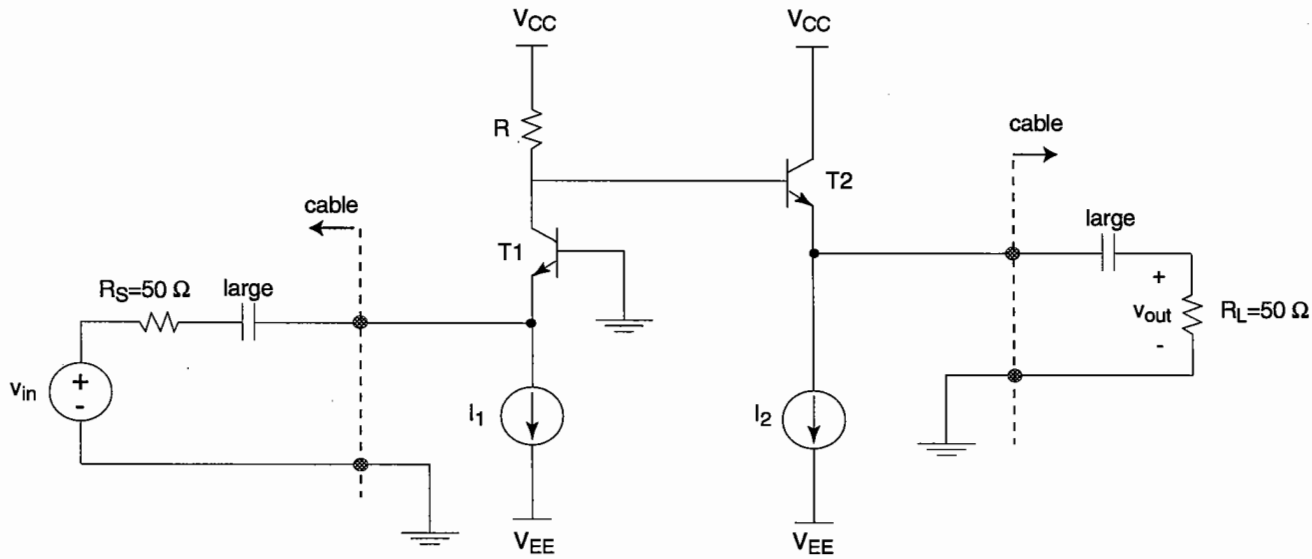
General guidelines (please read carefully before starting):

- Make sure to write your name on the space designated above.
- **Open book**: you can use any material you wish.
- All answers should be given in the space provided. Please do not turn in any extra material. If you need more space, use the back of the page.
- You have **three hours** to complete your exam.
- Make reasonable approximations and *state them*, i.e. quasi-neutrality, depletion approximation, etc.
- Partial credit will be given for setting up problems without calculations. **NO** credit will be given for answers without reasons.
- Use the symbols utilized in class for the various physical parameters, i.e. μ_n, I_D, E, etc.
- Every numerical answer must have the proper units next to it. Points will be subtracted for answers without units or with wrong units.
- Use $\phi = 0$ at $n_o = p_o = n_i$ as potential reference.
- Use the following fundamental constants and physical parameters for silicon and silicon dioxide at room temperature:

$$n_i = 1 \times 10^{10}\ cm^{-3}$$
$$kT/q = 0.025\ V$$
$$q = 1.60 \times 10^{-19}\ C$$
$$\epsilon_s = 1.05 \times 10^{-12}\ F/cm$$
$$\epsilon_{ox} = 3.45 \times 10^{-13}\ F/cm$$

1. *(28 points)* This problem studies an amplifier designed to boost a high-frequency signal midway along a 50-Ω cable. A block diagram of the cable and amplifier is shown below, together with the corresponding circuit.





In studying the amplifier, make use of the following information:

- To avoid undesired reflections within the input and output cables, the amplifier must be designed to have a 50 Ω input resistance and a 50 Ω output resistance. (To learn why, take 6.013!)
- The coupling capacitors in the block diagram and circuit isolate the biasing inside the amplifier from the cables. Assume the capacitors are large enough to be short circuits for the purposes of all small-signal modeling.
- Assume that both transistors in the amplifier exhibit the same forward current gain β, the same base-emitter capacitance C_π, and the same base-collector capacitance C_μ. When numerical values are needed, let $\beta_F = 200$, $C_\pi = 1$ pF, and $C_\mu = 0.1$ pF. Also, let the thermal voltage V_{th} be 25 mV. For both transistors, ignore their small-signal collector-emitter output resistance until Part 1i).
- Assume that the two bias current sources in the amplifier, I_1 and I_2, are ideal (*i.e.* their associated internal resistance is infinity).

1a) *(4 points)* The amplifier comprises two stages. For each of the following objectives, explain in a few sentences why the amplifier might be well-suited to meeting the objective.

☐ 50-Ω Input Resistance:

This is a very low value of R_{in}. The CB stage is required to make this possible.

☐ 50-Ω Output Resistance:

This is also a very low value of R_{out}. The common-collector stage is good at doing this.

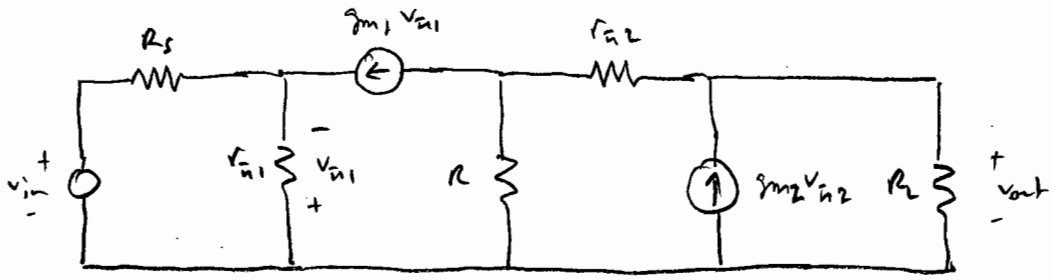
☐ High Voltage Gain:

Comes because the output resistance of the common base stage and the input resistance of the common drain stage are high. Then, there is a lot of voltage gain across T1 that T2 preserves.

☐ High Bandwidth:

High because there is no capacitor in the Miller position in T1 which is the transistor that gives high voltage gain.

1b) *(10 points)* Draw a small-signal circuit model of the entire amplifier including the Thevenin equivalent of the input cable, and the equivalent resistive load of the output cable. (Again, ignore the coupling capacitors.) Clearly label the value of each component in the amplifier model in terms of R, I_1, I_2, β_F and V_{th}. If you choose to label the components with symbols such as g_m and R_π, make sure to express those symbols in terms R, I_1, I_2, β and V_{th}. *(Neat drawing and appropriate expressions expected).*

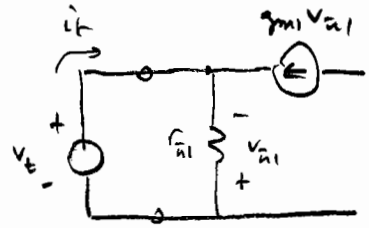


$$g_{m1} = \frac{I_1}{V_{th}} \qquad g_{m2} = \frac{I_2}{V_{th}}$$

$$r_{\pi 1} = \frac{\beta_F}{g_{m1}} \qquad r_{\pi 2} = \frac{\beta_F}{g_{m2}}$$

1c) *(2 points) Analytically* determine the input resistance of the amplifier. Express the result in terms of R, I_1, I_2, β_F, V_{th}, and R_{L}.

The input to the circuit looks like:



Note that

$$v_{\pi1} = -v_t$$

Then

$$i_t = -\frac{v_{\pi1}}{r_{\pi1}} - g_{m1}v_{\pi1} = v_t\left(\frac{1}{r_{\pi1}} + g_{m1}\right) \simeq v_t g_{m1}$$

And

$$R_{in} = \frac{1}{g_{m1}} = \frac{V_{th}}{I_1}$$

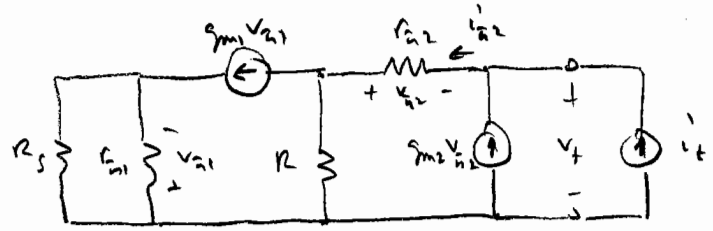
1d) *(2 points)* What must be the *numerical* value of I_1 so that the input resistance found in Part (1c) is 50 Ω?

Solving for I_1:

$$I_1 = \frac{V_{th}}{R_{in}} = \frac{0.025}{50} = 0.5\ \text{mA}$$

1e) *(2 points) Analytically* determine the output resistance of the amplifier. Express the result in terms of R, I_1, I_2, β_F, V_{th}, and R_S.

We draw the output portion of the amplifier:



Note that $v_{\pi1} = 0$ and $g_{m1}v_{\pi1} = 0$. Then

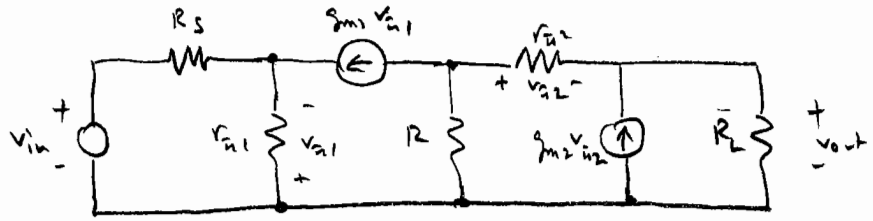
$$v_{\pi2} = -r_{\pi2}\, i'_{\pi2}$$

and

$$i'_{\pi2} = i'_t + g_{m1}v_{\pi2} = i'_t - g_{m2}r_{\pi2}i'_{\pi2} \Rightarrow i'_{\pi2} = \frac{i'_t}{1+\beta_F} \approx \frac{i'_t}{\beta_F}$$

Then $V_t = (R + r_{\pi2})\, i'_{\pi2} = \dfrac{R + r_{\pi2}}{\beta_F}\, i'_t = \left(\dfrac{R}{\beta_F} + \dfrac{1}{g_{m2}}\right) i'_t \Rightarrow R_{out} = \dfrac{R}{\beta_F} + \dfrac{1}{g_{m2}}$

1f) *(2 points)* Assume that the amplifier has been designed to have a 50 Ω input resistance and a 50 Ω output resistance. In this case, *analytically* determine the small-signal midband gain of the amplifier from v_{in} to v_{out}. Express the results in terms of R, I_1, I_2, β, V_{th} and $R_S = R_L = 50\ \Omega$. To determine the small-signal midband gain, assume that C_π and C_μ are open circuits.



We relate v_{in} to $v_{\pi1}$:

$$\frac{v_{in} + v_{\pi1}}{R_S} + g_{m1}v_{\pi1} = -\frac{v_{\pi1}}{r_{\pi1}}$$

$$v_{in}\frac{1}{R_S} = -v_{\pi1}\left(\frac{1}{r_{\pi1}} + g_{m1} + \frac{1}{R_S}\right) \approx -v_{\pi1}\left(g_{m1} + \frac{1}{R_S}\right)$$

$$\frac{v_{\pi1}}{v_{in}} = \frac{-1}{1 + g_{m1}R_S}$$

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We relate V_{out} to V_{in2}:

$$\frac{V_{in2}}{r_{in2}} + g_{m2} V_{in2} = \frac{V_{out}}{R}$$

$$V_{in2}\left(\frac{1}{r_{in2}} + g_{m2}\right) \simeq V_{in2} g_{m2} = \frac{V_{out}}{R_L}$$

$$\frac{V_{out}}{V_{in2}} = g_{m2} R_L$$

We relate V_{in1} to V_{in2}:

$$g_{m1} V_{in1} + \frac{V_{in2} + V_{out}}{R} + \frac{V_{in2}}{r_{in2}} = 0$$

$$g_{m1} V_{in1} = -V_{in2}\left(\frac{1}{r_{in2}} + \frac{1 + g_{m2} R_L}{R}\right) = -V_{in2}\frac{R + r_{in2} + \beta_F R_L}{r_{in2} R}$$

$$\frac{V_{in2}}{V_{in1}} = -\frac{g_{m1} r_{in2} R}{R + r_{in2} + \beta_F R_L}$$

All together

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 + g_{m1} R_s} \times \frac{g_{m1} r_{in2} R}{R + r_{in2} + \beta_F R_L} \times g_{m2} R_L = \frac{g_{m1} \beta_F R R_L}{(1 + g_{m1} R_s)(R + r_{in2} + \beta_F R_L)} =$$

$$= \frac{g_{m1} R R_L}{(1 + g_{m1} R_s)\left(\underbrace{\frac{R}{\beta_F} + \frac{1}{g_{m2}}}_{R_{out}} + R_L\right)} = \frac{g_{m1} R R_L}{(1 + g_{m1} R_s)(R_{out} + R_L)}$$

Since $R_{in} = \frac{1}{g_{m1}} = 50\,\Omega$, then $1 + g_{m1} R_s = 2$. Also $R_{out} = R_L = 50\,\Omega$.

All together

$$\frac{V_{out}}{V_{in}} = \frac{R}{200}$$

1g) *(2 points)* What must be the values of R and I_2 so that the output resistance is 50 Ω and the voltage gain is 25? *(Numerical values expected.)*

A voltage gain of 25 can be obtained with

$$R = 25 \times 200 = 5\ k\Omega$$

Output resistance of 50 now demands,

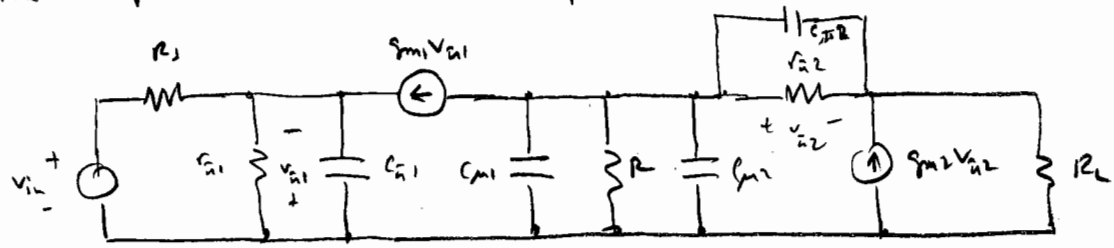
$$R_{out} = 50 = \frac{R}{\beta_F} + \frac{1}{g_{m2}} = \frac{5000}{200} + \frac{1}{g_{m2}} = 25 + \frac{1}{g_{m2}} = 25 + \frac{V_{th}}{I_2}$$

Then

$$I_2 = \frac{V_{th}}{25} = \frac{0.025}{25} = 1\ mA$$

1h) *(2 points) Numerically* estimate the bandwidth of the amplifier under the assumption that it has been designed to provide a 50 Ω input resistance, a 50 Ω output resistance, and a midband gain of 25.

The complete circuit with all caps looks like this:



We derive the time constant for each capacitor.

- $C_{\pi 1}$ is looking right at the input. Hence the Thevenin resistance that it sees is $R_s \,//\, R_{in}$. The time constant is:

$$\tau_{\pi 1} = C_{\pi 1}(R_s \,//\, R_{in}) = 1\ \mu F \times 25\ \Omega = 25\ ps$$

- $C_{\mu 1}$ and $C_{\mu 2}$ are in parallel. Let's compute the Thevenin resistance that they see:

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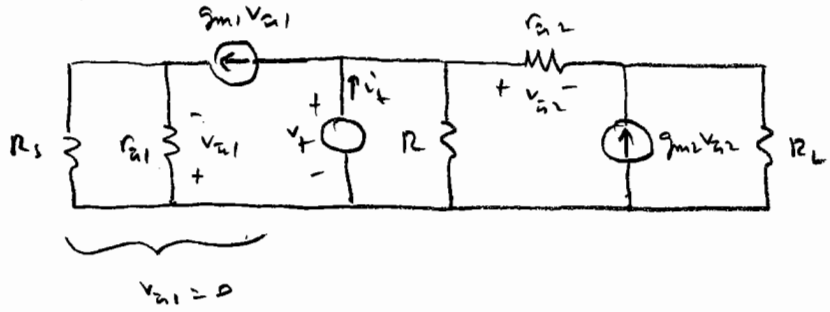


$$i_t = \frac{v_t}{R} + \frac{v_{\pi2}}{r_{\pi2}}$$

$$\frac{v_{\pi2}}{r_{\pi2}} + g_{m2}v_{\pi2} = \frac{v_t - v_{\pi2}}{R_L}$$

$$v_{\pi2}\left(\frac{1}{r_{\pi2}} + g_{m2} + \frac{1}{R_L}\right) = \frac{v_t}{R_L}$$

$$v_{\pi2} = \frac{v_t}{1 + g_{m2}R_L}$$

Then

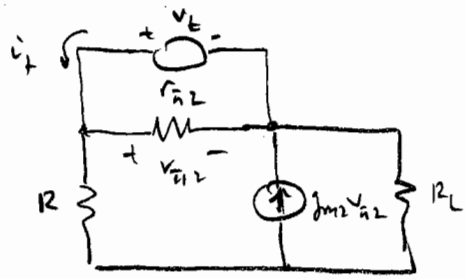
$$i_t = v_t\left\{\frac{1}{R} + \frac{1}{r_{\pi2}(1+g_{m2}R_L)}\right\}$$

Then

$$R_M = R \,//\, (r_{\pi2} + \beta R_L) = 5\,k\,//\,(5k + 200\times 50) = 5k\,//\,15k = 3.75\,k$$

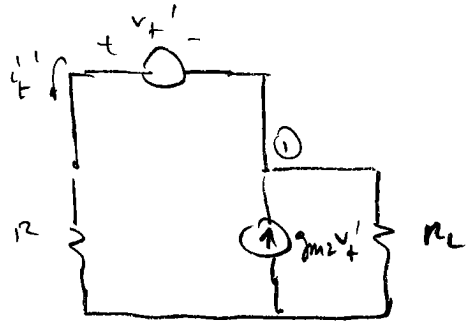
$$\tau_M = (C_{\mu1} + C_{\mu2}) \times R_M = 0.2\,\mu F \times 3.75\,k = 750\,ps$$

- Now $C_{\pi2}$:



Here we see $r_{\pi2}$ in parallel with something else and $V_{\pi2} = V_t$. Then we

analyze



we write a node current eq. for node ①

$$-i_t' + g_{m2}v_t' + \frac{v_t' - i_t'R}{R_L} = 0$$

$$v_t'\left(g_{m2} + \frac{1}{R_L}\right) = i_t'\left(1 + \frac{R}{R_L}\right) \rightarrow R_{th2}' = \frac{v_t'}{i_t'} = \frac{R_L + R}{1 + g_{m2}R_L}$$

and

$$R_{th2} = r_{th2} \,//\, \frac{R_L + R}{1 + g_{m2}R_L} = 5k \,//\, \frac{50 + 5k}{1 + 2} = 5k \,//\, 1.7k = 1.25k\Omega$$

Then $\tau_{th2} = 1.25\ ns$

All together $\Sigma\tau \simeq 2\ ns$ $\quad f_{3dB} \simeq 79\ MHz$

1i) *(2 points)* Assume that the Early Voltage of both transistors is 100 V. In a few sentences, explain why it is reasonable to ignore their collector-emitter output resistances during the analyses above.

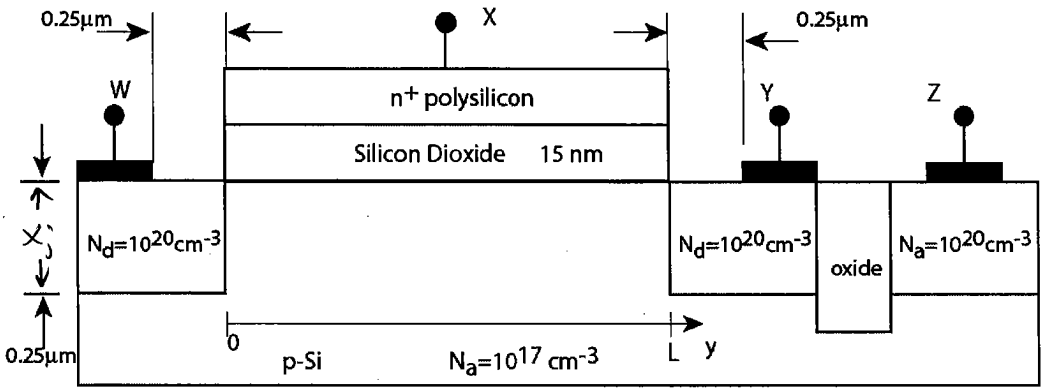
At a current level of 1 mA and 0.5 mA, the output resistance of the BJT's are:

$$r_{o1} = \frac{V_A}{I_1} = \frac{100\ V}{0.5\ mA} = 2\times10^5\ \Omega$$

$$r_{o2} = \frac{V_A}{I_2} = \frac{100\ V}{1\ mA} = 10^5\ \Omega$$

These are much higher than any of the resistances in the picture and they can be neglected.

2. *(21 points)* The device structure shown below has four terminals (W, X, Y, Z) and could be viewed as a n-channel MOSFET or a lateral npn bipolar transistor depending on the voltage applied to the various terminals. When operated as a MOSFET, $C_{ox} = 2.3 \times 10^{-7}\ F/cm^2$, $\gamma = 0.79\ V^{1/2}$, and $V_T = 0.6\ V$. The length of the quasi-neutral p-Si region is $L = 0.15\ \mu m$ and its width is $W = 10\ \mu m$. The electron diffusion coefficient in the p-type body is $D_n = 20\ cm^2/s$.



(2a) *(4 points)* If the device is to be operated as an n-channel MOSFET, identify the terminals *(answer W, X, Y, or Z in the space provided below)*:

Source: W Drain: Y Gate: X Body: Z

(2b) *(3 points)* If the device is to be operated as a lateral npn BJT, identify the terminals *(answer W, X, Y, or Z in the space provided below)*.

Emitter: W Base: Z Collector: Y

(2c) *(2 points)* For the device shown above, what is the flatband voltage of the MOS capacitor formed by connecting terminals W, Y and Z to ground and varying the voltage in terminal X? *(Numerical answer expected)*.

This is the flat-band voltage of a regular MOS structure, with our usual choice of reference:

$$\phi_{nt} = 0.55\ V$$

and

$$\phi_p = -\frac{kT}{q} \ln \frac{N_a}{n_i} = -0.025 \ln \frac{10^{17}}{10^{10}} = -0.40\ V$$

Then, the built-in potential is

$$\phi_B = \phi_{nt} - \phi_p = 0.95\ V$$

And the flat-band voltage is

$$V_{FB} = -\phi_B = -0.95\ V$$

(2d) *(2 points)* We operate the device as a bipolar transistor with V_{XW} biased at the flatband voltage of the MOS capacitor. What is the collector current if the device is biased with $V_{CE} = 2\ V$ and $V_{BE} = 0.6\ V$? *(Numerical answer expected).*

Use regular expression of collector current:

$$I_C = q A_E \frac{n_i^2}{N_a} \frac{D_n}{W_B} \exp \frac{qV_{BE}}{kT}$$

A_E is $x_j \times W$. W_B is L. Then:

$$I_C = 1.6\times10^{-19} \times 0.25\times10^{-4} \times 10\times10^{-4} \frac{10^{20}}{10^{17}} \frac{20}{0.15\times10^{-4}} \exp\frac{0.6}{0.025} = 1.4\times10^{-7}\ A = 0.14\ \mu A$$

(2e) *(2 points)* What is the transit time of electrons across the base region of the BJT when the device is biased as in (2d)? *(Numerical answer expected).*

This is simply given by:

$$\tau = \frac{L^2}{2D_n} = \frac{(0.15\times10^{-4})^2}{2\times20} = 5.6\times10^{-12} = 5.6\ ps$$

(2f) *(4 points)* Now we operate the device as a bipolar transistor with $V_{XW} = 0\ V$. What is the collector current if the device is biased with $V_{CE} = 2\ V$ and $V_{BE} = 0.6\ V$? *(Numerical answer expected).*

With $V_{XW} = 0$ V, there is going to be a depletion region under the gate. This will detract from the emitter area and reduce the collector current. Note that $V_{BE} = V_{ZW}$. Then, there is a voltage applied to the body with respect to the source. This is going to change the thickness of this depletion region.
In the depletion regime, the depletion thickness is given by:

$$X_d(V_{GB}) = \frac{\epsilon_s}{C_{ox}}\left[\sqrt{1 + \frac{4(\phi_f + V_{GB})}{\gamma^2}} - 1\right]$$

We have everything here:

$$X_d = \frac{1.05\times10^{-12}}{2.3\times10^{-7}}\left[\sqrt{1 + \frac{4(0.95-0.6)}{(0.79)^2}} - 1\right] = 3.7\times10^{-6} = 0.037\,\mu m$$

This region under the gate of the MOS does not conduct. Hence the new emitter area for the BJT is:

$$A_E = W_E(x_j - X_d) = 10\times10^{-4}\times(0.25-0.037)\times10^{-4} = 2.1\times10^{-8}\ cm^2$$

The collector current is then:

$$i_C(2f) = \frac{i_C(2d)}{A_E(2d)} \times A_E(2f) = \frac{0.14\ \mu A}{2.3\times10^{-8}} \times 2.1\times10^{-8} = 0.13\ \mu A$$

(2g) *(2 points)* If the device is to be used as a lateral npn BJT in the forward active regime, what is the maximum voltage you should bias the gate relative to the source (V_{GS})? Explain. *(Numerical answer and suitable explanation expected).*

one should avoid the MOSFET from turning on. This happens when $V_{GS} > V_T$. But with the BJT on, V_T shifts negative due to the back gate effect. The new V_T is:

$$V_T' = V_{T0} + \gamma\left(\sqrt{-2\phi_f - V_{BS}} - \sqrt{-2\phi_f}\right)$$

In this case, $V_{BS} = V_{BEon} = 0.6$ V. Then

$$V_T' = 0.6 + 0.79\left(\sqrt{0.8 - 0.6} - \sqrt{0.8}\right) = 0.25\ V$$

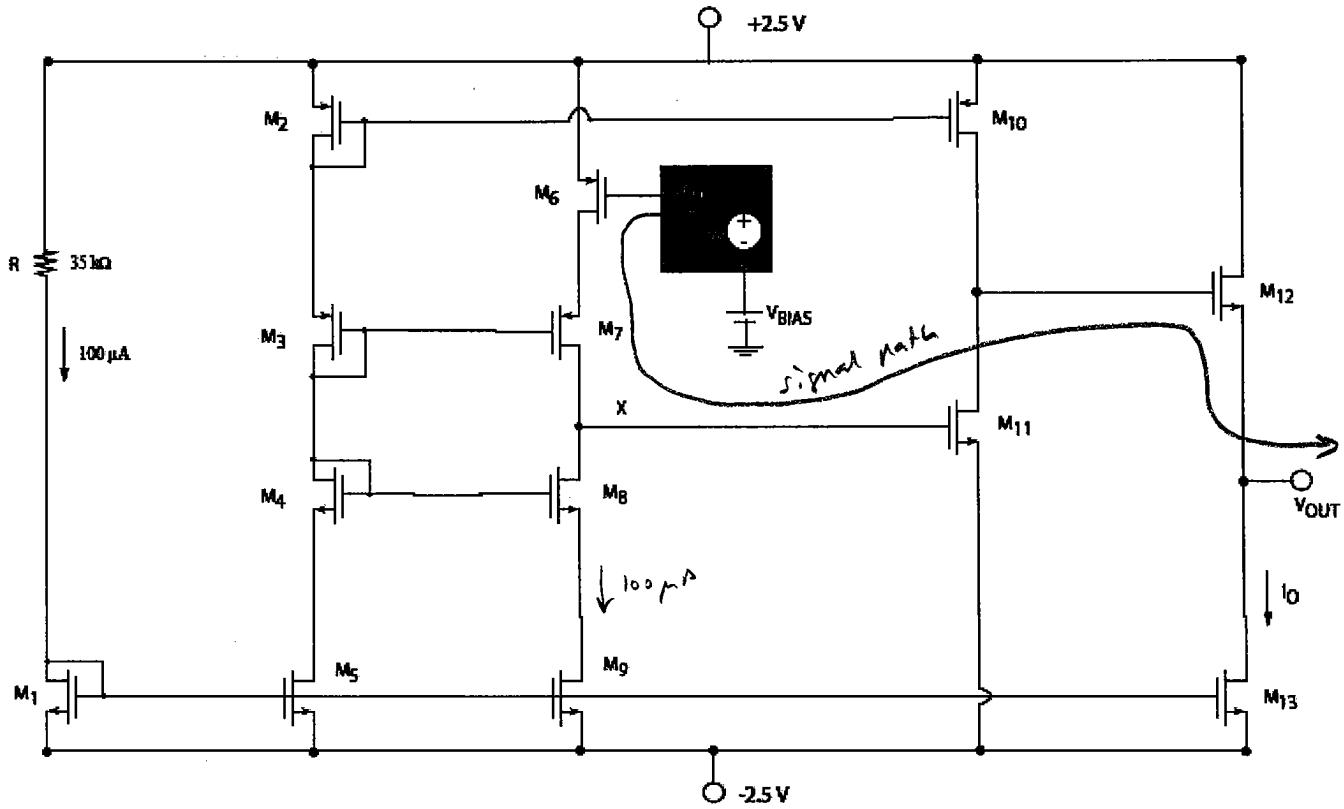
Then V_{GS} should not exceed .25 V

(2h) *(2 points)* If the device is to be used as an n-channel MOSFET in the saturation regime, what is the maximum voltage you should bias the body relative to the source (V_{BS})? Explain. *(Numerical answer and suitable explanation expected).*

In this case, you do not want any bipolar action, so V_{BS} should remain negative.

$V_{BS} <$

3. *(23 points)* Consider the following amplifier below.



These are the relevant technology parameters:

$V_{Tn} = 1.0\ V$, $\mu_n C_{ox} = 100\ \mu A/V^2$, $\lambda_n = 0.01\ V^{-1}$
$V_{Tp} = -1.0\ V$, $\mu_p C_{ox} = 50\ \mu A/V^2$, $\lambda_p = 0.01\ V^{-1}$

The sizes of the devices are as follows (first number indicates width, second number indicates length, both in microns):

M1 = M5 = M9 = 8/1
M4 = M8 = 8/1
M3 = M6 = M7 = 50/1
M2= M10 = 16/1
M11 = M12 = 25/1
M13=?

In this problem, ignore the impact of any backgate transconductance.

(3a) *(1 points)* In the circuit schematic above, trace the signal path from input to output? *(Neat line expected).*

see above

(3b) *(6 points)* List the transistors that perform the following functions:

(i) Signal Amplifier: M6, M7, M11, M12

(ii) Current Supply or Sink: M5, M9, M13, M10

(iii) Voltage Reference: M4, M3, M2, M1

(3c) *(2 points)* Determine V_{BIAS} *(Numerical answer expected).*

Since M9 = M1, the current through M6, M7, M8, and M9 is 100 μA.
For M6 to drive this current, its V_{SG} has to be:

$$I_{DP} = \frac{W}{2L} \mu_p C_{ox} (V_{SG} + V_{TP})^2$$

or

$$V_{SG} = \sqrt{\frac{2L}{W} \frac{I_{DP}}{\mu_p C_{ox}}} - V_{TP} = \sqrt{\frac{2}{50} \frac{100.}{50}} + 1 = 1.28 \text{ V}$$

Then

$$V_{BIAS} = V_{DD} - V_{SG} = 2.5 - 1.28 = 1.22 \text{ V}.$$

(3d) *(2 points)* If $I_O = 200\ \mu A$, what is W/L for M13? *(Numerical answer expected).*

M13 is mirrored off M1 which runs 100 μA. Then the W/L of M13 must be double that of M1:

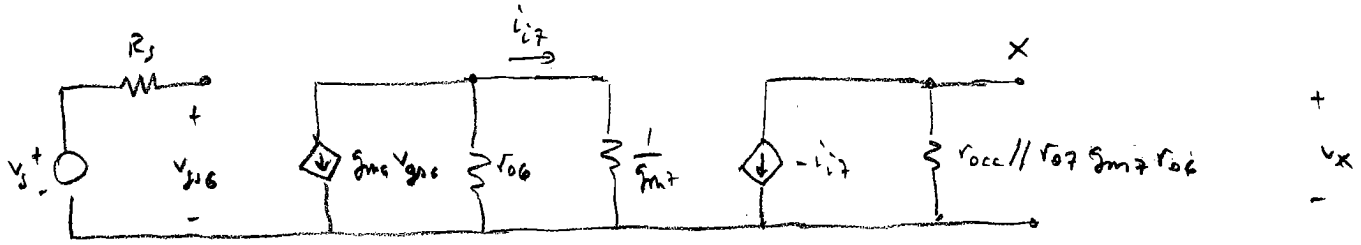
$$M13 = \frac{16}{1}$$

(3e) *(8 points)* Estimate the voltage gain at point X, that is, calculate v_x/v_s. *(Numerical answer expected).*

The output resistance of the cascode current source (M8+M9) is given in Rodinia's notes (p. 587):

$$r_{OCC} = g_{m8}\, r_{O8}\, r_{O9}$$

The voltage gain up to X can be obtained by stringing together the two small-signal equivalent circuit models of both stages:



Since $r_{O7} >> \frac{1}{g_{m7}}$, then

$$i_{i7} \triangleq -g_{m6} v_{gs6} = -g_{m6} v_s$$

[this page intentionally left blank]

Now

$$V_x = -i_{i7}\,(r_{occ} \,//\, g_{m7} r_{o7} r_{o6}) = g_{m6}(\quad) V_s$$

Then, the voltage gain is:

$$A_v = \frac{V_x}{V_s} = g_{m6}\,(r_{occ} \,//\, g_{m7} r_{o7} r_{o6})$$

Let us put HI:

$$g_{m6} = g_{m7} = \sqrt{2 \frac{W}{L} \mu_p C_{ox} I_D} = \sqrt{2 \times 50 \times 50 \times 100} = 707\ \mu S$$

$$g_{m8} = \sqrt{2 \times 8 \times 100 \times 100} = 40\ \mu S$$

$$r_{o8} = r_{o9} = \frac{\Delta V}{\lambda I_D} = \frac{1}{0.01 \times 100 \times 10^{-6}} = 10^6\ \Omega$$

$$r_{o6} = r_{o7} = \frac{1}{0.01 \times 100 \times 10^{-6}} = 10^6\ \Omega$$

Then

$$r_{occ} = 40 \times 10^{-6} \times 10^6 \times 10^6 = 40 \times 10^6 = 40\ M\Omega$$

Also

$$g_{m7} r_{o7} r_{o6} = 707 \times 10^{-6} \times 10^6 \times 10^6 = 707 \times 10^6 = 702\ M\Omega$$

Then

$$r_{oc} \,//\, g_{m7} r_{o7} r_{o6} = 38\ M\Omega$$

Finally

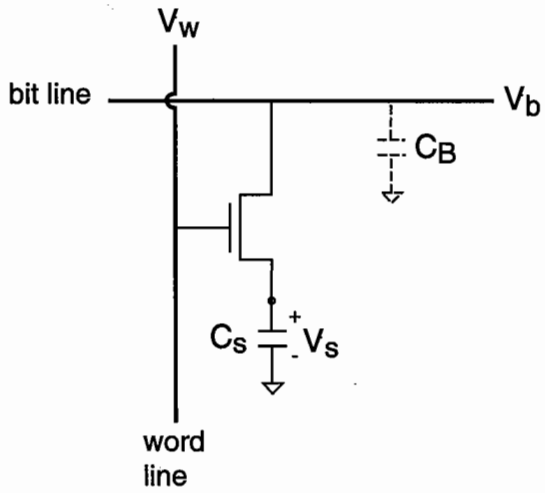
$$A_v = g_{m6}(\quad) = 707 \times 10^{-6} \times 38 \times 10^6 = 2.7 \times 10^4$$

(3f) *(4 points)* What is the output resistance of the amplifier? *(Numerical answer expected).*

The final stage is a common-drain stage with an output resistance given by:

$$R_{out} \simeq \frac{1}{g_{m12}} = \frac{1}{\sqrt{2\frac{W}{L}\mu_n C_{ox} I_D}} = \frac{1}{\sqrt{2 \times \frac{25}{1} \times 100 \times 10^{-6} \times 200 \times 10^{-6}}} = 1\ M\Omega$$

4. *(28 points)* Dynamic random-access memory (DRAM) is widely used in computer applications. This is because DRAMs are relatively fast, can be made very dense and are fairly inexpensive. Consider a one-transistor (DRAM) cell sketched below:



In this DRAM cell, the information is stored in the form of charge in the capacitor C_s. If the voltage across the capacitor V_s is HI, then a "1" is stored. If V_s is LO, a "0" is stored.

The "word line" is used to select cells for reading or writing, as follows:

- if the word line is at *ground* ($V_w = 0$), the cells on that line are not selected for reading or writing;
- if the word line is at $V_w = V_{DD}$, the cells on that line are selected for reading or writing.

The "bit line" is used to write or read the bits. It has three possible states:

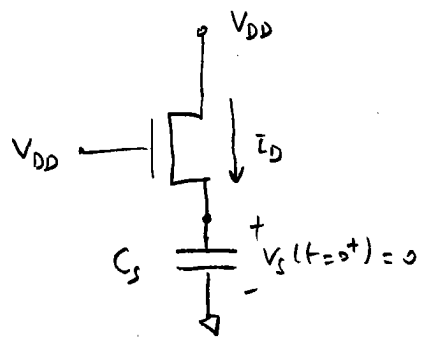
- if the bit line is at $V_b = V_{DD}$, a "1" is to be written
- if the bit line is at $V_b = 0\ V$, a "0" is to be written
- if the bit line is *floating*, the stored bit in the capacitor is to be read.

In this problem you will analyze the basic operation of the DRAM cell. In this DRAM cell the transistor is characterized by the following parameters: $L = 1\ \mu m$, $W = 4\ \mu m$, $\mu_n C_{ox} = 50\ \mu A/V^2$, $V_T = 1\ V$. The storage capacitor is $C_s = 50\ fF$. The bit line has a capacitance $C_B = 500\ fF$. $V_{DD} = 3.3\ V$.

□ Consider the operation of writing a "1" when the cell had a "0" stored at $t = 0^-$, that is, $V_s(t = 0^-) = 0$. At $t = 0$, the word line and the bit line are set to V_{DD} ($V_w = V_b = V_{DD}$).

(4a) *(2 points)* In what regime is the transistor operating at $t = 0^+$? Explain. *(Suitable explanation expected).*

At $t = 0^+$, this is the situation:



The source is at 0 V while the gate and drain are at V_{DD}. Then, the transistor is in saturation.

(4b) *(2 points)* In what regime is the transistor operating at $t \to \infty$? Explain. *(Suitable explanation expected).*

At $t = 0^+$, the transistor is in saturation, therefore, current flows into the capacitor which will charge up. In consequence V_s rises and the amount of overdrive on the transistor gets reduced. As time goes on, the capacitor charges more and more and V_s continues to rise, with the gate and drain both at V_{DD}; the transistor remains in saturation but with less drive as time goes on. Given enough time, V_s will rise until the transistor goes into cut-off. At this point, the current stops flowing and V_s no longer changes. Hence, at $t \to \infty$, the transistor is in cut-off.

(4c) *(4 points)* Estimate the value of V_s at $t \to \infty$. Explain your result. *(Numerical answer and suitable explanation expected).*

As explained in (4b), at $t \to \infty$, the transistor has just cut-off. Hence

$$V_{GS} = V_{DD} - V_S = V_T$$

Hence

$$V_S = V_{DD} - V_T = 3 - 1 = 2\text{V}$$

(4d) *(4 points)* Estimate the charge in C_s at $t \to \infty$. *(Numerical answer expected).*

The charge in the capacitor is simply:

$$Q_S = C_S \times V_S = 50 \times 10^{-15}\,\text{F} \times 2\text{V} = 1.2 \times 10^{-13}\,\text{C} = 0.12\,\mu\text{C}$$

(4e) *(4 points)* Estimate the time that it takes for the capacitor to charge up to 80% of its final value. *(Numerical answer expected).*

The equation that controls the dynamics of the capacitor charge up is:

$$I_D = C_s \frac{dV_s}{dt}$$

Since the transistor remains at all times (but $t \to \infty$) in the saturation regime, then

$$I_D = \underbrace{\frac{W}{2L}\mu_n C_{ox}}_{K} (V_{GS} - V_T)^2 = K (V_{DD} - V_s - V_T)^2$$

Hence we have a simple differential equation to solve:

$$K (V_{DD} - V_s - V_T)^2 = C_s \frac{dV_s}{dt}$$

We separate variables and integrate

$$\frac{K}{C_s} \int_0^t dt = \int_0^{V_s} \frac{dV_s}{(V_{DD} - V_s - V_T)^2} = -\int_0^{V_s} \frac{-dV_s}{(V_{DD} - V_s - V_T)^2} = -\frac{1}{V_{DD} - V_s - V_T}\Big|_0^{V_s}$$

Then

$$t = \frac{C_s}{K} \left(\frac{1}{V_{DD} - V_s - V_T} - \frac{1}{V_{DD} - V_T} \right)$$

The time that it takes to reach 80% of $V_{DD} - V_T$ is:

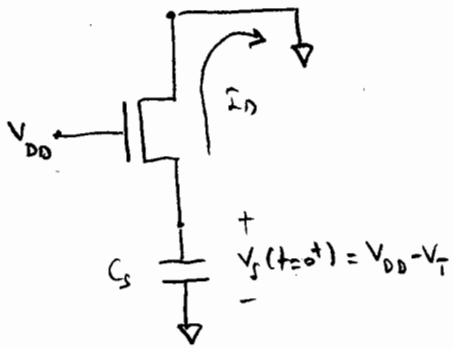
$$t = \frac{C_s}{K} \left[\frac{1}{V_{DD} - V_T - 0.8(V_{DD} - V_T)} - \frac{1}{V_{DD} - V_T} \right] = \frac{C_s}{K} \frac{1}{V_{DD} - V_T} \left(\frac{1}{0.2} - 1 \right) =$$

$$= \frac{C_s \times 4}{K (V_{DD} - V_T)} = \frac{50 \times 10^{-15} \times 4}{2 \times 50 \times 10^{-6} \times 2.3} = 8.7 \times 10^{-10} = 0.87 \text{ ns}$$

□ Now consider the operation of writing a "0" when the cell stored a "1" at $t = 0^-$, that is, $V_s(t = 0^-) = V_s(HI)$ from previous part (if you didn't solve for (4c), assume that $V_s(HI) = V_{DD}$). At $t = 0$, the word line is set to V_{DD} ($V_w = V_{DD}$) and the bit line is set to zero ($V_b = 0$).

(4f) *(2 points)* In what regime is the transistor operating at $t = 0^+$? Explain. *(Suitable explanation expected).*

At $t = 0^+$, this is the situation:



Notice that in this case, current will bleed off upwards through the MOSFET into ground. The top terminal is therefore the source and the bottom one is the drain. Then

$$V_{GS} = V_{DD}$$

$$V_{DS} = V_{DD} - V_T = V_{GS} - V_T$$

Hence the transistor is right at the boundary between the linear and the saturation regimes.

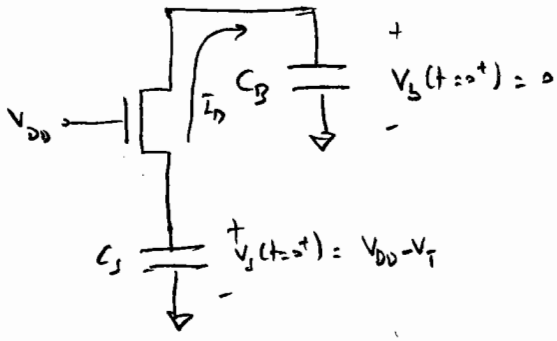
(4g) *(2 points)* In what regime is the transistor operating at $t \to \infty$? Explain. *(Suitable explanation expected).*

As $t \to \infty$, the charge will bleed off through the transistor. Since $V_{GS} = V_{DD}$ at all times, the transistor is always on though in the linear regime. As $t \to \infty$, $V_s \to 0$, and $V_{DS} \to 0$ but since $V_{GS} = V_{DD}$, there is an inversion layer under the gate and the transistor is in the linear regime, though with $V_{DS} = 0$.

□ Now consider the operation of reading a "1". In this case, again, $V_s(t = 0^-) = V_s(HI)$ (if you didn't solve for (4c), assume that $V_s(HI) = V_{DD}$). At $t = 0$, the word line is set to V_{DD} ($V_w = V_{DD}$) and the bit line is left floating with an initial value $V_b(t = 0^-) = 0$.

(4h) *(2 points)* In what regime is the transistor operating at $t = 0^+$? Explain. *(Suitable explanation expected).*

This is the situation at $t = 0^+$:



This is a situation identical to that of 4f. The transistor is therefore at the boundary between the linear and the saturation regimes.

(4i) *(2 points)* In what regime is the transistor operating at $t \to \infty$? Explain. *(Suitable explanation expected).*

As t evolves, the charge in C_J will bleed through the transistor and charge C_B. The flow of charge will stop when $V_J = V_b$. At that point, V_{DS} across the transistor is zero. Since

$$C_B >> C_J$$

the final value of voltage

$$V_J(t \to \infty) = V_b(t \to \infty) << V_{DD} - V_T$$

Hence the transistor is in, or in the linear regime.

(4j) *(4 points)* Estimate the value of $V_b(t \to \infty)$. *(Numerical answer expected).*

The charge that exists at $t = 0^+$ in C_S, at $t \to \infty$ has to then redistributed between C_S and C_B so that the voltage is the same.

The charge at $t = 0^+$ is

$$Q_S(t = 0^+) = C_S V_S(t = 0^+) = 0.2\ \mu C$$

The charge at $t \to \infty$ is

$$Q_S(t \to \infty) + Q_B(t \to \infty) = C_S V_S(t \to \infty) + C_B V_b(t \to \infty) =$$
$$= (C_S + C_B) V_b(t \to \infty) = Q_S(t = 0^+)$$

Then

$$V_b(t \to \infty) = \frac{Q_S(t = 0^+)}{C_S + C_B} = \frac{0.12\ \mu C}{50 + 500\ fF} = 0.22\ V$$