3.155J / 6.152J

Micro/Nano Processing Technology

TAKE-HOME QUIZ

FALL TERM 2005

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1) This is an open book, take-home quiz. You are not to consult with other class members or anyone else. You may discuss the solution to this exam only with the course staff.

2) **The quiz is due on Wednesday, December 14, AT THE START OF CLASS. You should hand in the quiz, rather than submitting it through the course website.**

3) There are parts of this quiz which will have more than one correct answer. Explain your answers, showing how and why you arrived at your solution either with analytical expressions, written explanations, or both.

4) Reference any source of specific material parameters, which includes title of article or book, journal, author and page number. For the class texts, you can simply indicate: Plummer, pg. #. You may find it faster and easier to use charts rather than equations, but in some situations that may not be possible and the theoretical equations (eg. Deal-Grove) must be used. <u>Assume intrinsic diffusion</u>.

5) Justify any assumptions (and you will certainly have to make some). Indicate where you make assumptions or approximations.

6) Some questions require qualitative answers. Keep them brief and focused on the most significant features.

7) GRADING: The submitted material should be clearly written and concise. The grader will spend a maximum of 30 minutes grading each submission. Poorly written or overly voluminous reports will therefore be penalized.

PROBLEM STATEMENT

Knowles recently introduced a MEMS microphone. The only public information on the process and design of this microphone is what is contained in a recently issued Knowles patent (the '090 patent). Your assignment is to develop a detailed process sequence for the fabrication of this device. In addition, you are being asked to develop a process which integrates the microphone with a depletion-mode MOSFET.

Part 1 (75 points)
You should develop a process flow with a level of detail equivalent to the attached process flow (i.e. temperatures, times, implant doses). Your process can only utilize the capabilities of the fabrication facility detailed in an attached description. Write your process description in the same form as the sample process flow attached, with supporting calculations appended. Also included in the process flow should be rough cross-sectional drawings of the wafer at various steps in the process. The detailed specs for the microphone and MOSFET are listed on the next page. In order to integrate the MOSFET, you may need to change the order of some of the steps in the '090' patent, and you will certainly need to add steps. Be sure to keep track of the backside of the wafer (i.e. if it gets doped, or has film deposited on it, make sure you explicitly include steps to remove films or protect the back as needed).

Part 2 (20 points)
Roughly sketch the masks (for one device) that would be needed to fabricate the device. All features should be no smaller than 5 microns.

Part 3 (5 points)
Draw a final cross-section of your device, with the masks generated in Part 2. Label all critical sizes.

Notes regarding implants and diffusions:

1) Assume that the silicon dioxide / silicon interface is reflecting for the dopants (i.e. there is no diffusion across the boundary).
2) To simplify calculations, choose implant conditions such that the implant may be treated as an impulse of dopant at the surface for subsequent diffusions.
3) Assume all diffusions are intrinsic and non-interacting.
4) You will need to make an assumption about the rate of lateral diffusion of dopants.
5) Intrinsic Diffusion Coefficients in Silicon (cm^2/s). Neglect diffusion at temperatures below 900°C. If you need a diffusion coefficient at another temperature, extrapolate using these numbers and assuming an exponential temperature behavior.

	900°C	1000°C	1100°C
Arsenic	2×10^{-16}	4×10^{-15}	5×10^{-14}
Boron	8×10^{-16}	2×10^{-14}	2×10^{-13}
Phosphorus	8×10^{-16}	1×10^{-14}	1×10^{-13}

MICROPHONE AND MOSFET Specs

Assume wafers are 750 micron thick (8” diameter)

Microphone:

Backplate

Heavily boron doped – to serve as an etch stop
Thickness = 10 micron
Pressure relief holes spaced 50 microns apart (center to center)
Pressure relief holes = 10 micron diameter

Backplate to Membrane Gap = 1 micron

Membrane

Formed by fusion bonding of a SOI wafer
Doping level = 10^{16} cm^{-3} (p-type)
Thickness = 2 micron
Surface facing the backplate should be heavily p-doped ~ 10^{19} cm^{-3} to form a good capacitor. You should minimize the depth of this doped region to minimize stress effects.
Top surface should have a p-doped region only in the area where contact is made to the membrane. This can be accomplished at the same time as the substrate contact to the MOSFET, and has the same specs.
Diameter (to support pillars) = 500 micron

MOSFET

Depletion mode, poly gate nMOS
Channel length = 5 micron
Channel width = 100 micron
Gate oxide thickness = 20nm
Poly thickness = 0.5 micron
Field oxide thickness = 0.25 micron (note you don’t have Si_3N_4 and thus can not perform the LOCOS process)
Channel doping (n-type) = 10^{17} cm^{-3} at surface, 10^{16} cm^{-3} at 0.25 micron
Source/Drain junction depth = 0.25 micron
Source/Drain surface doping (n-type) = 10^{19} cm^{-3}
Substrate contact – need to include a p-type diffusion to make contact to substrate and membrane of microphone
Substrate contact doping level at surface = 10^{19} cm^{-3}
Single level metal: Al, 1 micron thick

Connections

The gate of the MOSFET should be connected by the Al layer to the membrane. Each of the other electrical connections (source, drain, two backplate regions – 2A and 2B in the patent) should be connected to 75 micron x 75 micron bonding pads (using the Al layer) which sit on the field oxide and are distributed around the microphone membrane.

TYPICAL PROCESS FLOW SHEET

Starting Material: 8" diameter, (100) silicon (n-type, 10^{14} cm^{-3}), 700 µm thick

Steps:

1) RCA clean
2) Grow SiO_2. Desired Thickness = 250 Å, Temp = 1000°C, Time = 20 minutes, Ambient = Dry 02. This oxide is to minimize channeling during the implant step.
3) Implant back-side of wafer to improve back-side contact. Energy = 100 keV , Dose = $5x10^{15}$ cm^{-2}, Element = Phosphorus.
4) Timed etch in BOE (Buffered Oxide Etch) to remove oxide. Rate = 1000 Å/min, Time = 35 seconds. (Includes 20 second over-etch to ensure completion.)
5) RCA clean
6) Grow SiO_2. Thickness = 1000Å, Temp = 950°C, Time = 20 minutes , Ambient = Wet O2 . This oxide is used to mask the implants in steps 9 and 12.
7) Photolithography - Mask #1. Dark Field
8) Timed etch in BOE (Buffered Oxide Etch) to pattern oxide. Rate = 1000 Å/min, Time = 80 seconds. End this process step with a photoresist strip.
9) Implant front-side of wafer with a n-type dopant. Energy = 50 keV, Dose = $2.6x10^{14}$ cm^{-2}, Element = Arsenic.
10) Photolithography - Mask #2. Dark Field
11) Timed etch in BOE (Buffered Oxide Etch) to pattern oxide. Rate = 1000 Å/min, Time = 80 seconds . End this process step with a photoresist strip.
12) Implant front-side of wafer with a p-type dopant. Energy = 20 keV , Dose = $5x10^{12}$ cm^{-2}, Element = Boron.
13) Timed etch in BOE (Buffered Oxide Etch) to remove all oxide. Rate = 1000 Å/min, Time = 80 seconds .
14) RCA clean
15) Grow SiO_2. Thickness = 1000 Å, Temp = 1100°C, Time = 40 minutes Ambient = Dry O2 . To facilitate hand calculations of the diffusion, we assume the Si/SiO_2 boundary is stationary when determining junction depths.
16) Dopant Drive-In. Temp = 1100°C, Time = 1.2 hours, Ambient = N2 .
17) Deposit LPCVD Polysilicon. The poly will be in-situ doped with Phosphorus. Thickness = 5000 Å Temp = 600°C. (We neglect diffusion during this deposition.)
18) Photolithography - Mask #3. Clear field.
19) Etch polysilicon in SF_6 plasma. (Assume infinite selectivity with oxide.) End this process step with a photoresist strip.
20) Strip polysilicon from back-side in SF_6 plasma.

MICROFABRICATION FACILITY

- 1000 ft^2 testing and packaging area including automatic parametric tester, die-bond and wire-bonding machines, and a plastic injection molding machine.
- All equipment is designed for 8” silicon wafers, and a vendor of silicon wafers is available who can supply any dopant type, concentration, and orientation needed. You can also purchase SOI wafers.

Process Equipment:

RCA Clean station

Acid Station

Solvent Station

8 furnaces:

1. Gate Oxidation (N_2, Dry 0_2)
2. General Purpose Oxidation (N_2, Dry and Wet 0_2)
3. Solid source boron doping
4. Solid source phosphorous doping
5. Dopant drive-in
6. Metal Sinter (400°C)
7. Silicon Fusion Bond Anneal Furnace with Wet and Dry Oxidation capability
8. LPCVD Polysilicon (625°C, Growth Rate = 0.5µm/hour, in-situ doping capability)

Epitaxial Silicon available through a local vendor (1100°C, Growth Rate = 1000Å/min, n-type or p-type doping from 10^{14} cm^{-3} to 10^{19} cm^{-3})

Plasma Etcher (gases for Si, SiO_2, and Si_3N_4 etching)

Plasma Deposition System (for SiO_2 - 400°C)

Ion Implantation (available through a local vendor across the street)

Metal Sputter Deposition System and Evaporation System

Full photolithography system:

Contact Aligner

min. feature size = 2 µm

alignment tolerance = ±1 µm

Spinner for resist and other films, Develop Station, Ovens, and Plasma Stripper

KOH Etching Bench: This includes a mechanical apparatus for performing one-sided etching. (Details on this apparatus are attached.)

Optical Microscopes, Ellipsometer, Dektak surface profiler, Sheet Resistivity Monitor

Packaging area including automatic parametric tester, die-bond and wire-bonding machines