Lecture 39 - Bipolar Junction Transistor
(cont.)

May 11, 2007

Contents:

1. Evolution of BJT design
2. Bipolar issues in CMOS

Announcement:

Final Exam: Wednesday, May 23, 1:30-4:30 PM
Covers entire subject, but will emphasize lectures #24-39 (MOSFET and BJT). *Calculator required.* Open book.

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Key questions

- How has BJT design evolved since its first integration? How is it likely to evolve in the future?
- Bipolar issues in CMOS???

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1. Evolution of BJT design

- *Junction-isolated BJT*

First integrated BJT.

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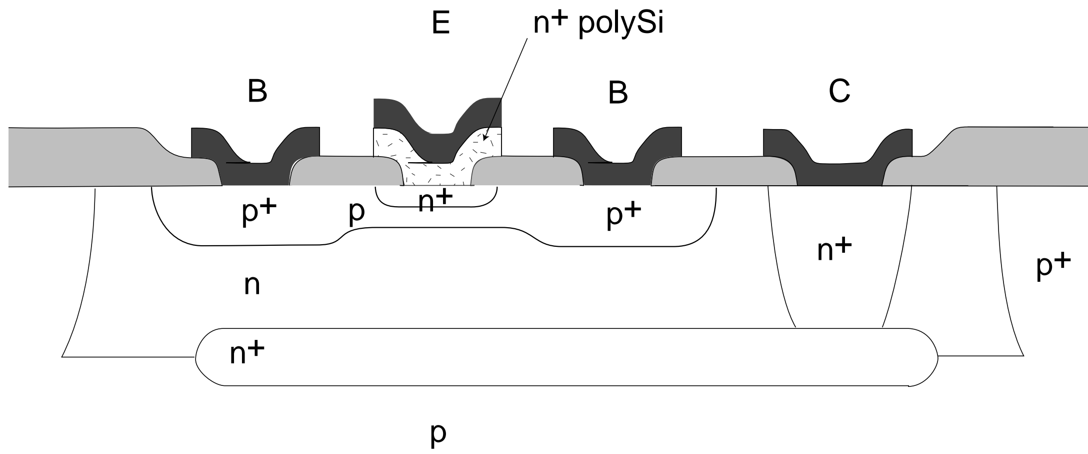
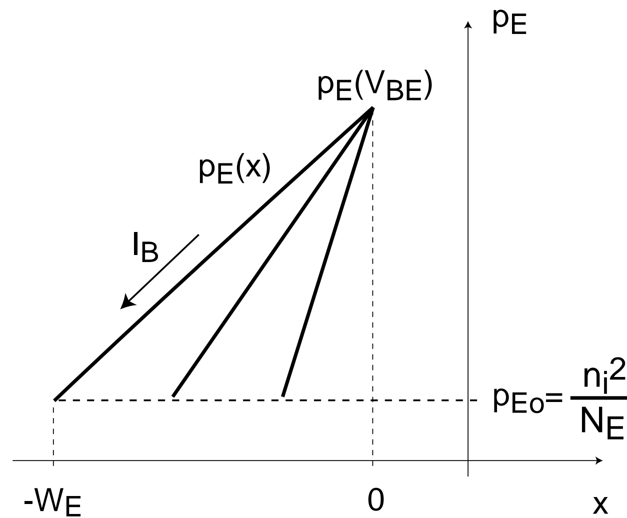
• *Poly-Si emitter BJT*



Problem of metal-contacted emitter: emitter thickness scales badly.



$$W_E \downarrow \Rightarrow I_B \uparrow \Rightarrow \beta_F \downarrow$$

Poly-Si extension effectively increases emitter thickness: β_F preserved when W_E scales down.

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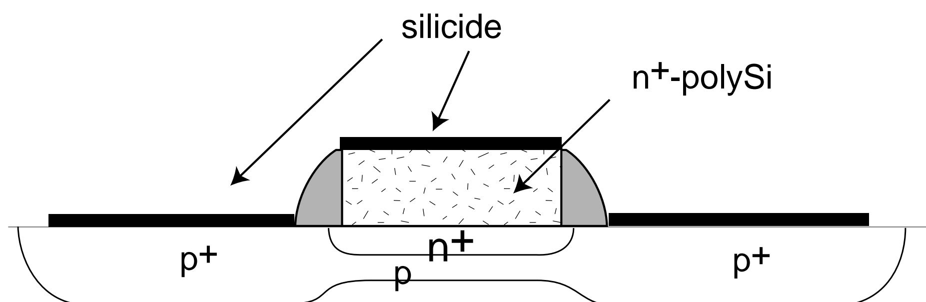
• *Single-poly self-aligned BJT*



Unique feature:

-extrinsic base self-aligned to intrinsic device $\Rightarrow \frac{A_C}{A_E} \downarrow, R_{Bext} \downarrow$

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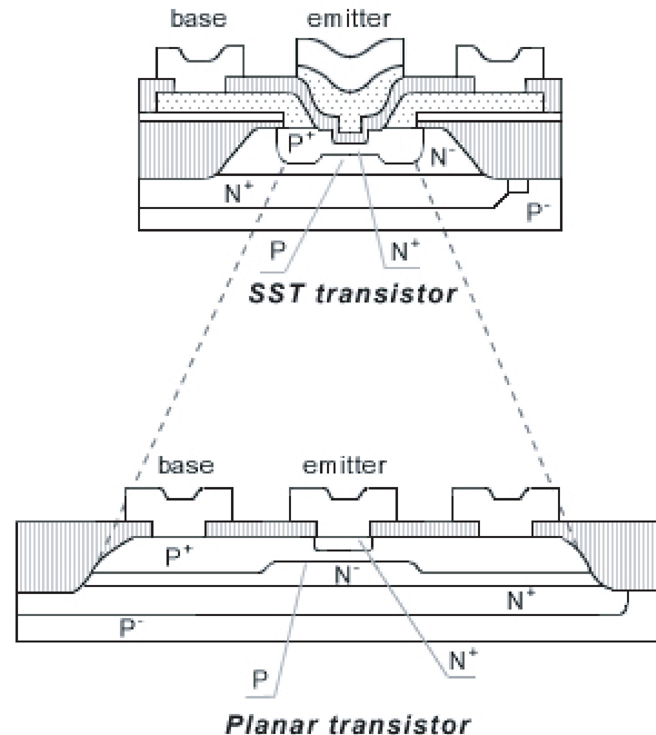
- *Double-poly self-aligned BJT*



Bipolar transistor structure using
Super Self-aligned Process Technology (SST).
Adapted from T. Nakamura,
***IEEE Trans. Electron Dev. 42** (3), 390 (1995).*

Figure 3 in: Nakamura, T., and H. Nishizawa. "Recent Progress in Bipolar Transistor Technology." *IEEE Transactions on Electron Devices* 42, no. 3 (1995): 390-398. © 1995 IEEE.

Unique feature:

-base contacts made on polySi over isolation $\Rightarrow \frac{A_C}{A_E} \downarrow$, smaller footprint

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• *Selectively-implanted collector (SIC) BJT*

Figure removed due to copyright restrictions.

Unique feature:

-intrinsic collector doping level raised through self-aligned implant
$\Rightarrow\ J_{Cmax}\uparrow, f_T\uparrow$

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- *Trench-isolated BJT*

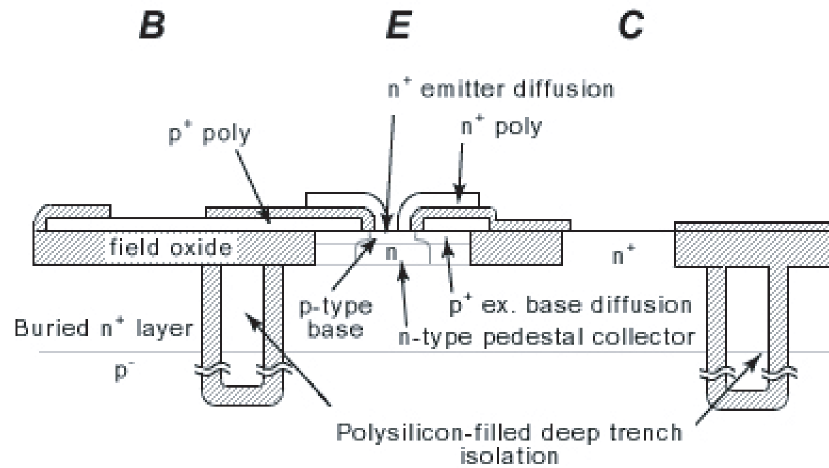

Figure 3 in Warnock, J. "Silicon Bipolar Device Structures for Digital Applications: Technology Trends and Future Directions." *IEEE Transactions on Electron Devices* 42, no. 3 (1995): 377-389.
© 1995 IEEE.

Unique feature:

-deep-trench isolation $\Rightarrow \; A_S \downarrow$

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• *SOI-BJT*

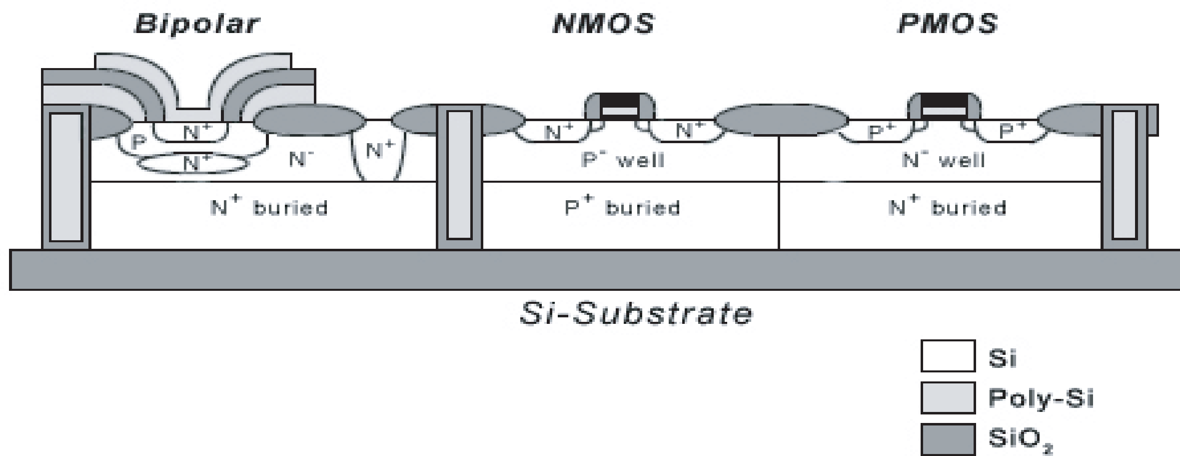

Figure 15 (a) on p. 396 in: Nakamura, T., and H. Nishizawa. "Recent Progress in Bipolar Transistor Technology." *IEEE Transactions on Electron Devices* 42, no. 3 (1995): 390-398. © 1995 IEEE.

Unique feature:

-silicon-on-insulator substrate $\Rightarrow$ $C_S \downarrow$, smaller footprint

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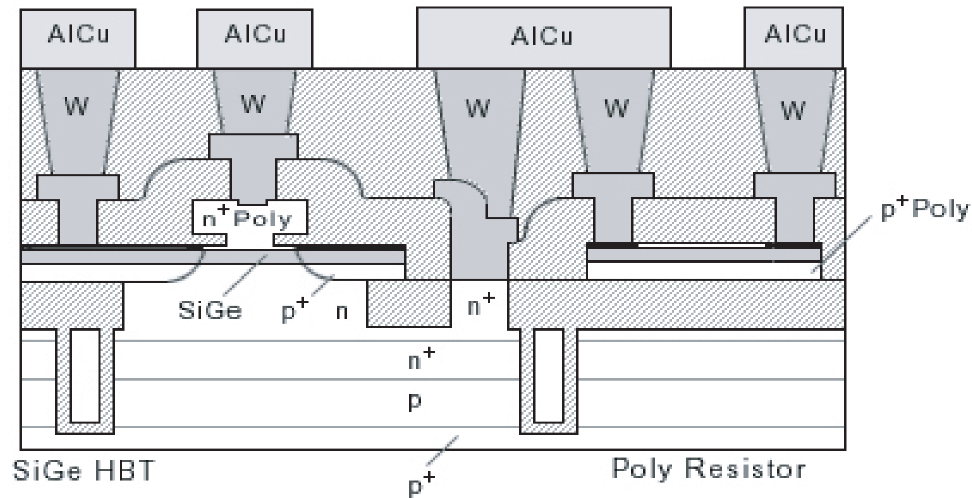
• *Epitaxial SiGe HBT*



*Schematic cross section of the SiGe HBT used in this investigation. Adapted from J. A. Babcock et al., **IEDM**, 1995, p. 357.*

Figure 1 on p. 357 in Babcock, J. A., J. D. Cressler, L. S. Vempati, A. J. Joseph, D. L. Harame. "Correlation of Low-frequency Noise and Emitter-base Reverse-bias Stress in Epitaxial Si- and SiGe-base Bipolar Transistors." International Electron Devices Meeting, Washington, DC, December 10-13, 1995. Technical Digest. Piscataway, NJ: Institute of Electrical and Electronics Engineers, 1995, p. 357-360. ISBN: 9780780327009. © 1995 IEEE.

Unique features:

-epitaxial base: enhanced thickness and doping control $\Rightarrow W_B \downarrow N_B \uparrow \rightarrow f_T \uparrow, R_B \downarrow$

-Ge in base: heterojunction effect, drift field in base (if gradient in Ge composition) $\Rightarrow I_S \uparrow, f_T \uparrow, R_B \downarrow, V_A \uparrow$

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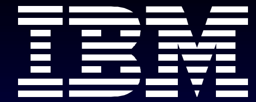
SiGe HBT Cross Section (0.25μm SiGe BiCMOS)



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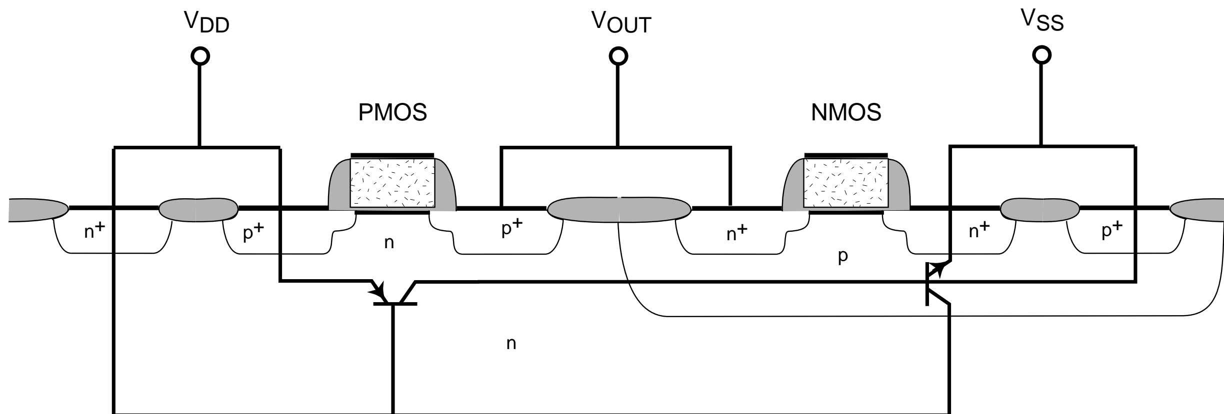
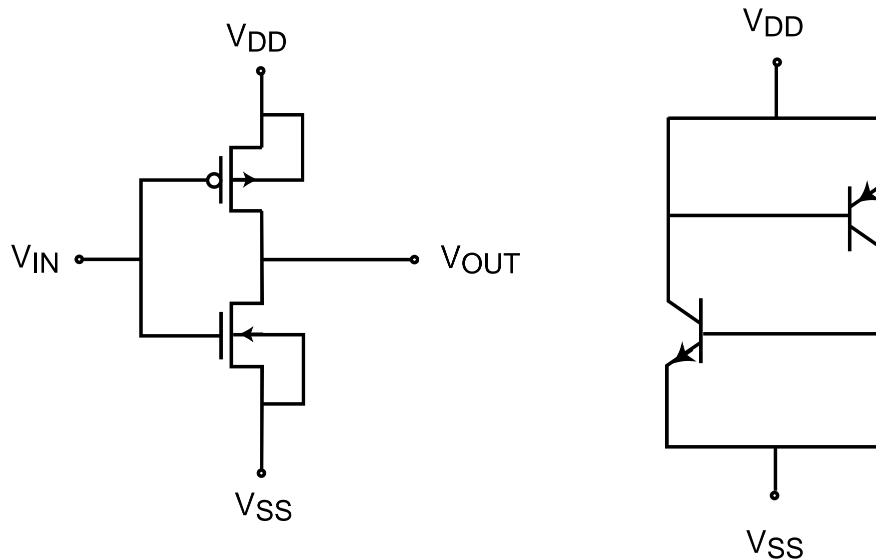
2. Bipolar issues in CMOS

□ *Latch up*: interaction of two hidden BJT's inside a CMOS pair.





In principle, no problem because in both BJTs, $V_{BE} = 0$.

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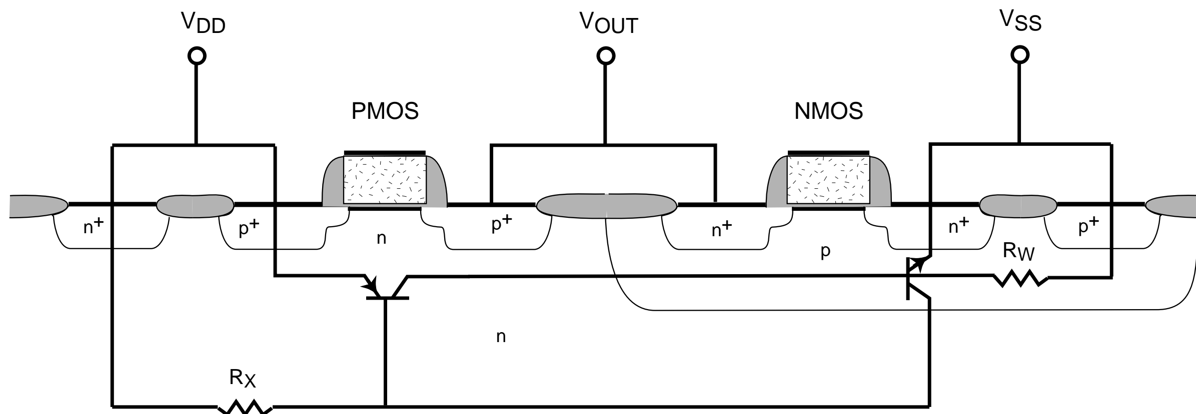
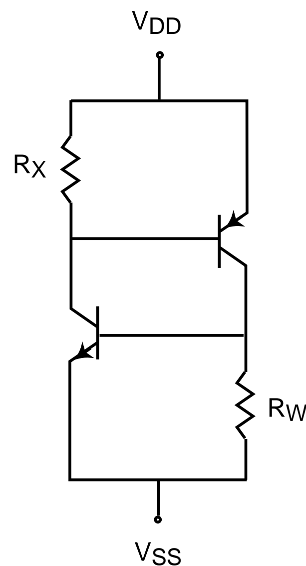
But there are also two parasitic resistors:



More complete equivalent circuit model:



Suppose for some reason, current flows through $R_X \Rightarrow$ pnp goes into FAR $\Rightarrow I_C(pnp) \uparrow \Rightarrow$ ohmic drop in R_W $\Rightarrow$ npn goes into FAR $\Rightarrow I_C(npn) \uparrow \Rightarrow$ more ohmic drop in R_X

Positive feedback loop can cause device destruction.

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Latch-up started by:

- minority carrier injection into substrate by transient forward bias on pn junctions (typically in input or output circuits)
- photogeneration by ionizing radiation
- impact ionization by hot carriers

Elimination of latch up:

- reduce R_X and R_W
- reduce β_{npn} and β_{pnp}

Then do:

- use heavily doped substrate (need lower doping epi layer on top for devices)
- sufficient transistor spacing
- guard rings at sensitive locations

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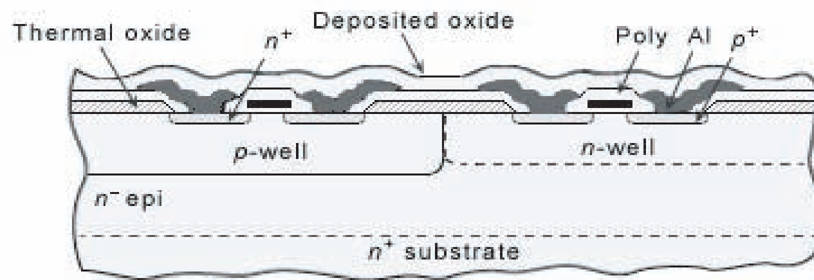
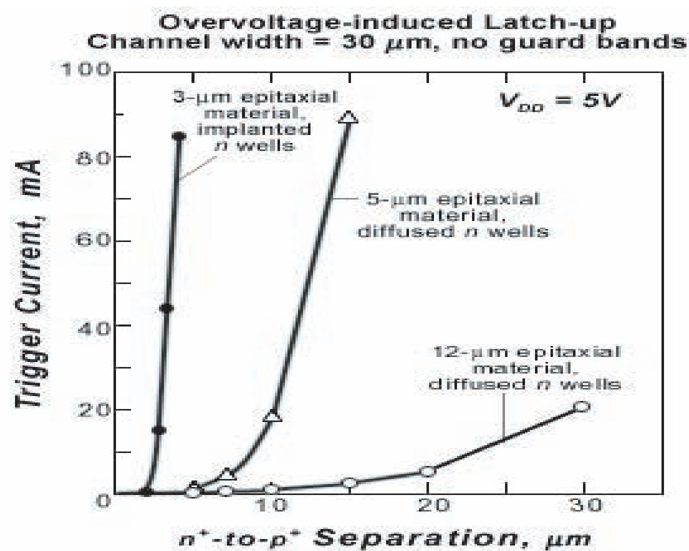


An advanced twin-well process for VLSI CMOS applications. The high-conductivity substrate reduces susceptibilty to latch-up; the separately doped well regions provide precise control of MOSFET characteristics.

Adapted from R. S. Muller and T. I. Kamins, ***Device Electronics for Integrated Circuits, 2nd ed.****, Wiley, 1986, p. 463.*

Image by MIT OpenCourseWare.



An n-well CMOS (a) structure with butted contacts and (b) triggering current vs. n+-to-p+ separation.

Adapted from E. S. Yang, ***Microelectronic Devices****, McGraw Hill, 1988, p. 315.*

Image by MIT OpenCourseWare.

- the higher the trigger current, the higher the immunity to latch-up
- thinner epi on top of n^+-substrate → better immunity
- larger n^+-p^+ spacing → better immunity

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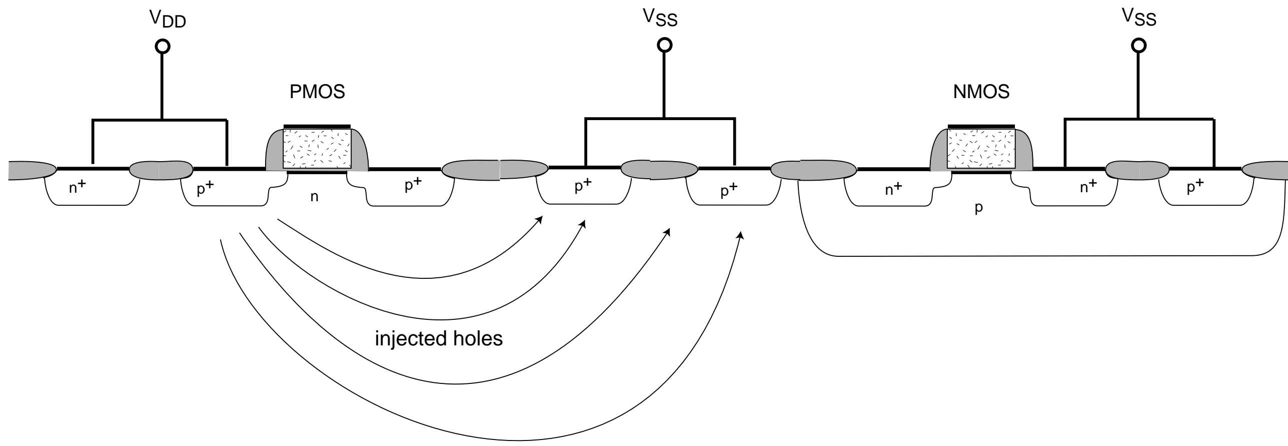
Guard ring: reverse-biased pn junction that collects injected holes.



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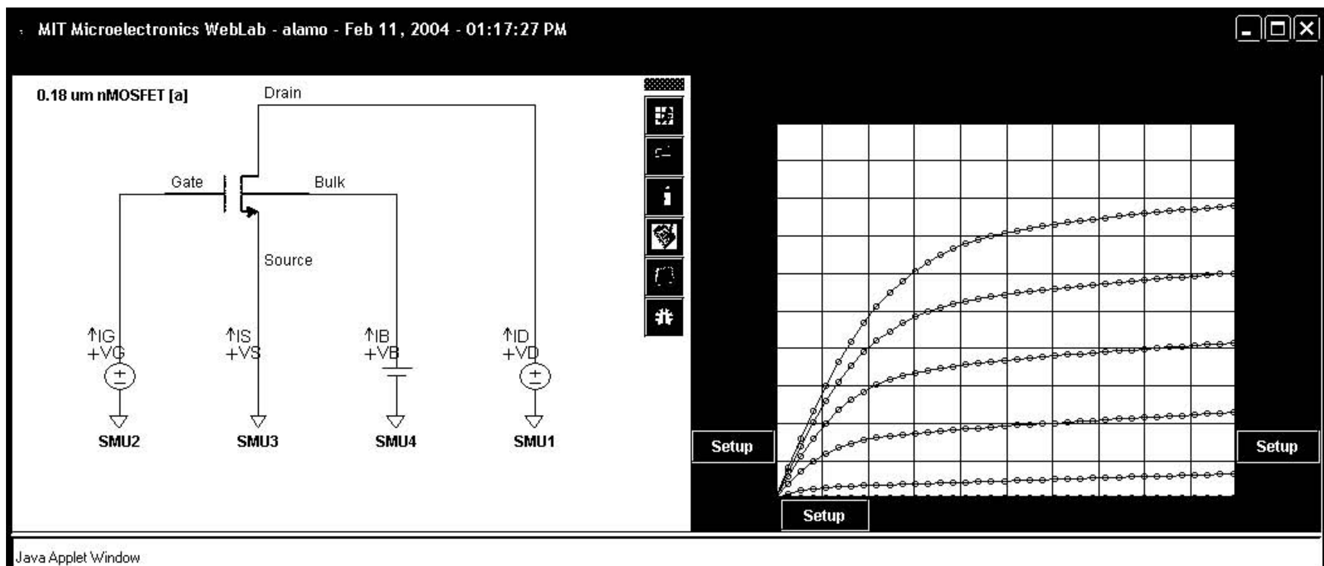
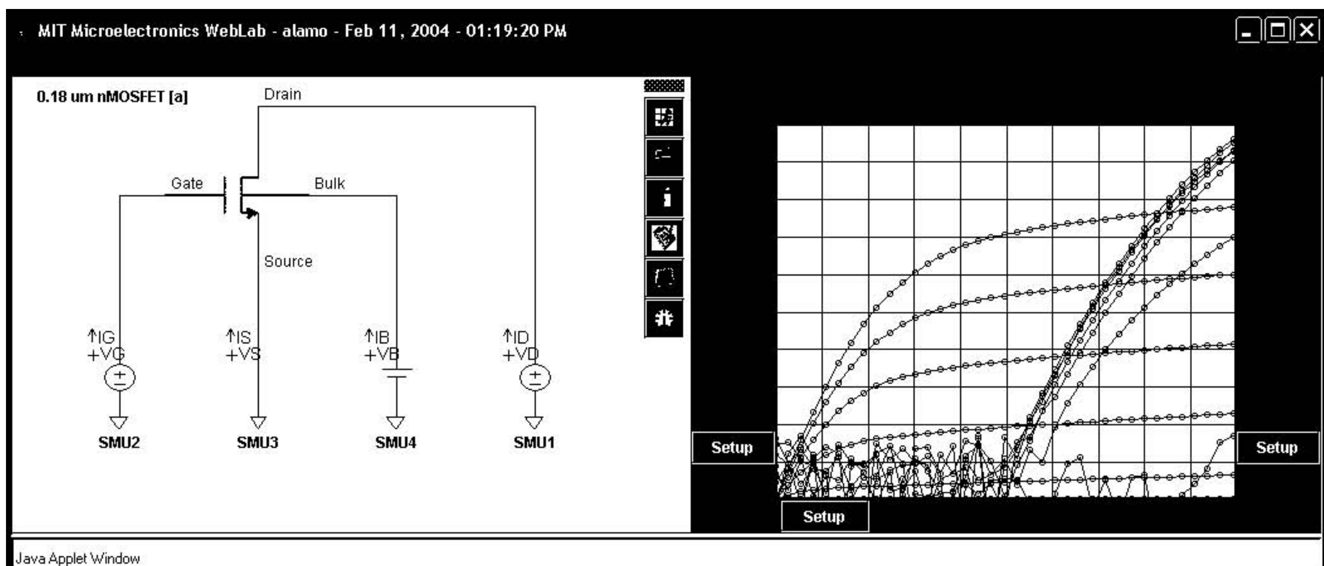
□ *Floating-body effects in SOI MOSFETs*

Output characteristics of 0.18 μm MOSFET ($V_{SB} = 0$):



Body current ($V_{SB} = 0$):



Impact ionization visible in body current

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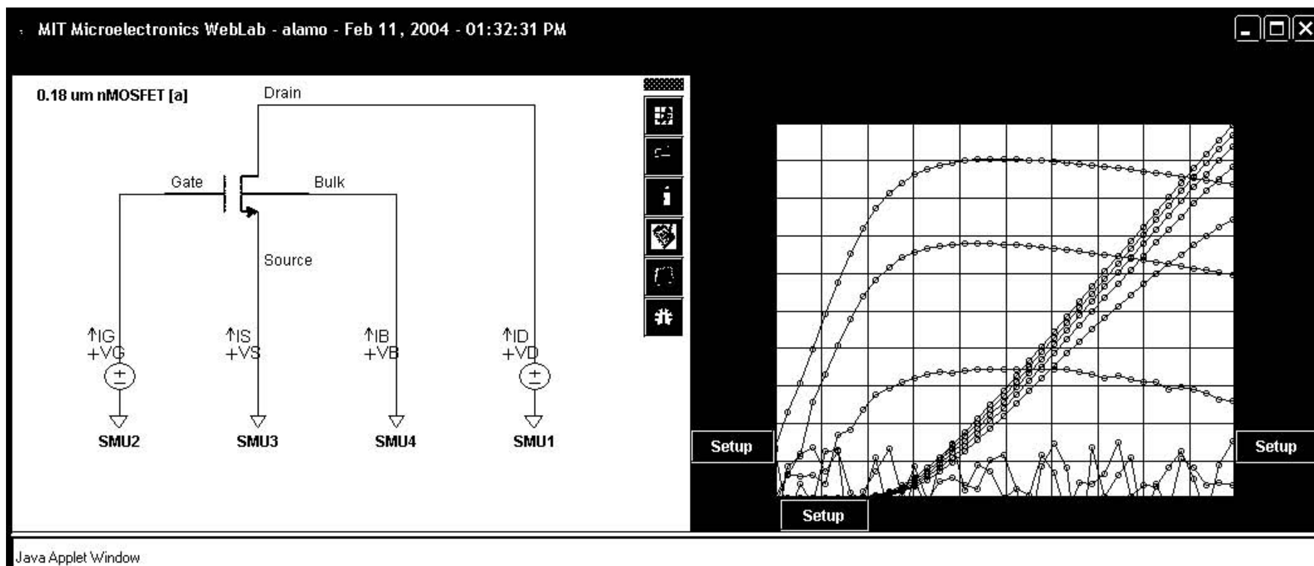
Body current ($V_{DS} = 0 - 1.8\ V$, $\Delta V_{DS} = 0.3\ V$, $V_{SB} = 0$):



Impact ionization strongly depends on V_{DS}

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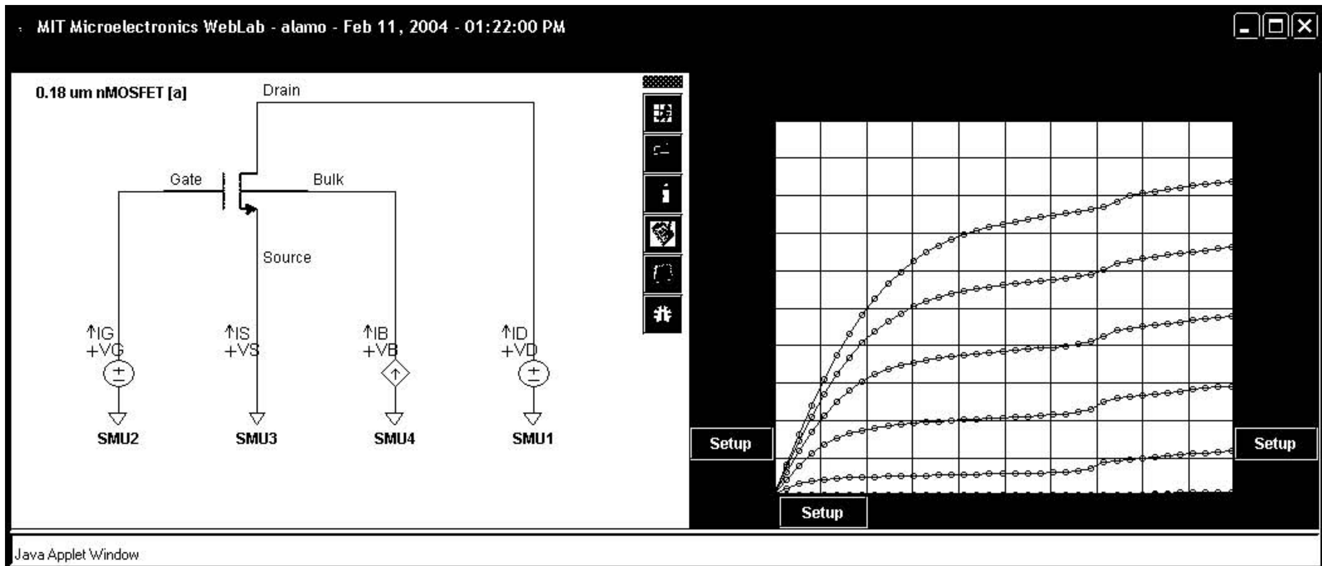
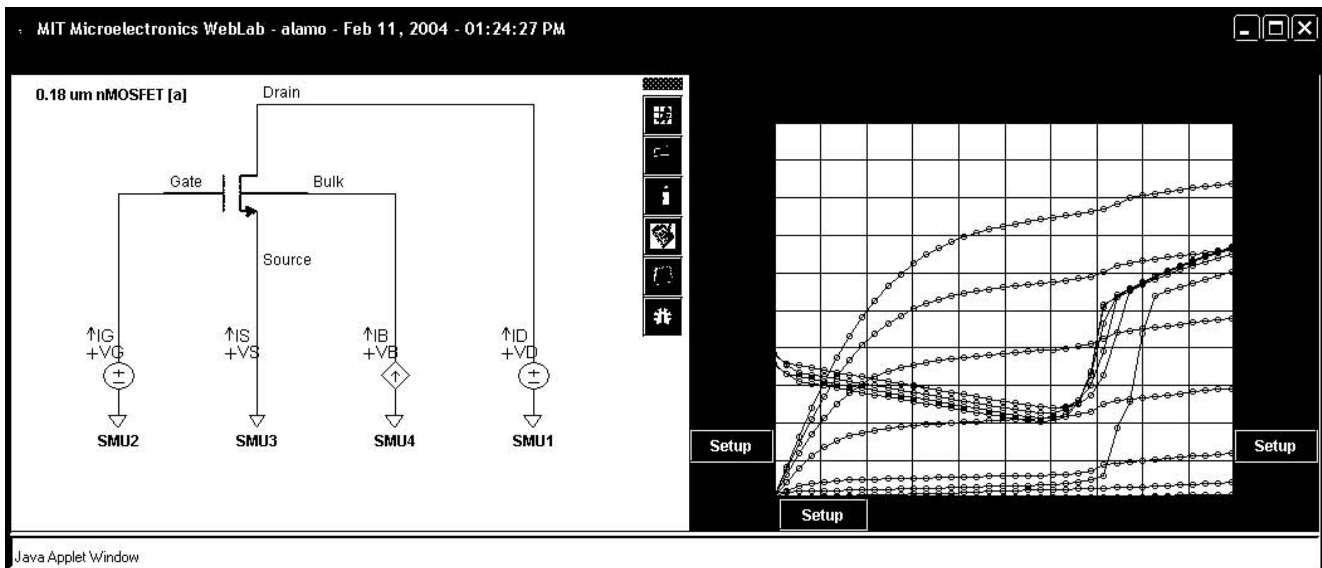
Output characteristics of 0.18 μm MOSFET with floating body ($I_B = 0$):



Body voltage ($I_B = 0$):



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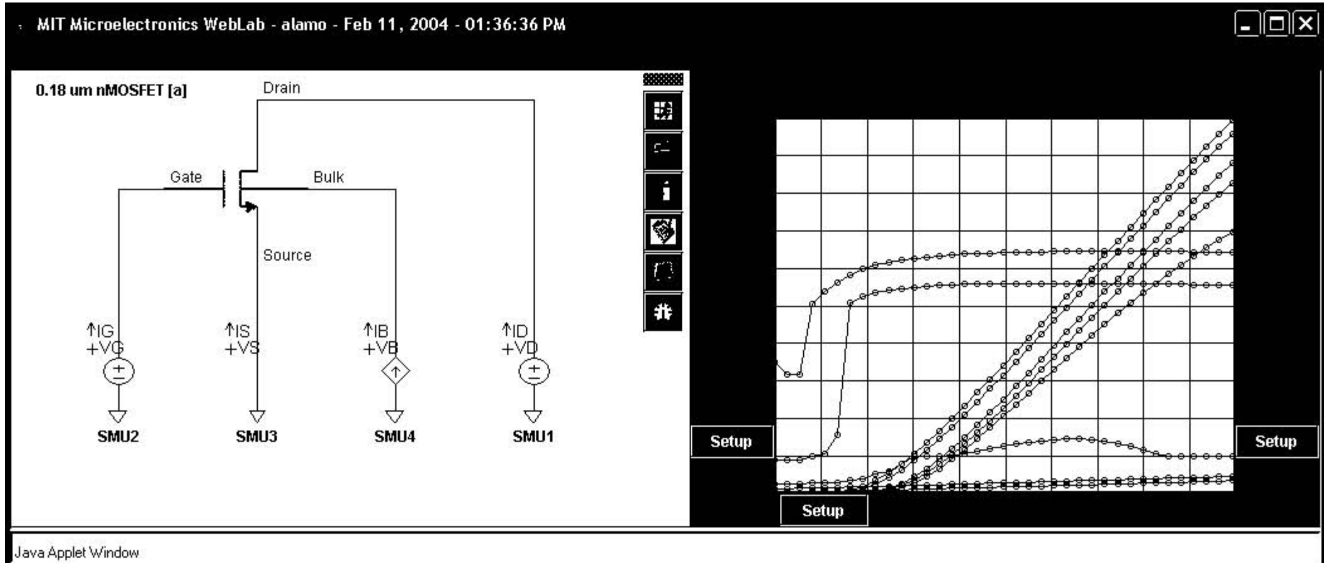
Body voltage ($V_{DS} = 0 - 1.8\ V$, $\Delta V_{DS} = 0.3\ V$, $I_B = 0$):



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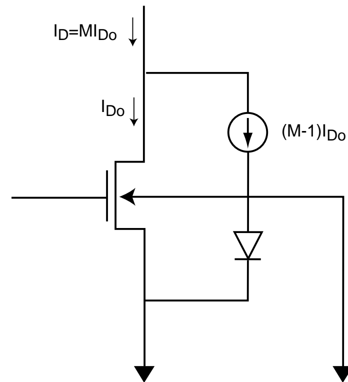
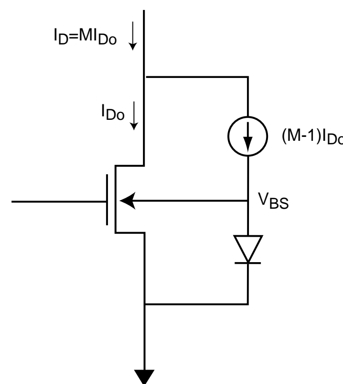
In SOI MOSFET, there is no body contact ⇒ body floating ⇒ impact ionization at high V_{DS} forward biases body-source junction





Floating body is a problem in SOI:

- "kink" in the output characteristics
- threshold voltage shifts dynamically (results in overdrive during switching that speeds up logic circuits)
- complex timing and switching simulations
- potential from premature breakdown

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Other bipolar effects in MOSFETs:

- Can't implement floating pn diodes in CMOS process
- Breakdown and snap-back (bipolar-induced breakdown)

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Key conclusions

- *Megatrends* of BJT development:
  footprint $\downarrow$, vertical dimensions $\downarrow$, $J_C \uparrow$, $f \uparrow$, $\tau \downarrow$, $BV \downarrow$.
- Bipolar effects pervasive in any device with multiple n and p regions.
- CMOS latch-up interaction of parasitic npn and pnp BJTs; can lead to device destruction.
- Floating body in SOI-MOSFETs improves performance but makes modeling much harder

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