Lecture 31 - The "Short" Metal-Oxide-Semiconductor Field-Effect Transistor *(cont.)*

April 25, 2007

Contents:

1. Short-channel effects *(cont.)*

Reading assignment:

P. K. Ko, "*Approaches to Scaling.*"

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Key questions

- Why does the threshold voltage seem to depend on the gate length of a MOSFET?
- Why does the threshold voltage of a MOSFET seem to depend on V_{DS}?

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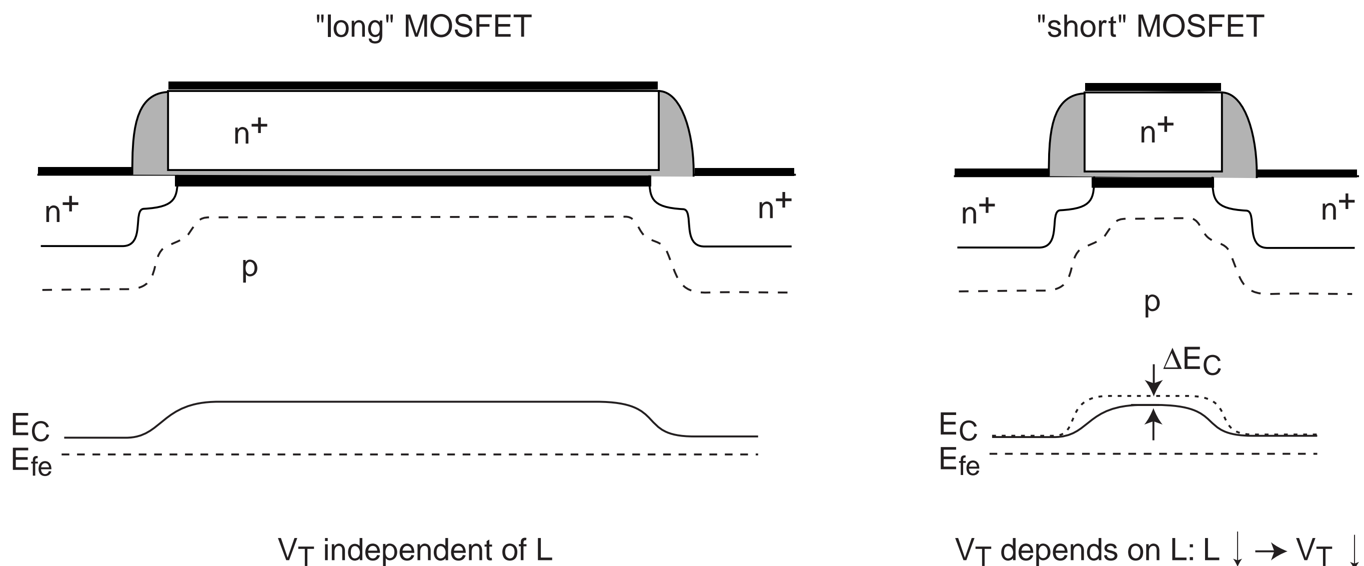
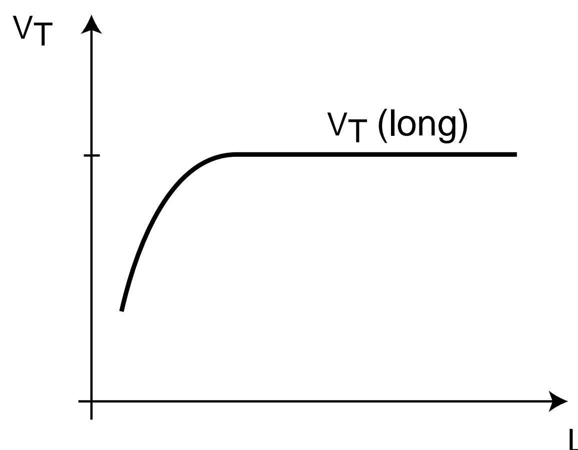
1. Short-channel effects *(cont.)*

□ V_T dependence on L

Ideally, V_T does not depend on L, it only depends on x_{ox} and N_A.

If L is short enough, depletion regions of source and drain start overlapping underneath channel.





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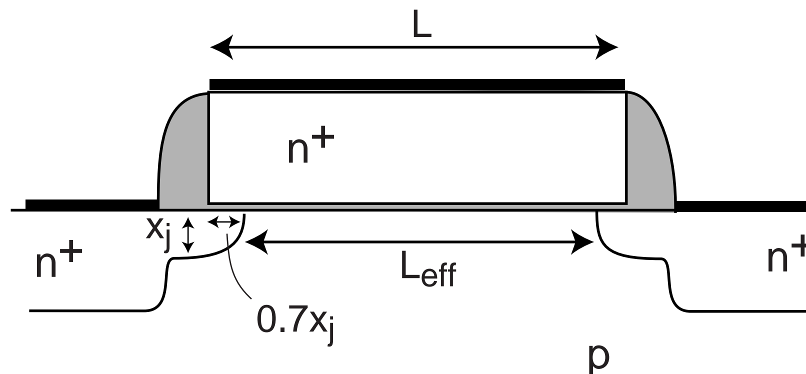
Complex 2D electrostatic problem:

- ΔV_T depends on the relative strength of the lateral electrostatics vs. the transversal electrostatics (*"electrostatic integrity"*).
- The tighter the gate controls ϕ_s, the weaker ΔV_T dependence on L.

Key dependencies:

- $x_{ox} \downarrow \Rightarrow |\Delta V_T| \downarrow$
- $N_A \uparrow \Rightarrow |\Delta V_T| \downarrow$
- $x_j \downarrow \Rightarrow L_{eff} = L - 2 \times 0.7\, x_j \uparrow \Rightarrow |\Delta V_T| \downarrow$



This is bad! long MOSFET: $V_T = f(x_{ox}, N_A)$

short MOSFET: $V_T = f(x_{ox}, N_A, L, x_j)$

Most important consequence: V_T harder to control in manufacturing environment.

V_T model in next section.

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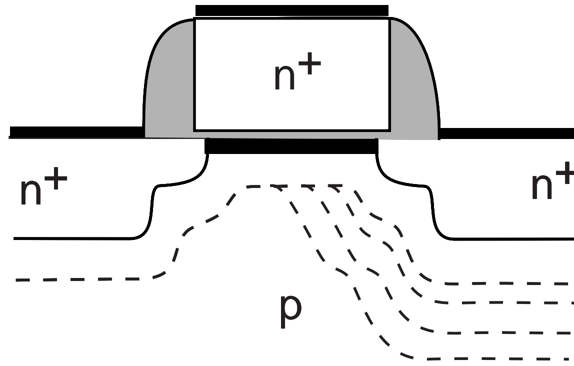
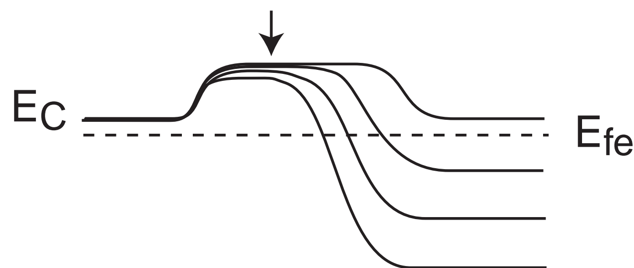
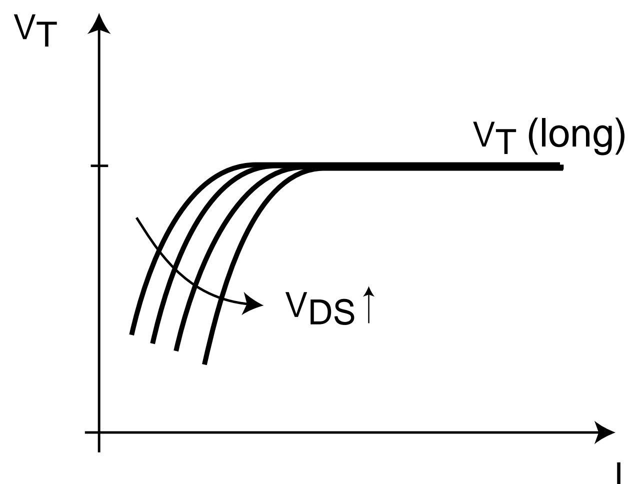
□ Drain-induced barrier lowering (DIBL)

Depletion region associated with drain junction expands as $V_{DS} \uparrow \Rightarrow$ additional V_T shift.







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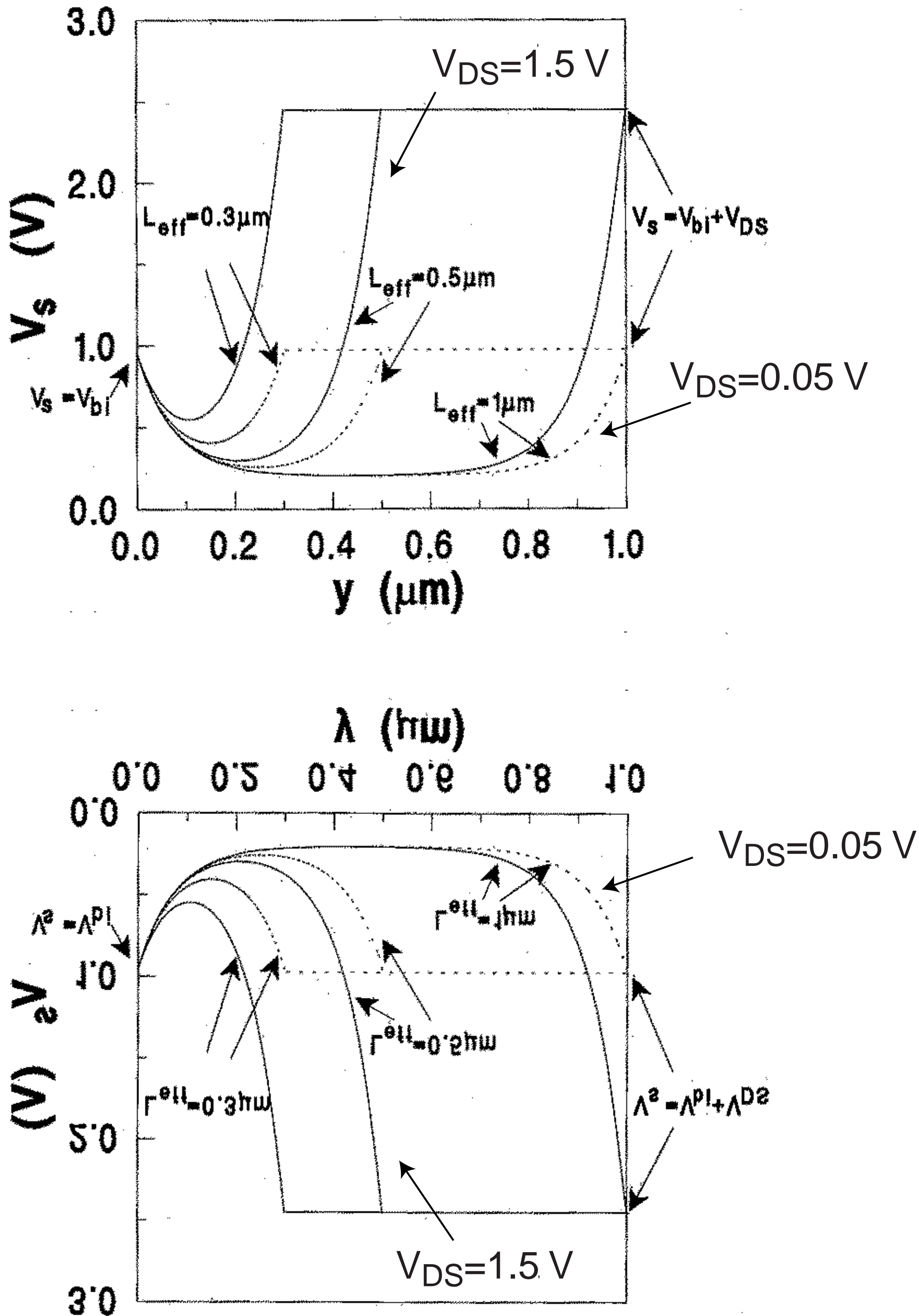

Liu, Z.-H., C. Hu, J.-H. Huang, T.-Y. Chan, M.-C. Jeng, P. K. Ko, and Y. C. Cheng. "Threshold Voltage Model for Deep-Submicrometer MOSFET's." *IEEE Transcations on Electron Devices* 40, no. 1 (1993): 86-95. Copyright 1993 IEEE. Used with permission.

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Simple analytical approximation to ΔV_T [Liu et al., TED 40, 86 (1993)]:

$$\Delta V_T = [3(\phi_{bi} - \phi_{sth}) + V_{DS}]e^{-L_{eff}/\lambda} + 2\sqrt{(\phi_{bi} - \phi_{sth})(\phi_{bi} - \phi_{sth} + V_{DS})}e^{-L_{eff}/2\lambda}$$

with characteristic length:

$$\lambda = \sqrt{\frac{\epsilon_s}{\epsilon_{ox}} x_{ox} x_{dmax}}$$

and

$$L_{eff} = L - 2 \times 0.7\, x_j$$

Quantification of DIBL:

$$DIBL = |\frac{V_T(V_{DS} = V_{DD}) - V_T(V_{DS} = 0.1\ V)}{V_{DD} - 0.1}| \ \ mV/V$$

for a certain L device.

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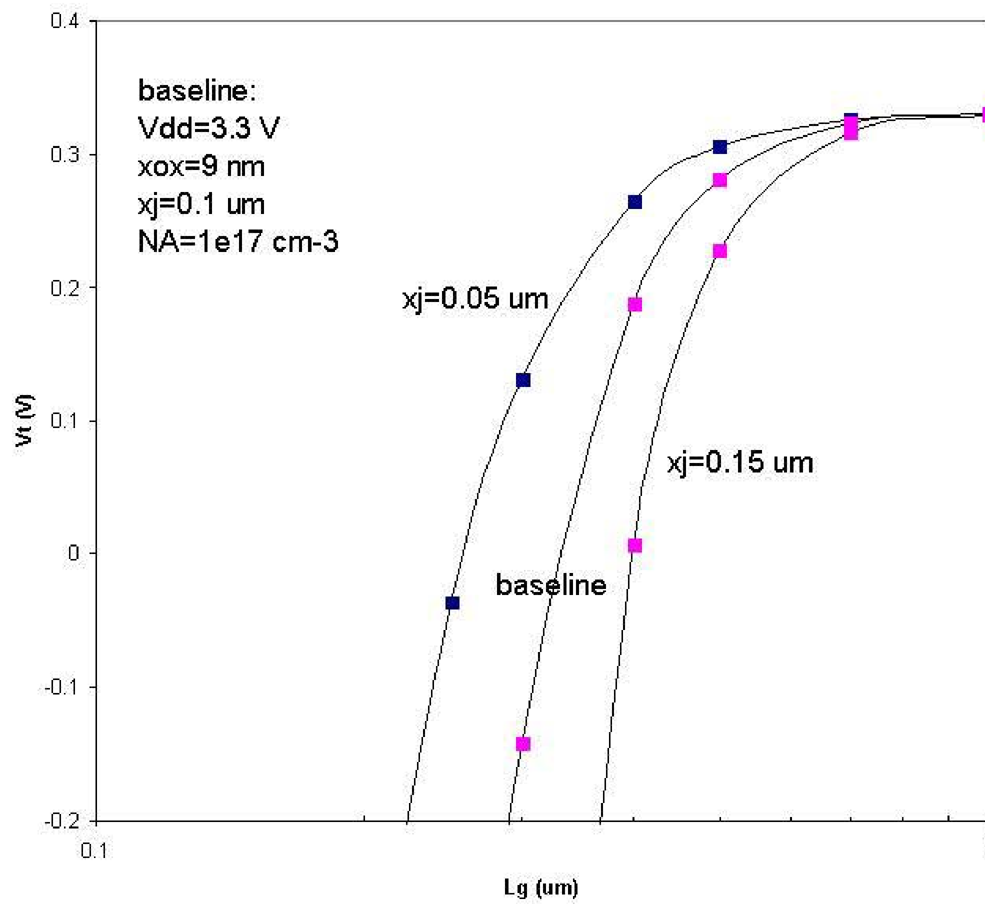

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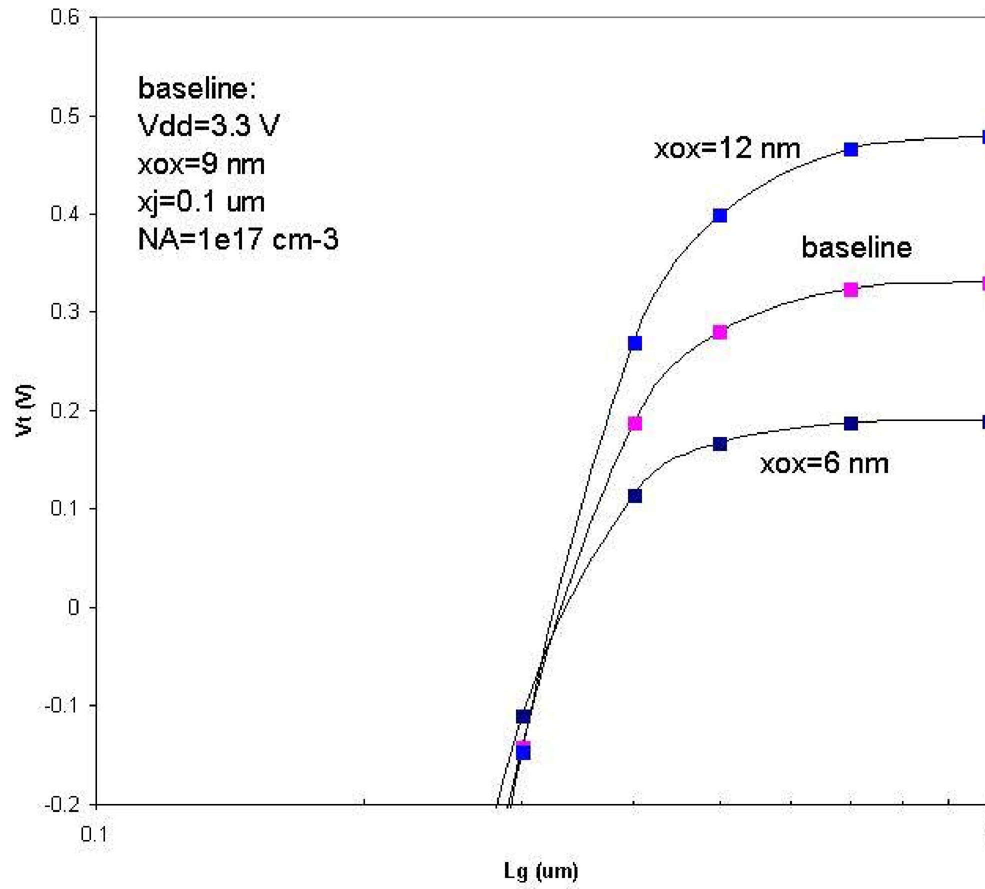

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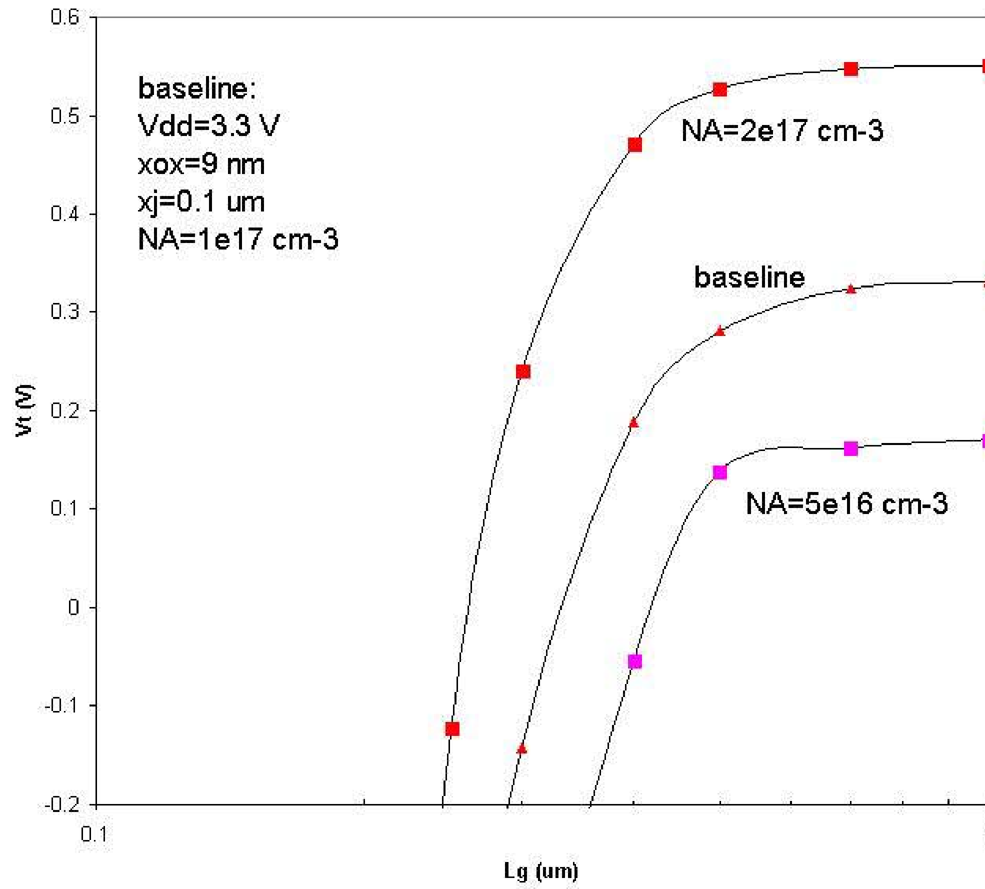

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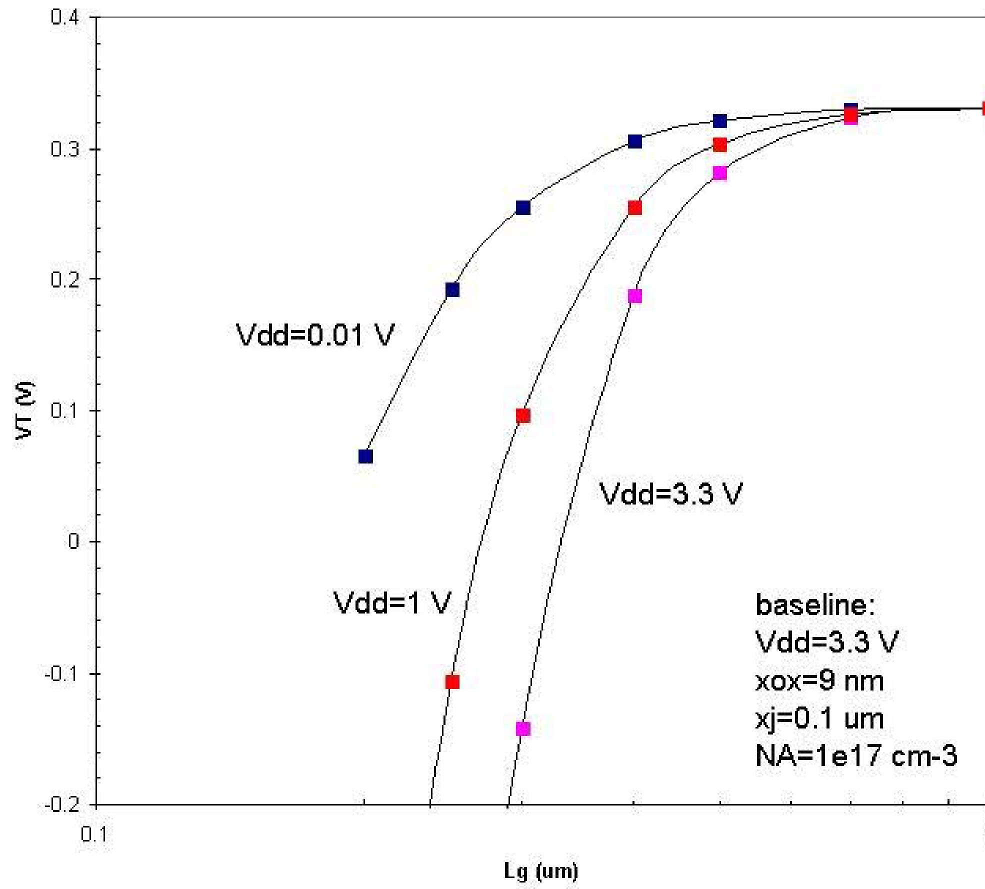

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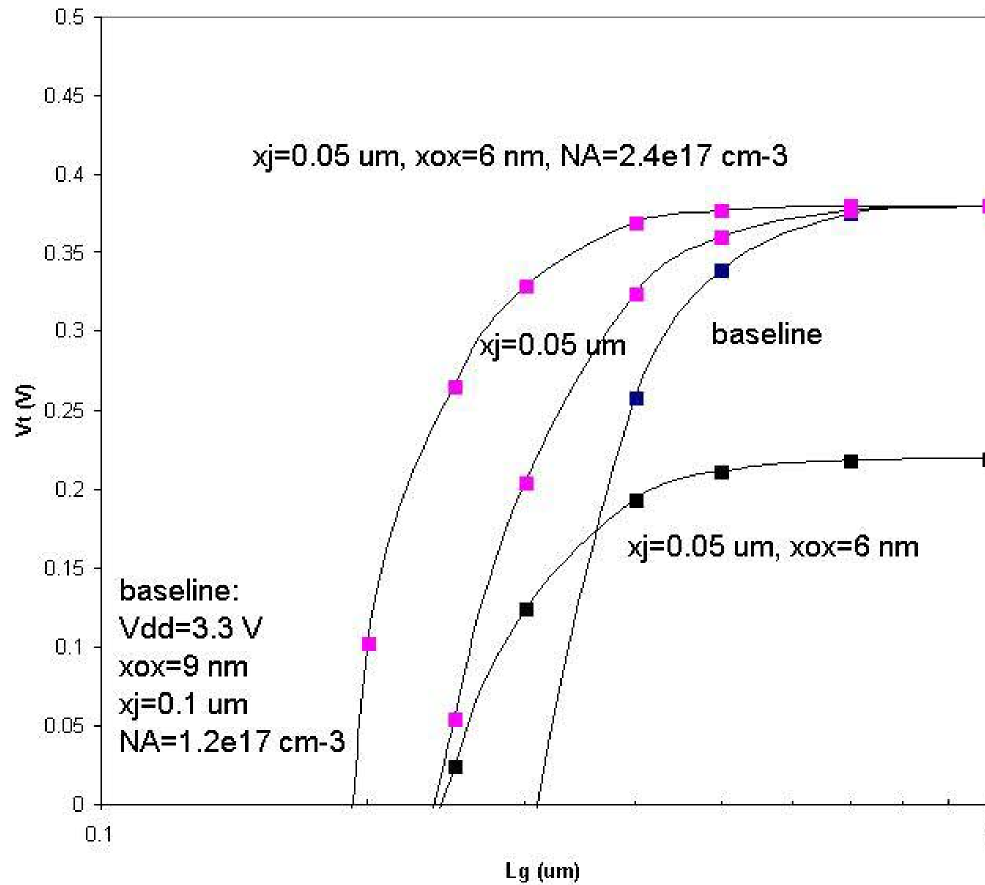

MOSFET design approach to manage DIBL:

1. shallower S/D junctions: $x_j = 0.1\ \mu m \rightarrow 0.05\ \mu m$
2. thinner gate oxide: $x_{ox} = 9\ nm \rightarrow 6\ nm$
3. increased body doping: $N_A = 1.2 \times 10^{17}\ cm^{-3} \rightarrow 2.4 \times 10^{17}\ cm^{-3}$

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Comparison of simple model with 2D simulations:

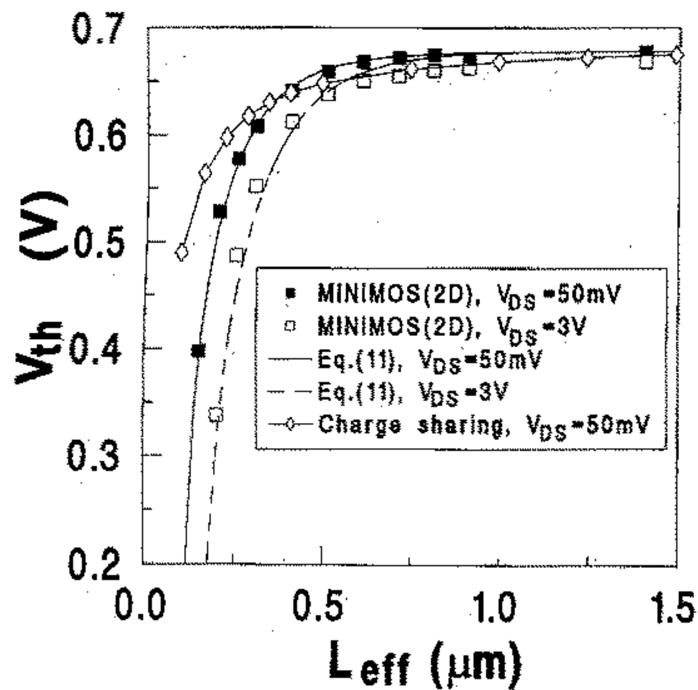

Fig. 4. A comparison of the V_{th} calculated using the charge sharing model, the two-dimensional numerical simulation (MINIMOS), and our model. The device parameters used are the same as those in Fig. 3.

Liu, Z.-H., C. Hu, J.-H. Huang, T.-Y. Chan, M.-C. Jeng, P. K. Ko, and Y. C. Cheng. "Threshold Voltage Model for Deep-Submicrometer MOSFET's." *IEEE Transcations on Electron Devices* 40, no. 1 (1993): 86-95. Copyright 1993 IEEE. Used with permission.

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Comparison of simple model with experiments:

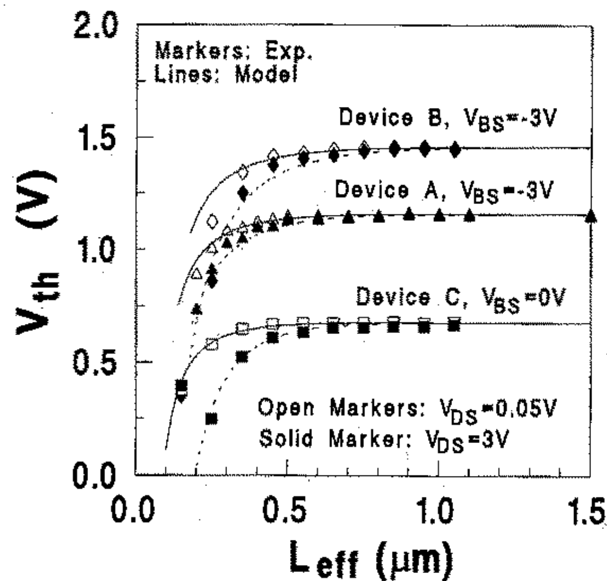

Fig. 5. Experimental and calculated threshold voltage versus effective channel length for non-LDD MOSFET's from different technologies, i.e., Device A: T_{OX} = 55 Å, $N_{SUB} = 3.6 \times 10^{17} cm^{-3}$, $X_j = 0.25$ μm, $l = 0.04$ μm; Device B: T_{OX} = 86 Å, $N_{SUB} = 1.5 \times 10^{17} cm^{-3}$, $X_j = 0.2$ μm, $l = 0.05$ μm; and Device C: T_{OX} = 156 Å, $N_{SUB} = 4 \times 10^{16} cm^{-3}$, $X_j = 0.2$ μm, $l = 0.09$ μm.

Liu, Z.-H., C. Hu, J.-H. Huang, T.-Y. Chan, M.-C. Jeng, P. K. Ko, and Y. C. Cheng. "Threshold Voltage Model for Deep-Submicrometer MOSFET's." *IEEE Transcations on Electron Devices* 40, no. 1 (1993): 86-95. Copyright 1993 IEEE. Used with permission.

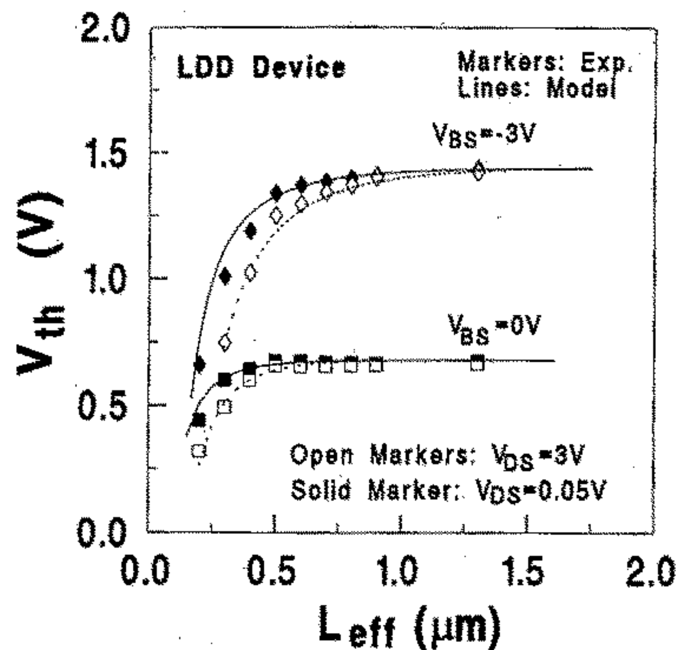

Fig. 7. Typical threshold voltage behavior for LDD device.

Liu, Z.-H., C. Hu, J.-H. Huang, T.-Y. Chan, M.-C. Jeng, P. K. Ko, and Y. C. Cheng. "Threshold Voltage Model for Deep-Submicrometer MOSFET's." *IEEE Transcations on Electron Devices* 40, no. 1 (1993): 86-95. Copyright 1993 IEEE. Used with permission.

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DIBL also affects I_{off}: $V_{DS} \uparrow \Rightarrow V_T \downarrow \Rightarrow I_{off} \uparrow$

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Shift of subthreshold curves.

Figure 5 on page 41 in
Fichtner, W., and H. W. Potzl. "MOS Modelling by Analytical Approximations." *International Journal of Electronics* 46, no. 1 (1979): 33-55.

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Key conclusions

- V_T depends on L and V_{DS}:
  - For short L, V_T depends on L: $L \downarrow \Rightarrow V_T \downarrow$.
  - *Drain-induced barrier lowering (DIBL)*: impact of V_{DS} on V_T: $V_{DS} \uparrow \Rightarrow V_T \downarrow$.
- ΔV_T reflects relative strength of lateral electrostatics vs. transveral electrostatics (*"electrostatic integrity"*).
- Electrostatic integrity improves if $x_{ox} \downarrow$, $N_A \uparrow$, $L \uparrow$, $x_j \downarrow$.
- DIBL problematic because:
  - V_T hard to control
  - $I_{off} \uparrow$

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