Lecture 29 - The "Long" Metal-Oxide-Semiconductor Field-Effect Transistor *(cont.)*

April 20, 2007

Contents:

1. Non-ideal and second-order effects *(cont.)*

Reading assignment:

del Alamo, Ch. 9, §9.7.3, 9.7.4

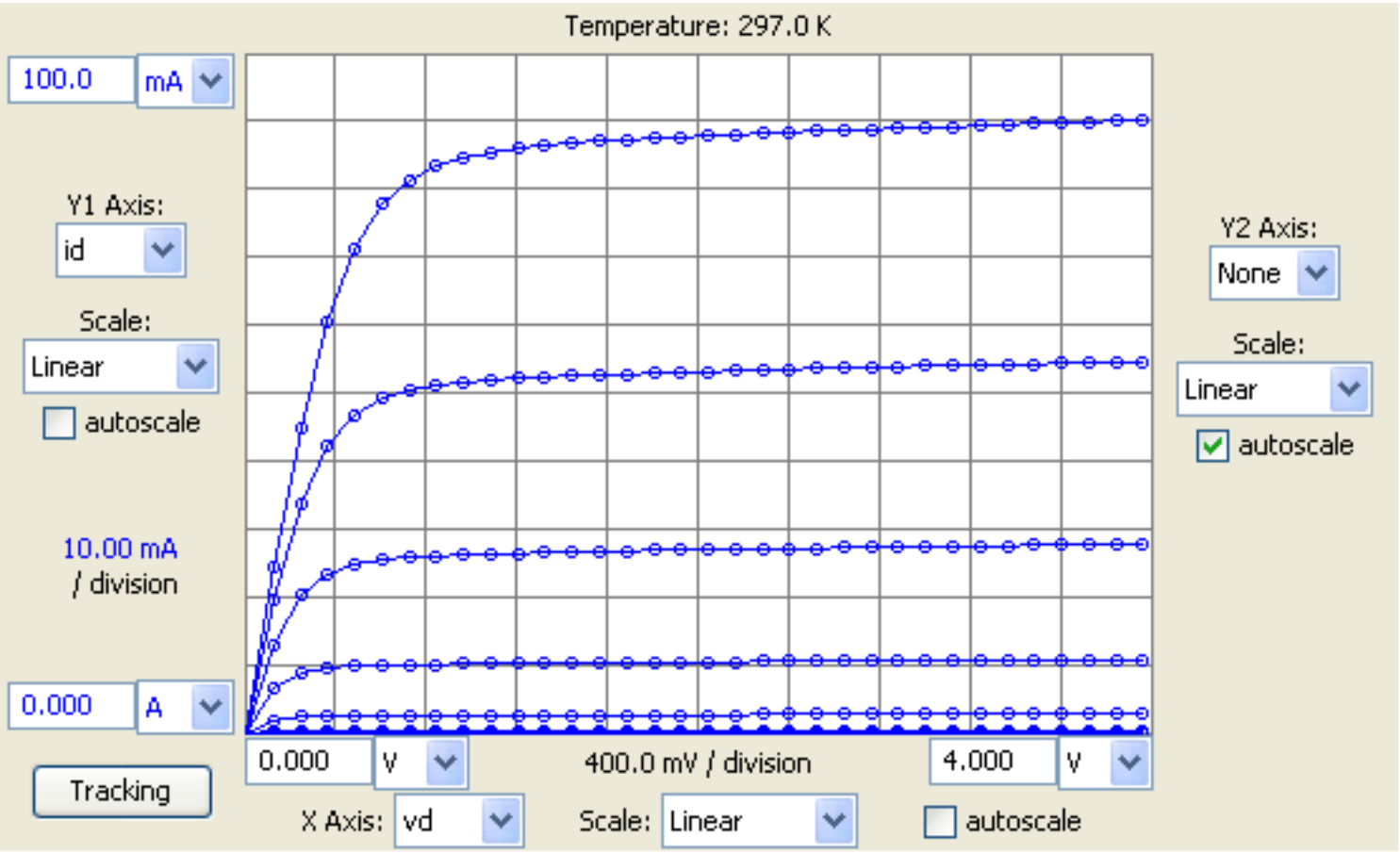
Key questions

- The MOSFET current in the saturation regime is not perfectly saturated. Why?
- What are the key dependencies of the output conductance?
- What is the physics of carrier transport in the subthreshold regime?
- What are the key dependencies of the subthreshold current?
- Why is the subthreshold current important?

1. Second-order and non-ideal effects in MOSFET *(cont.)*

□ Channel length modulation

Output characteristics of n-MOSFET (2N7000):



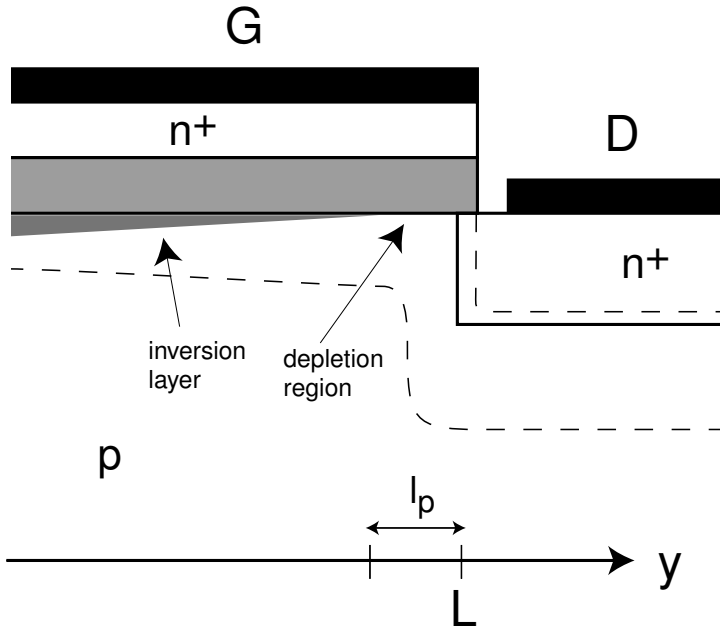
Note:

- small but distinct slope in $I_D - V_{DS}$ characteristics in saturation regime
- slope increases with V_{GS}

Origin is channel length modulation:

To first order, in saturation, V_{DS} no longer controls the electrostatics of the channel $\Rightarrow$ I_D saturates with further increases in V_{DS}

However, increases in V_{DS} beyond V_{DSsat} must be accommodated somehow $\Rightarrow$ depletion region opens up at drain-end of channel:

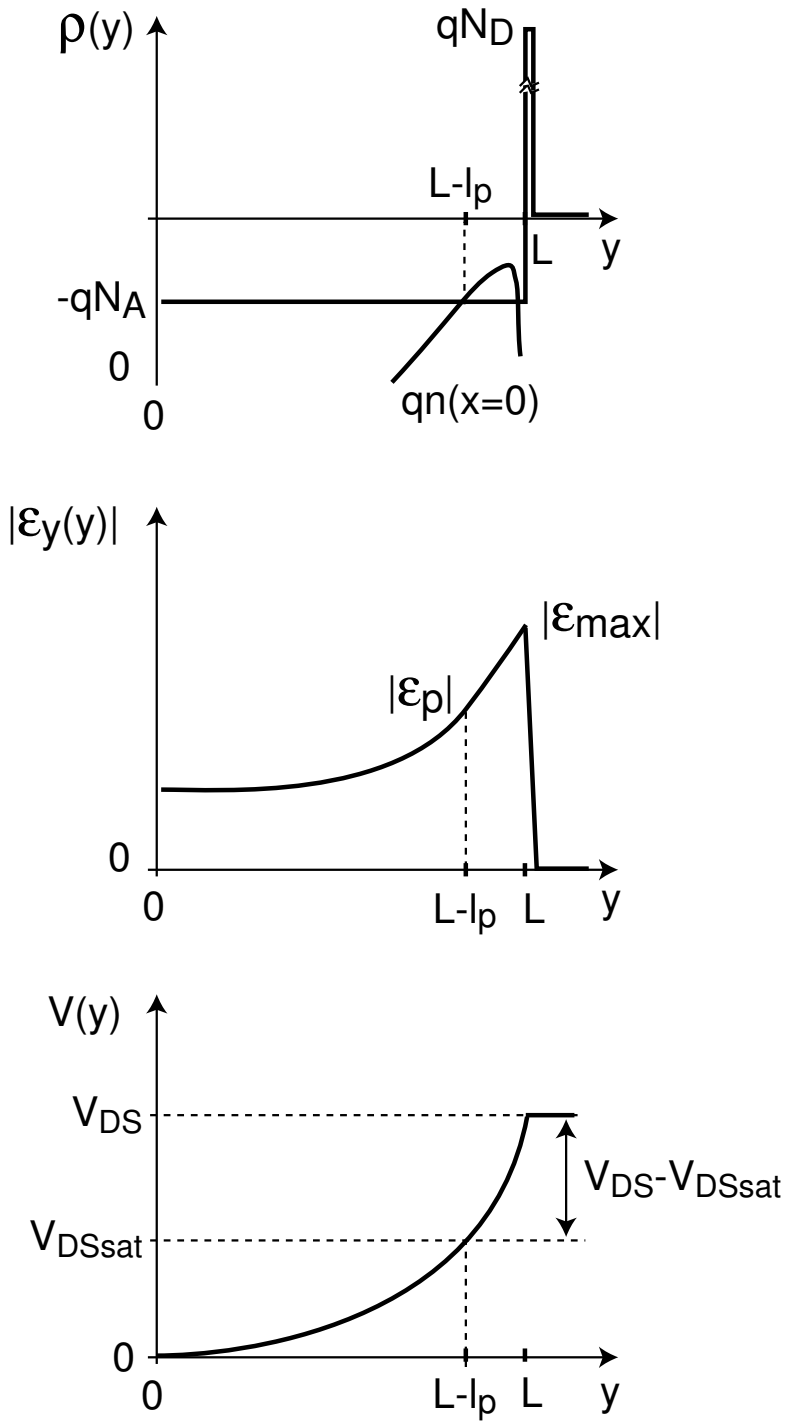


As $V_{DS} - V_{DSsat} \uparrow$:

$\Rightarrow$ *effective* channel length shortens: $L \rightarrow L - l_p$

$\Rightarrow$ lateral field in channel $\uparrow$ $\Rightarrow$ $I_D \uparrow$: imperfect saturation

Lateral electrostatics in pinch-off region:



To model Channel Length Modulation, need model for l_p vs. V_{DS}.

Main result (see details in notes):

$$l_p \simeq \frac{V_{DS} - V_{DSsat}}{|\mathcal{E}_p|}$$

where $\mathcal{E}_p$ is peak field at the pinch-off point:

$$|\mathcal{E}_p| \simeq \frac{q}{kT}\frac{V_{DSsat}}{2L}$$

Note key dependencies:

- At pinchoff, when $V_{DS} = V_{DSsat}$, $l_p = 0$
- l_p linear on $V_{DS} - V_{DSsat}$
- $l_p \sim L$

Impact on I_D

Since:

$$I_{Dsat} \propto \frac{1}{L}$$

Then, channel length modulation implies:

$$I_{Dsat} \propto \frac{1}{L - l_p} = \frac{1}{L(1 - \frac{l_p}{L})} \simeq \frac{1}{L}(1 + \frac{l_p}{L}) = \frac{1}{L}(1 + \frac{V_{DS} - V_{DSsat}}{|\mathcal{E}_p|L})$$

Assumed that in well designed device $l_p \ll L$

Define λ as *Channel Length Modulation Parameter* (units V^{-1}):

$$\lambda = \frac{1}{|\mathcal{E}_p|L}$$

Then:

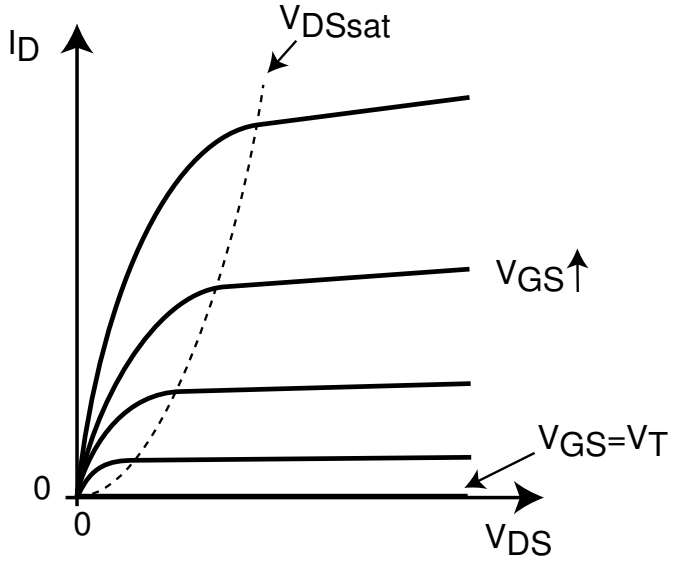
$$I_{Dsat} \simeq \frac{W}{2L}\mu_e C_{ox}(V_{GS} - V_T)^2[1 + \lambda(V_{DS} - V_{DSsat})]$$

λ is a parameter characteristic of the technology

$$I_{Dsat} \simeq \frac{W}{2L}\mu_e C_{ox}(V_{GS} - V_T)^2[1 + \lambda(V_{DS} - V_{DSsat})]$$

Features of new term:

- goes to zero for $V_{DS} = V_{DSsat}$
- proportional to $I_{Dsat} \Rightarrow$ slope of $I_D - V_{DS}$ characteristics increases the higher V_{GS}



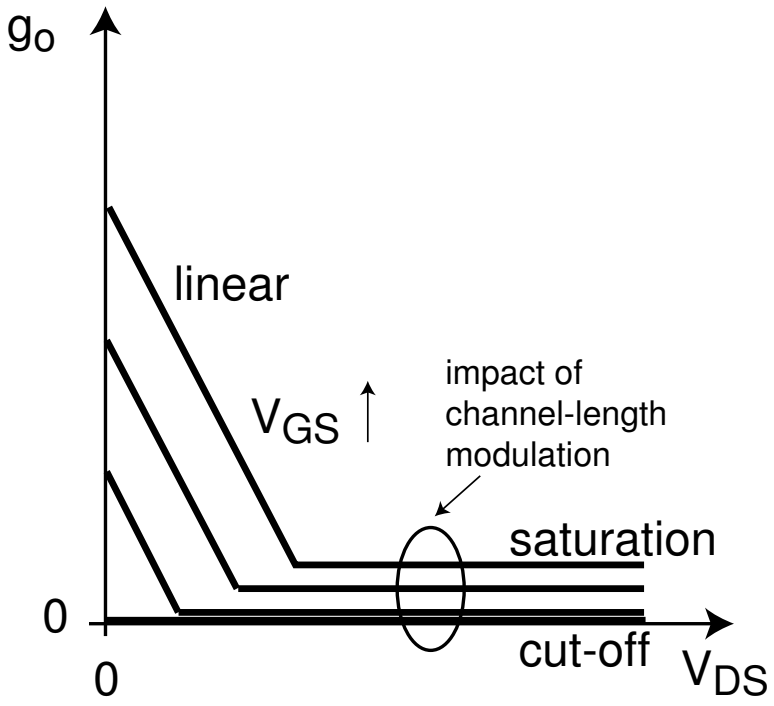
In analogy with BJT, $1/\lambda$ sometimes referred to as *Early voltage*.

Output conductance: slope in I_D in saturation regime:

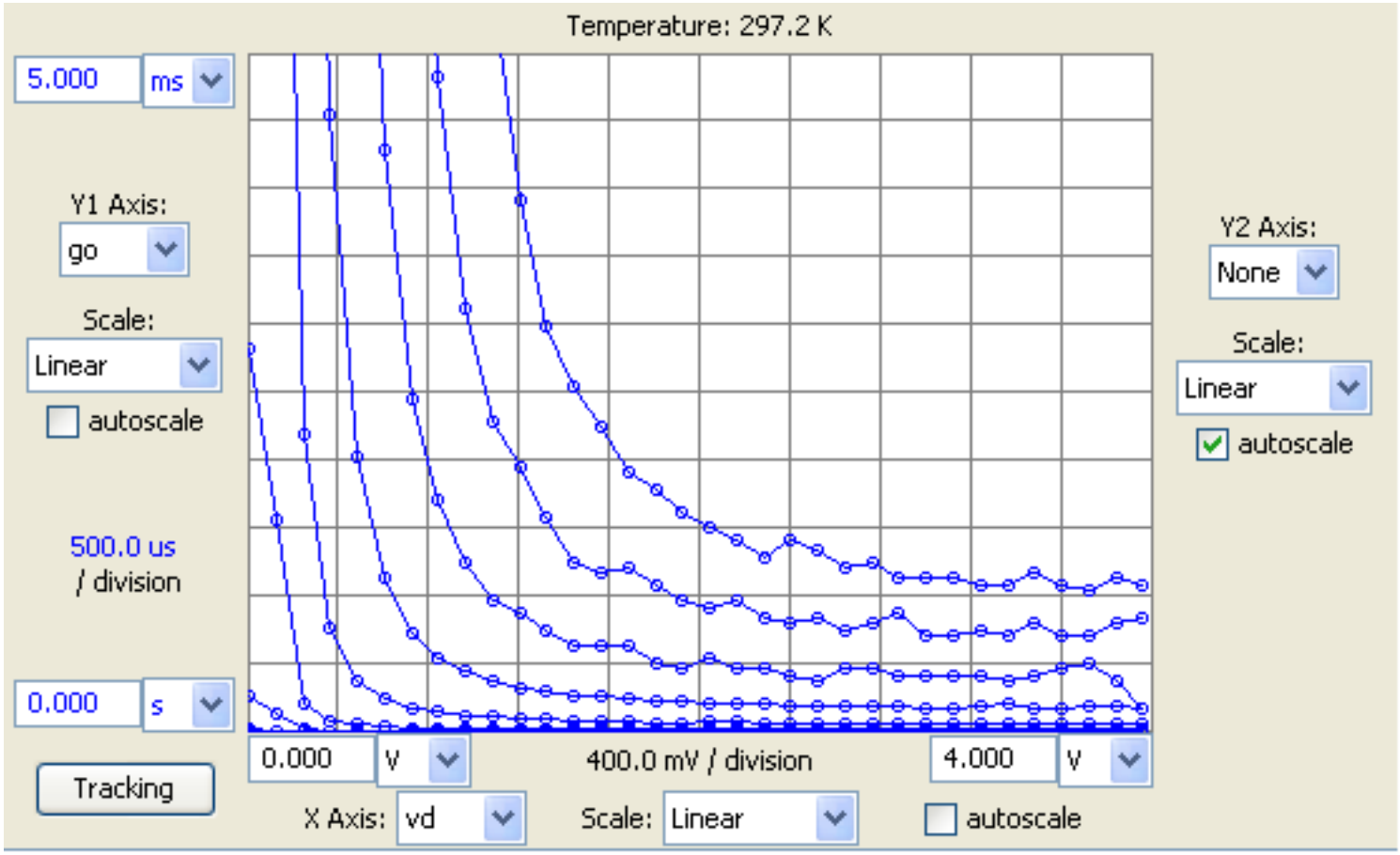
$$g_o = \frac{\partial I_{Dsat}}{\partial V_{DS}}|_{V_{GS},V_{BS}} \simeq \lambda I_{Dsat}$$

Important result: for a given technology, g_o only depends on I_{Dsat}:

$$g_o \propto I_{Dsat}$$

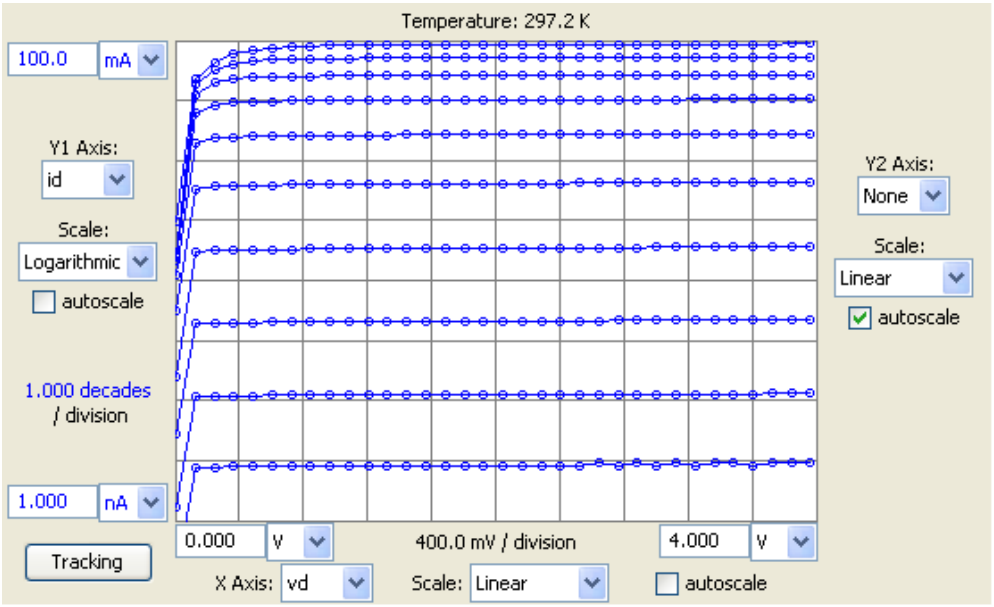


Output conductance of 2N7000 n-MOSFET:

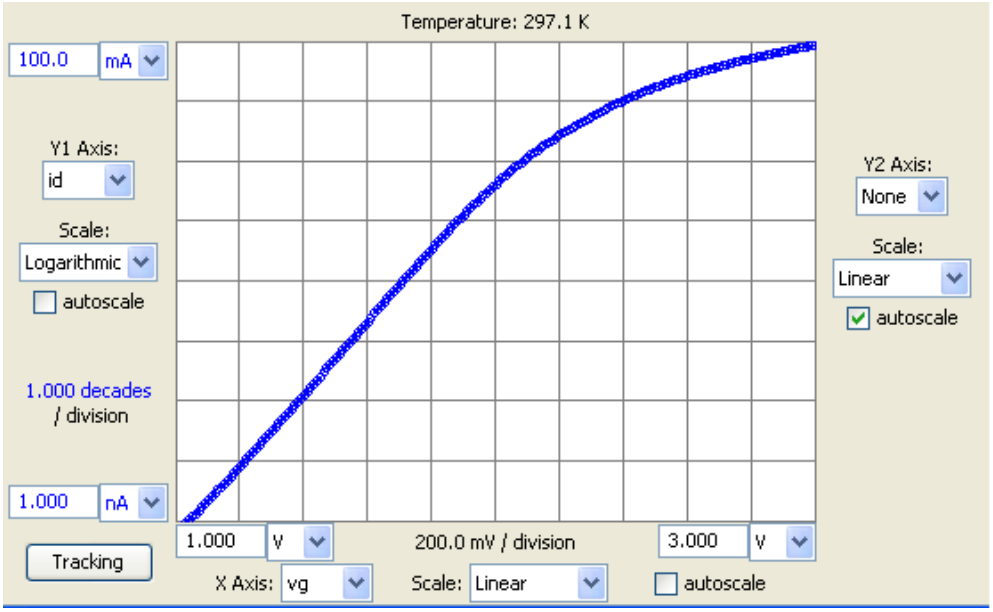


□ Subthreshold regime

Output characteristics of MOSFET in saturation in semilog scale:



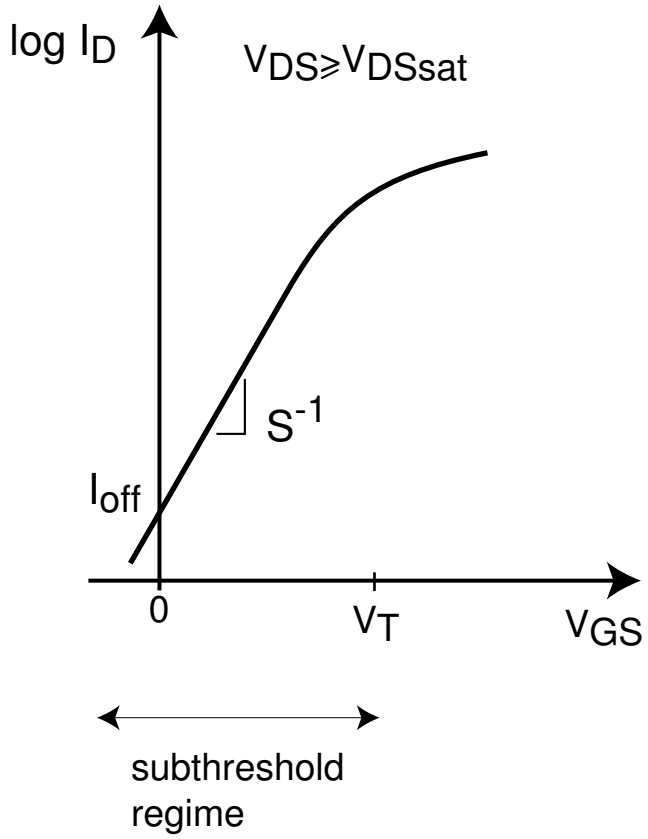
Transfer characteristics of MOSFET in saturation in semilog scale:



Experimental observations below threshold:

- I_D exponential on V_{GS}
- I_D saturated with V_{DS} down to very small values of V_{DS}

$$I_D \propto \exp \frac{q(V_{GS} - V_T)}{nkT}$$



Two key figures of merit of subthreshold regime:

• *Inverse subthreshold slope*, S: voltage required to increase I_D by 10X:

$$S = \frac{nkT}{q} ln10$$

If $n = 1$, $S = 60\ mV/dec$ at 300 K.

Want S small to shut off MOSFET quickly.

In well designed devices, $S \simeq 70 - 90\ mV/dec$ at 300 K.

• *Off current*, I_{off}:

$$I_{off} = I_D(V_{GS} = 0)$$

For logic CMOS, want I_{off} in nA range.

I_{off} set by S and V_T.

□ Subtreshold current:

MOS structure in weak inversion regime (below threshold). Inversion charge depends exponentially on V_{GS}:

$$Q_e(V) \simeq -\frac{kT}{q} C_{sth} \exp \frac{q(V - V_T)}{nkT}$$

with

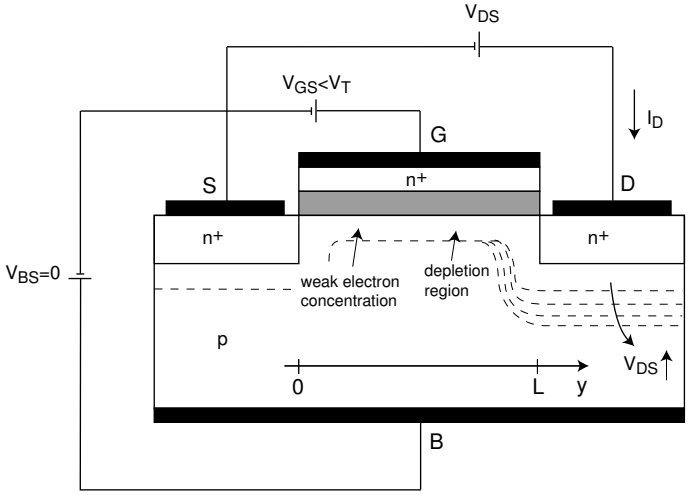
$$n = 1 + \frac{C_{sth}}{C_{ox}}$$

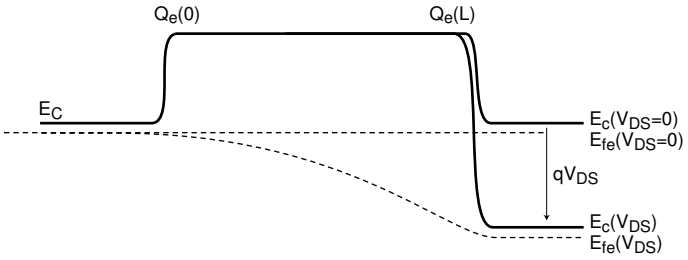
The subthreshold current shows the dependencies of Q_e in weak-inversion regime.

But, how does this charge flow from source to drain?

In weak inversion, dominant electrostatic feature is depletion region under gate ⇒ electron Fermi level in drain, does not "grab" on electron Fermi level in inversion layer (there is no inversion layer!)

Potential distribution under gate set by voltage on gate and not drain:





In subthreshold regime:

- no longitudinal field in channel
- energy band diagram looks like the base of bipolar transistor
- electrons flow from source to drain by **diffusion**

Diffusion current:

$$I_D = -WD_e\frac{dQ_e}{dy}$$

No recombination along channel $\Rightarrow$ profile is linear in y:

$$I_D = -WD_e \frac{Q_e(y=L) - Q_e(y=0)}{L}$$

- On the source side, $V = V_{GS}$:

$$Q_e(y=0) \simeq -\frac{kT}{q} C_{sth} \exp \frac{q(V_{GS} - V_T)}{nkT}$$

- On the drain side, $V = V_{GD} = V_{GS} - V_{DS}$:

$$Q_e(y=L) \simeq -\frac{kT}{q} C_{sth} \exp \frac{q(V_{GS} - V_{DS} - V_T)}{nkT}$$

All together:

$$I_D \simeq \frac{W}{L} D_e \frac{kT}{q} C_{sth} \exp \frac{q(V_{GS} - V_T)}{nkT} (1 - \exp \frac{-qV_{DS}}{nkT})$$

$$I_D \simeq \frac{W}{L} D_e \frac{kT}{q} C_{sth} \exp \frac{q(V_{GS} - V_T)}{nkT} (1 - \exp \frac{-qV_{DS}}{nkT})$$

Notice: $V_{DS} = 0 \Rightarrow I_D = 0$.

If $V_{DS} \gg \frac{kT}{q}$:

$$I_D \simeq \frac{W}{L} D_e \frac{kT}{q} C_{sth} \exp \frac{q(V_{GS} - V_T)}{nkT}$$

with:

$$n = 1 + \frac{\gamma}{2\sqrt{2\phi_f}} = 1 + \frac{C_{sth}}{C_{ox}}$$

Key dependencies of subthreshold slope:

- $x_{ox} \downarrow \Rightarrow C_{ox} \uparrow \Rightarrow n \downarrow \Rightarrow$ sharper subthreshold.
- $N_A \uparrow \Rightarrow C_{sth} \uparrow \Rightarrow n \uparrow \Rightarrow$ softer subthreshold.
- $V_{SB} \uparrow \Rightarrow C_{sth} \downarrow \Rightarrow n \downarrow \Rightarrow$ sharper subthreshold.
- $T \uparrow \Rightarrow$ softer subthreshold.

n reflects electrostatic competition between top gate and body ("bottom gate")

- Effect of N_A:

Figure removed due to copyright restrictions.

Yang, Edward S. *Microelectronic Devices*. New York, NY: McGraw-Hill, 1988, p. 268. ISBN: 9780070722385.

- Effect of V_{SB}:

Figure removed due to copyright restrictions.

Sze, S. M. *Physics of Semiconductor Devices*. 2nd ed. New York, NY: Wiley, 1981, p. 448. ISBN: 9780471056614.

- Effect of T:

Figure removed due to copyright restrictions.

Sze, S. M. *Physics of Semiconductor Devices*. 2nd ed. New York, NY: Wiley, 1981, p. 453. ISBN: 9780471056614.

□ Subthreshold regime important because it determines *off current*, I_{off}:

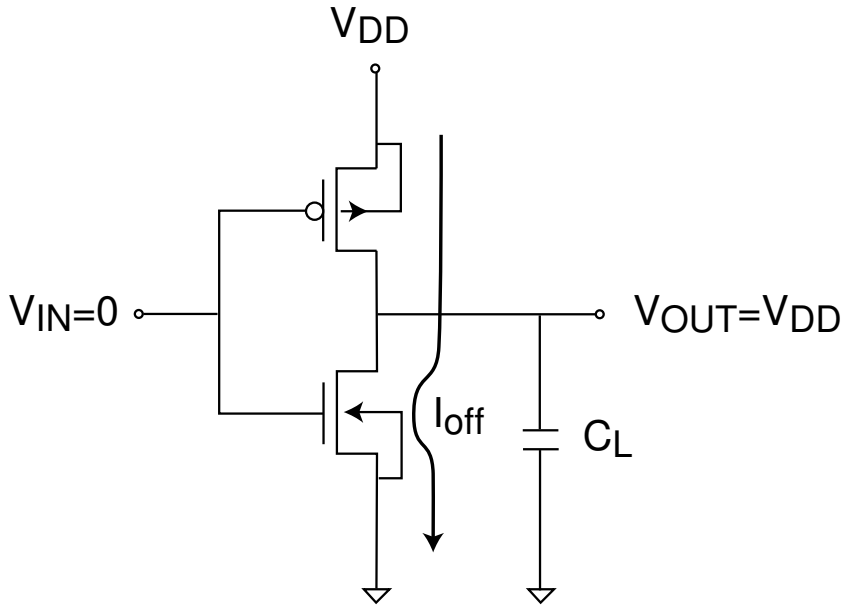
$$I_{off} = I_D(V_{GS} = 0, V_{DS} = V_{DD}) \simeq \frac{W}{L} D_e \frac{kT}{q} C_{sth} \exp \frac{-qV_T}{nkT}$$

To get $I_{off} \downarrow$:

- $L \uparrow \Rightarrow$ performance $\downarrow$
- $V_T \uparrow \Rightarrow$ performance $\downarrow$
- $n \downarrow \Rightarrow N_A \downarrow \Rightarrow$ "short-channel" effects $\uparrow$
  $\Rightarrow x_{ox} \downarrow \Rightarrow$ field in oxide $\uparrow$

I_{off}: key goal in logic device design

I_{off} important because it contributes to DC power dissipation in CMOS:



$$W_{off} = I_{off} V_{DD}$$

Example:

$I_{off} = 100\ pA/\mu m$, $W = 5\ \mu m$, $V_{DD} = 3.3\ V \Rightarrow W_{off} = 1.7\ nW$.

If 10^7 transistors $\Rightarrow\ W_{off} = 17\ mW$.

I_{off} thermally activated: $T \uparrow \Rightarrow I_{off} \uparrow\uparrow \Rightarrow W_{off} \uparrow\uparrow$.

Same example with $V_{th} = 0.7\ V$ and $S^{-1} = 75\ mV/dec$ @ 75^oC:

$$W_{off}(75^oC) = 74 \times W_{off}(25^oC) = 1.1\ W$$

Key conclusions

- *Channel length modulation*: as $V_{DS} > V_{DSsat}$, depletion region widents at drain-end of channel $\Rightarrow \;\; L \downarrow \rightarrow I_{Dsat} \uparrow$ (imperfect saturation).
- Rough model:

$$I_{Dsat} \simeq \frac{W}{2L}\mu_e C_{ox}(V_{GS} - V_T)^2[1 + \lambda(V_{DS} - V_{DSsat})]$$

- Output conductance due to channel length modulation:

$$g_o \propto I_{Dsat}$$

- *Subthreshold regime*: I_D drops off exponentially below V_T:

$$I_D \propto \exp\frac{q(V_{GS} - V_T)}{nkT}$$

- *Inverse subthreshold slope*:

$$S = (1 + \frac{C_{sth}}{C_{ox}})\frac{kT}{q}\ln 10$$

- *Off current* of CMOS, $I_D(V_{GS} = 0, V_{DD} = 0)$, set by subthreshold regime. Important for static power dissipation.