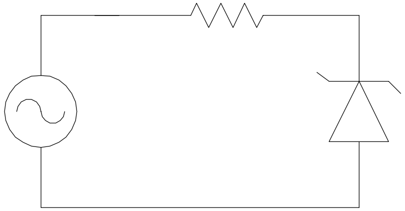
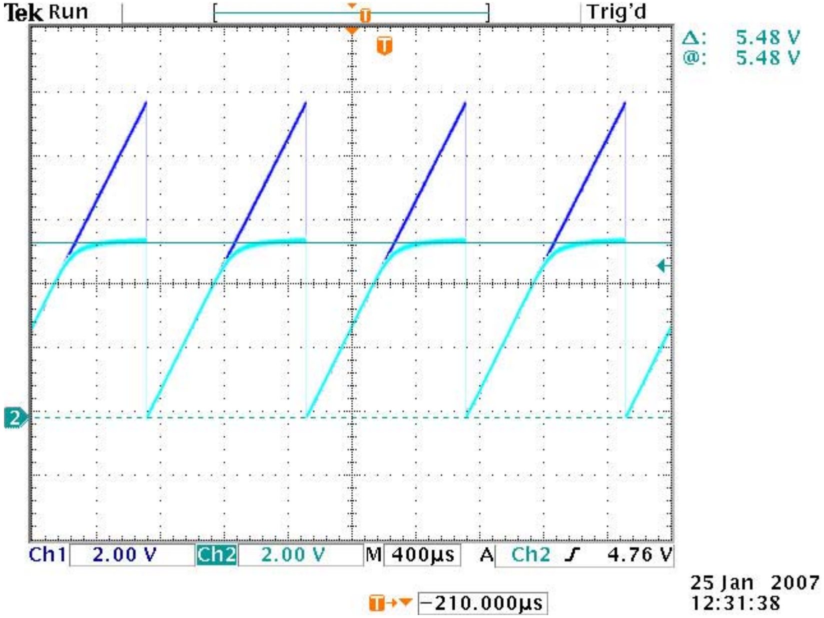
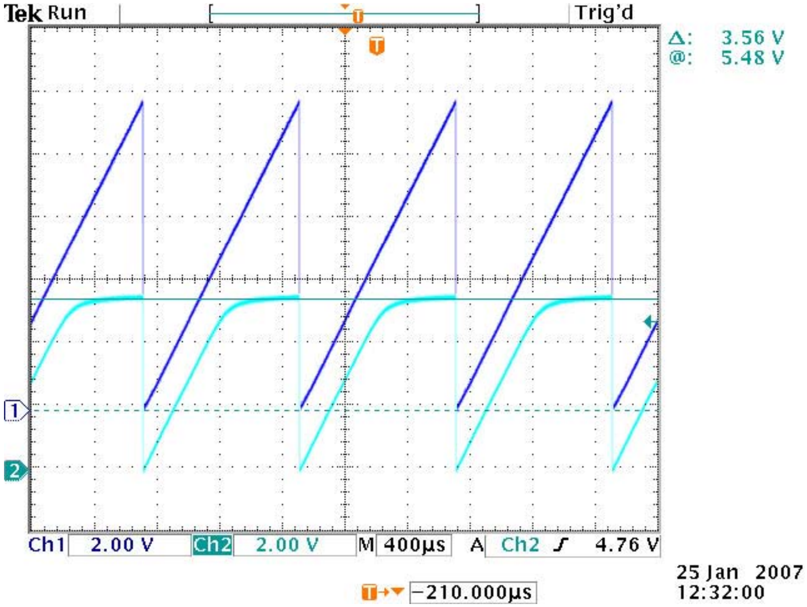
Lab 3 Revisited

- Zener diodes

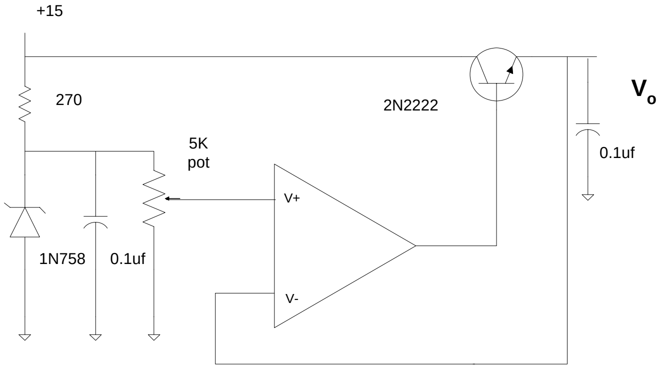


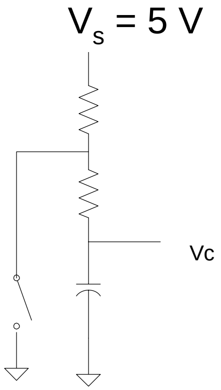




Lab 3 Revisited

- Voltage regulators
- 555 timers





$$V_c = V_s\left(1 - e^{-\frac{t}{RC}}\right)$$

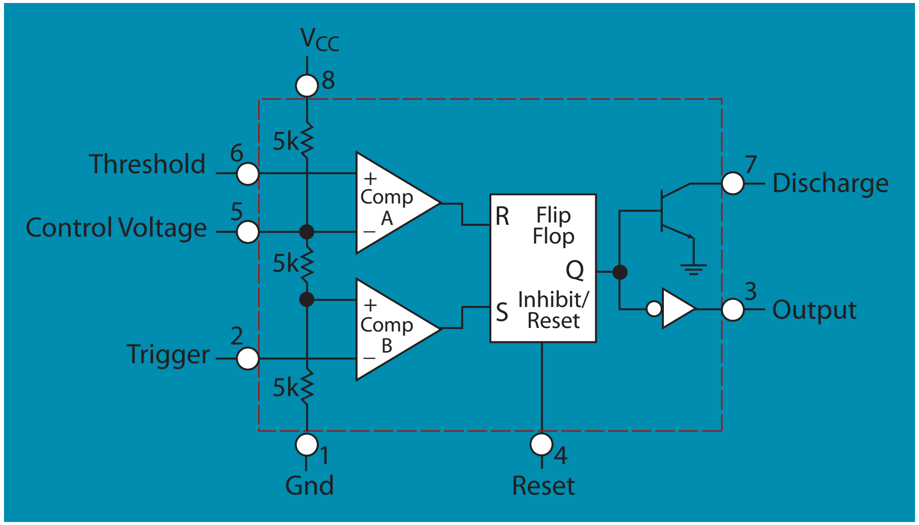
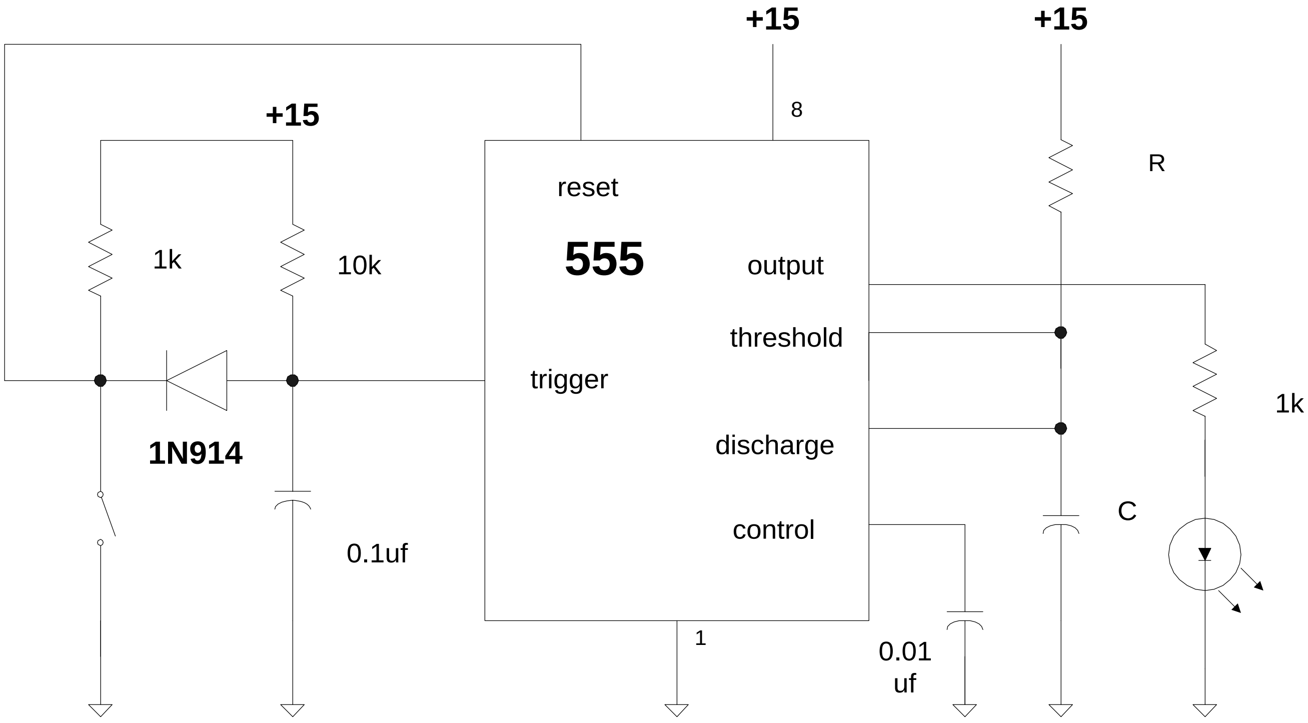


Figure by MIT OpenCourseWare.

Closet Light Timer



Digital Circuits

- Real world analog signals have noise – unavoidable.
- Digital circuits offers better noise immunity.
- Use voltage to represent “0” and “1”
  - Avoid forbidden voltage zone.
  - Make standards tighter for output than for inputs.

- Data (HCMOS family): 0 (low), 1 (high)
  - Input voltage low: **0.0 – 0.7v**
  - Input voltage high: **>2.0V**
  - Output low: **<0.4v**
  - Output high: **>3.98v**

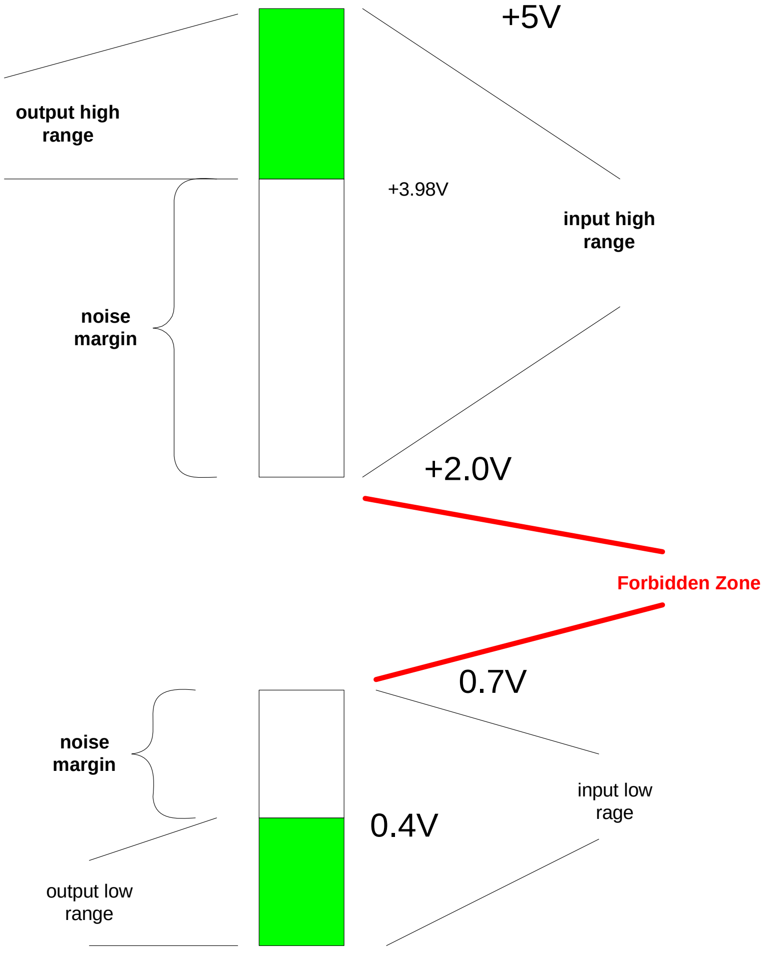
Digital Circuits

HCMOS 1 (high)

- **Output high: >3.98v**
- Input voltage high: >2.0V

HCMOS 0 (low)

- **Output low: <0.4v**
- Input voltage low: 0.0 – 0.7v

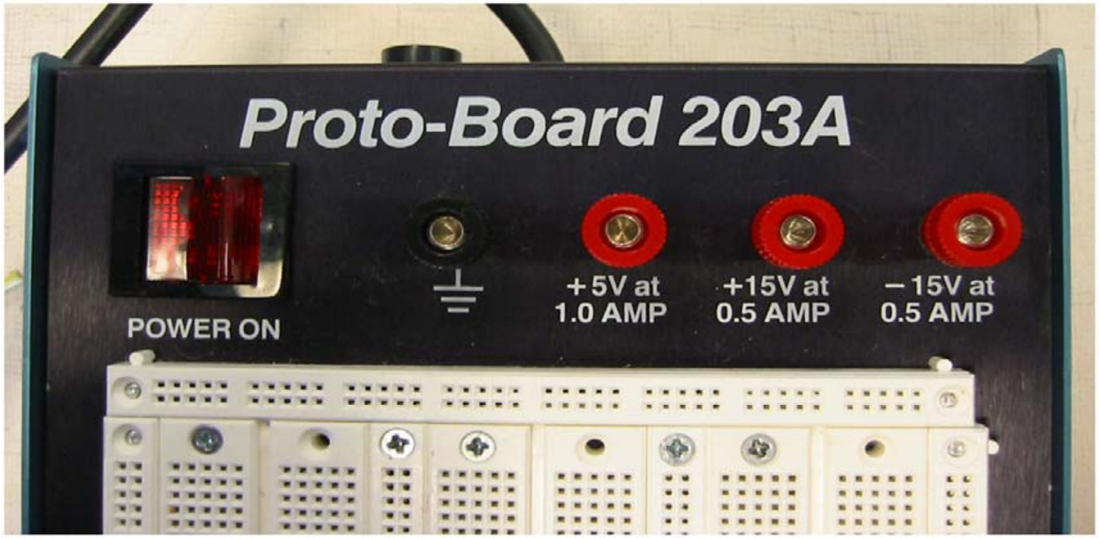


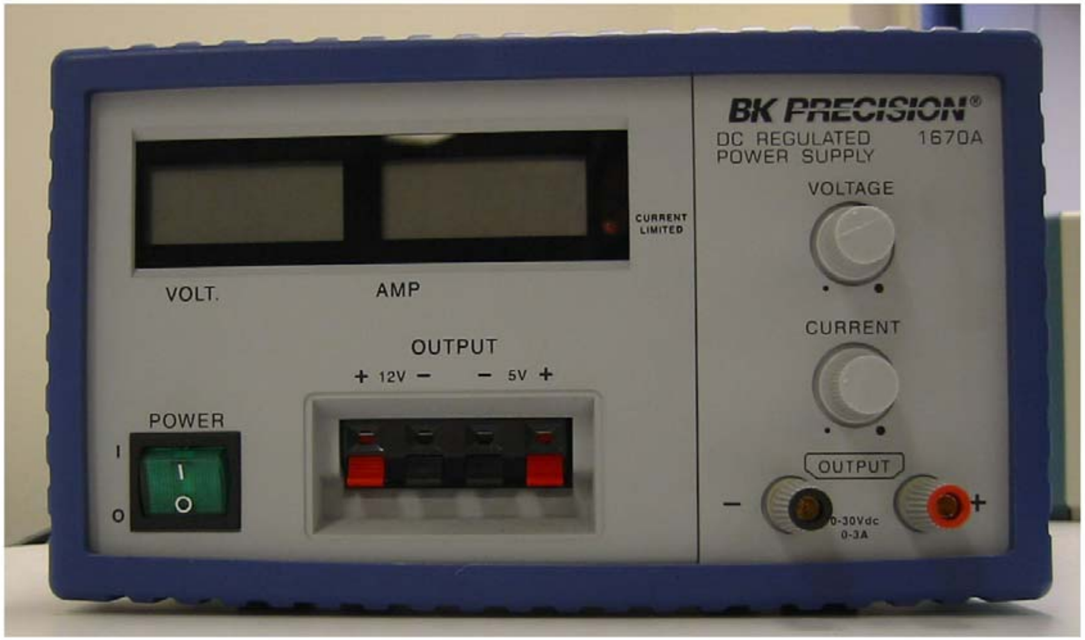
Power Requirements

- The following power supplies are common for analog and digital circuits:

  +5v for digital circuits,
  +15v, -15v for analog,
  -5v, +12v, -12v also used
  +3.3

- Other voltages generally derived.


Proto-Board 203A
POWER ON
+5V at 1.0 AMP
+15V at 0.5 AMP
−15V at 0.5 AMP


BK PRECISION®
DC REGULATED POWER SUPPLY
1670A
CURRENT LIMITED
VOLT.
AMP
OUTPUT
+ 12V − − 5V +
POWER
I
O
VOLTAGE
CURRENT
OUTPUT
−
+
0-30Vdc
0-3A

Boolean Algebra

$A\ B = A\ \&\ B$

$\overline{A}$ = Inverse of A

$\overline{A\ B}$ = Inverse of [A&B]

DeMorgan's Law

$$\overline{A\ B} = \overline{A} + \overline{B}$$

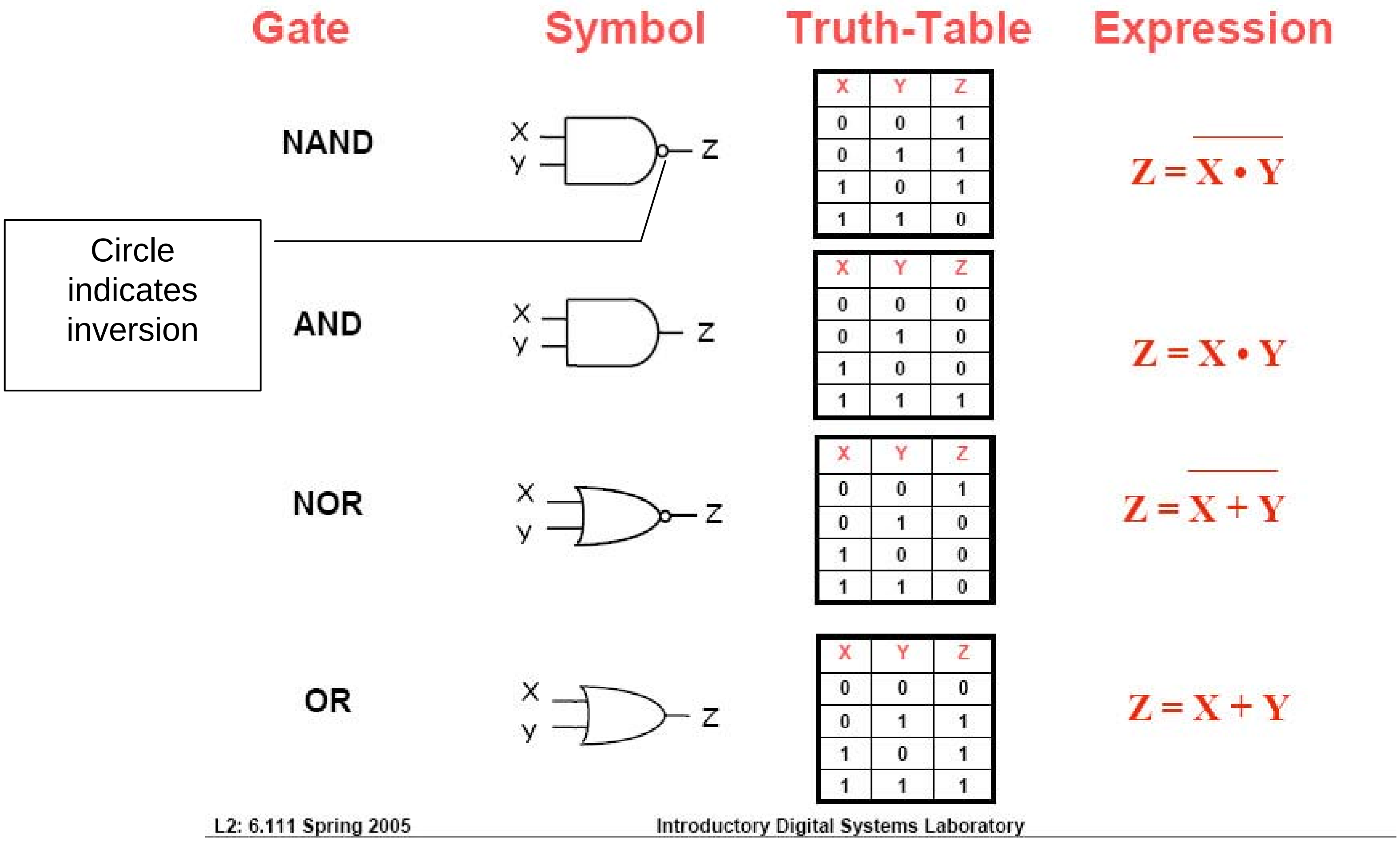
$$\overline{A + B} = \overline{A}\ \&\ \overline{B}$$

Digital System Implementation

- Start with AND, OR, NOR, NAND gates and add more complex building blocks: registers, counters, shift registers, multiplexers. Wire up design. High manufacturing cost, low fix costs. Examples 74LS, 74HC series IC

- For volume production, move to PALs, FPGAs, ASICs. Low manufacturing cost, high fix costs.

Basic Gates



Circle indicates inversion

Gate | Symbol | Truth-Table | Expression

NAND

X	Y	Z
0	0	1
0	1	1
1	0	1
1	1	0

$Z = \overline{X \bullet Y}$

AND

X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

$Z = X \bullet Y$

NOR

X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	0

$Z = \overline{X + Y}$

OR

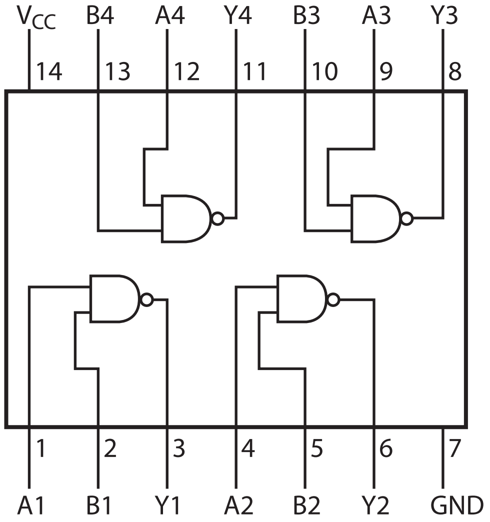
X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

$Z = X + Y$

L2: 6.111 Spring 2005 Introductory Digital Systems Laboratory

74LS00 NAND Gate

Dual-In-Line Package

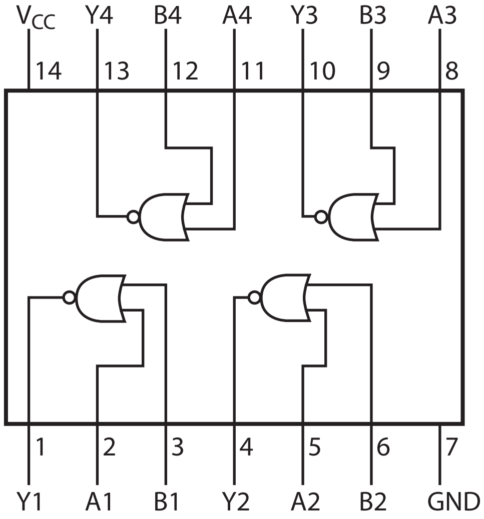


This device contains four independent gates each of which performs the logic NAND function.

Figure by MIT OpenCourseWare, adapted from the National Semiconductor 54LS00 datasheet.

74LS02 NOR Gate

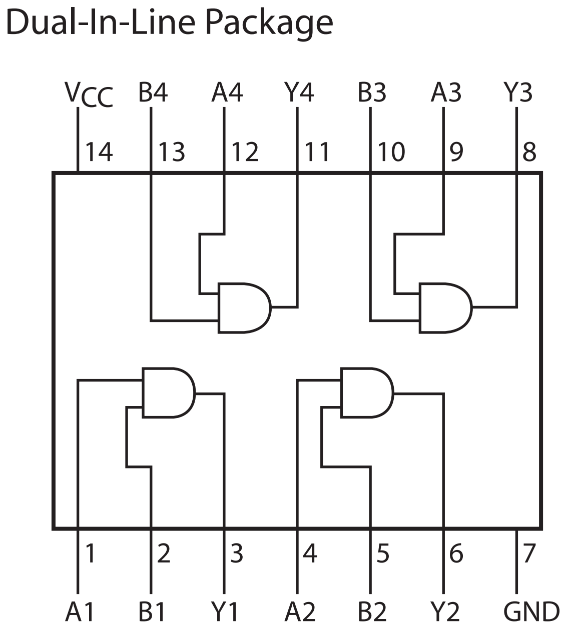
Dual-In-Line Package



This device contains four independent gates each of which performs the logic NOR function.

Figure by MIT OpenCourseWare, adapted from the National Semiconductor 54LS02 datasheet.

74LS08 AND Gate

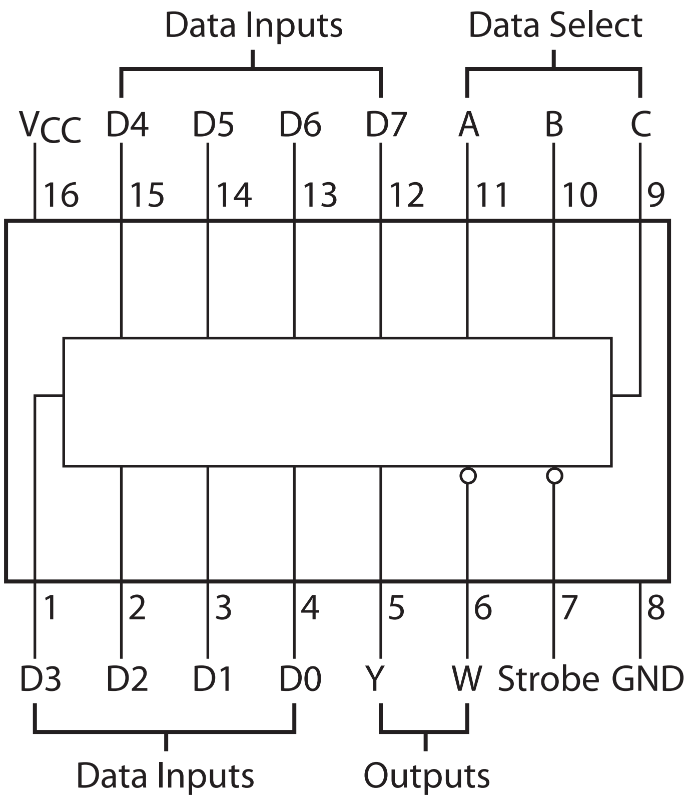


This device contains four independent gates each of which performs the logic AND function.

Figure by MIT OpenCourseWare, adapted from the National Semiconductor 54LS08 datasheet.

74LS151
8-1 Multiplexer

Dual-in-line Package



Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

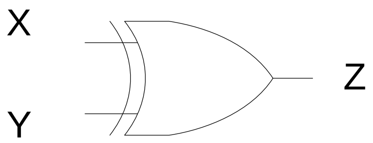
H = High Level, L = Low Level, X = Don't Care

D0, D1_D7 = Level of the Respective D Input

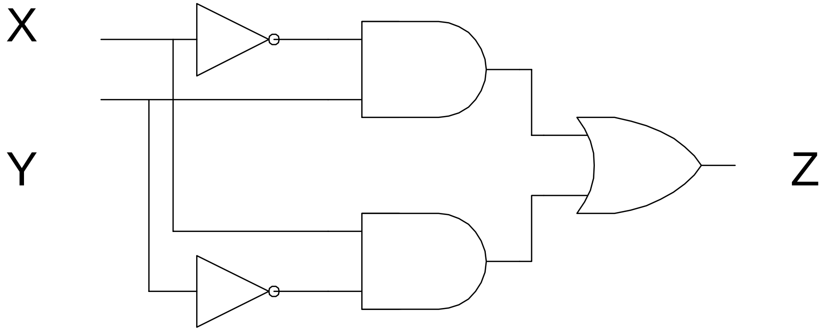
Figures by MIT OpenCourseWare.

Building Logic

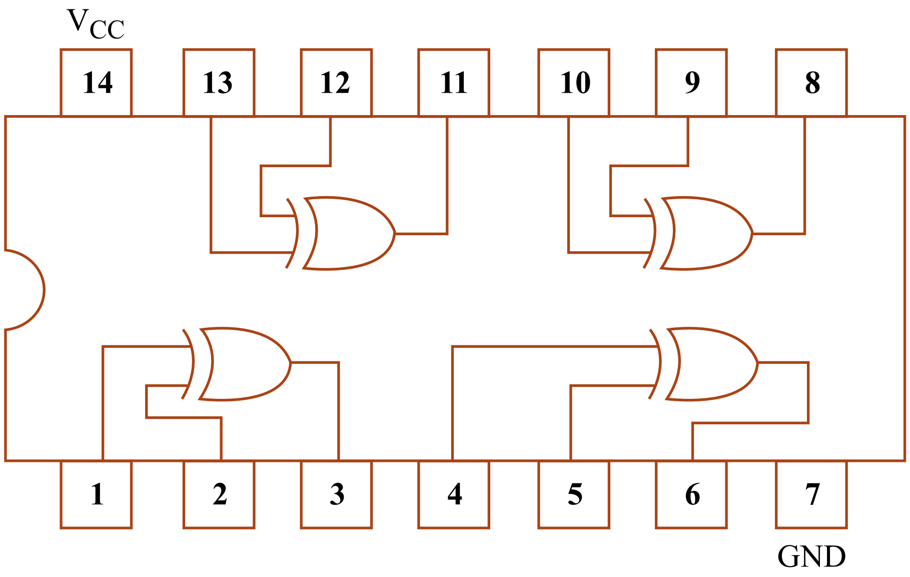
- From basic gates, we can build other functions: Exclusive OR Gate



X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	0



74LS86 Exclusive OR

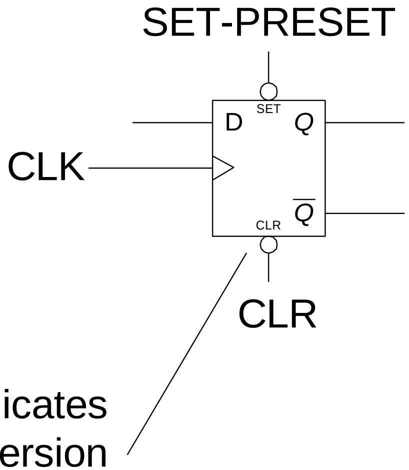


Truth Table

In		Out
A	**B**	**Z**
L	L	L
L	H	H
H	L	H
H	H	L

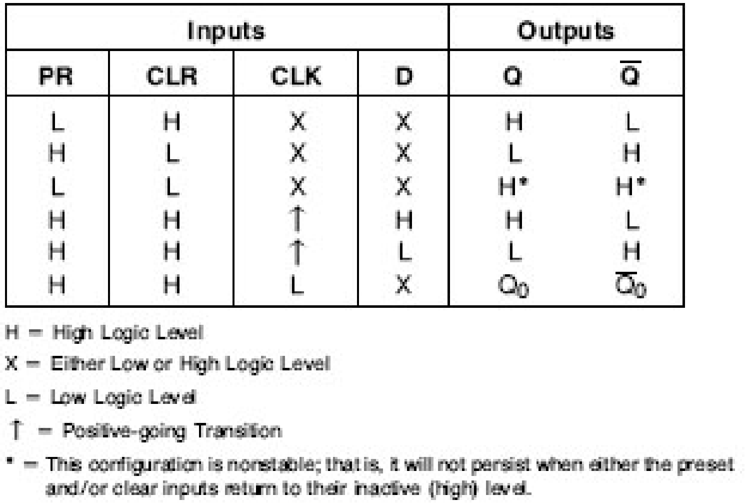
Figure by MIT OpenCourseWare, based on Motorola datasheet.

74LS74 D Flip Flop



circle indicates inversion (active low)

Note both Q and Qbar



Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = High Logic Level

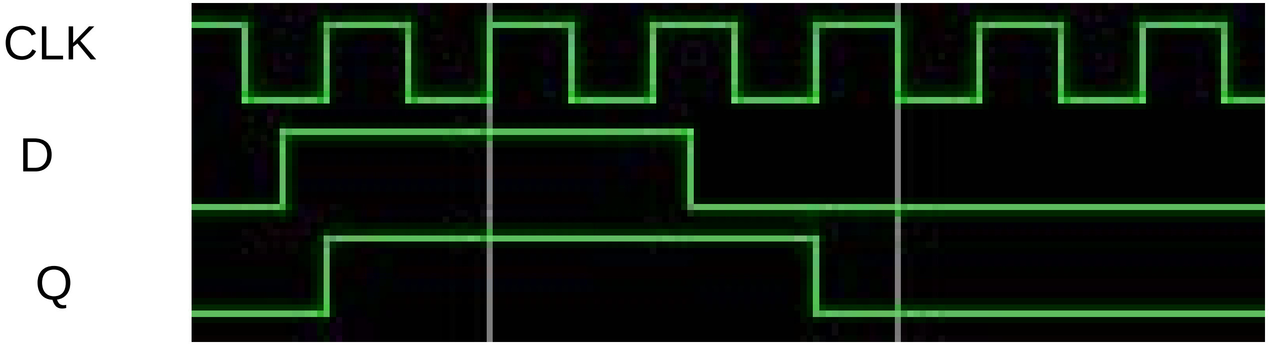
X = Either Low or High Logic Level

L = Low Logic Level

↑ = Positive-going Transition

* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (high) level.

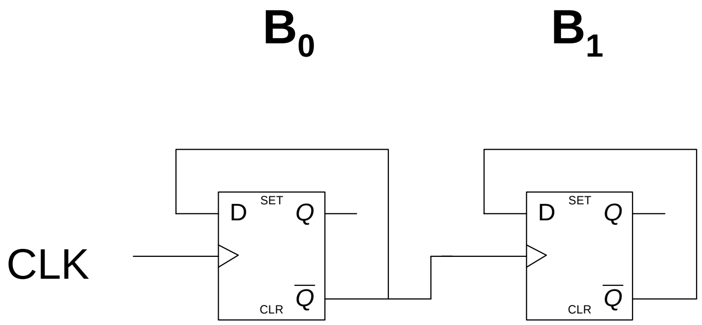
Reprinted with permission of National Semiconductor Corporation.



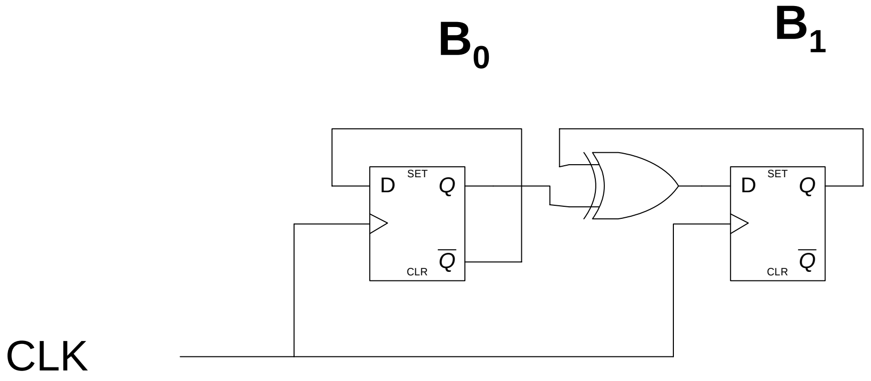
Counters

- Ripple carry
  - Previous stage used to clock next bit;

B_1	B_0
0	0
0	1
1	0
1	1



- Synchronous
  - Same clock used for each bit

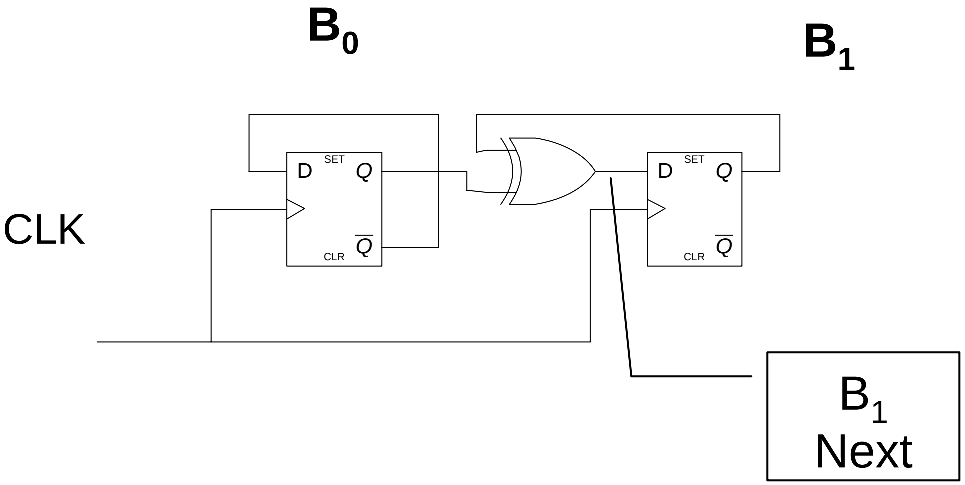


Power connections not shown

Building a Synchronous Counter

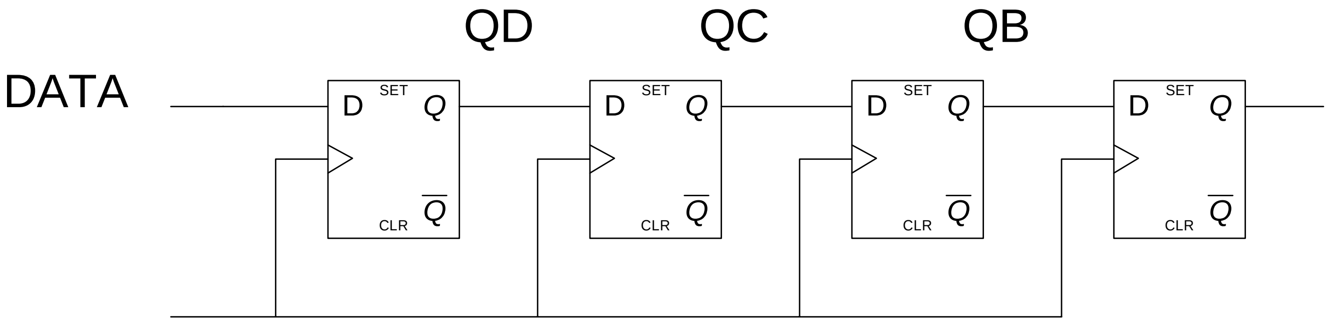
- All bits clock on the same clock signal.
- Next count based on current count.

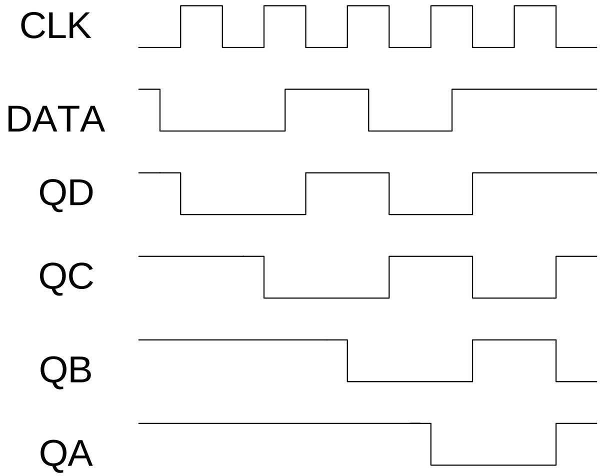
B_1	B_0	B_1 Next
0	0	0
0	1	1
1	0	1
1	1	0



Power connections not shown

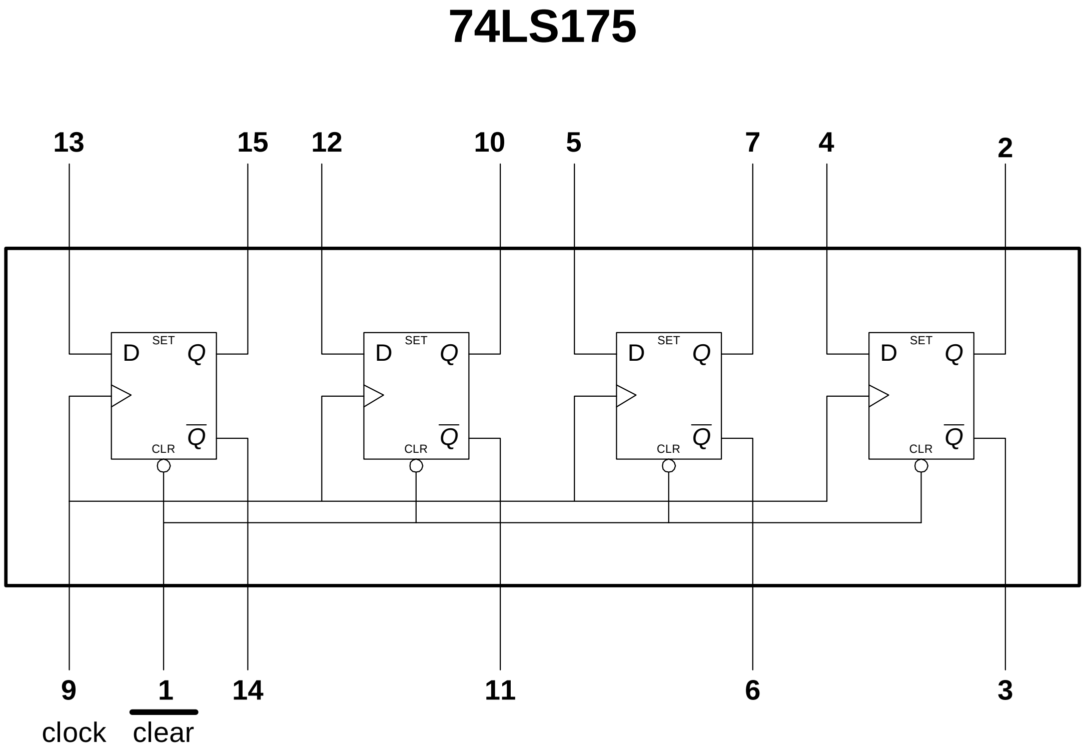
Shift Register





Converts serial data to parallel data or parallel data to serial data.

74LS175 4 Bit Shift Register



Clock and $\overline{\text{Clear}}$ are common for all FF. The D FF will store the state of their individual D inputs on the LOW to HIGH Clock transition, causing the individual Q and $\overline{Q}$ to follow.

A LOW input on the $\overline{\text{Clear}}$ will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs.

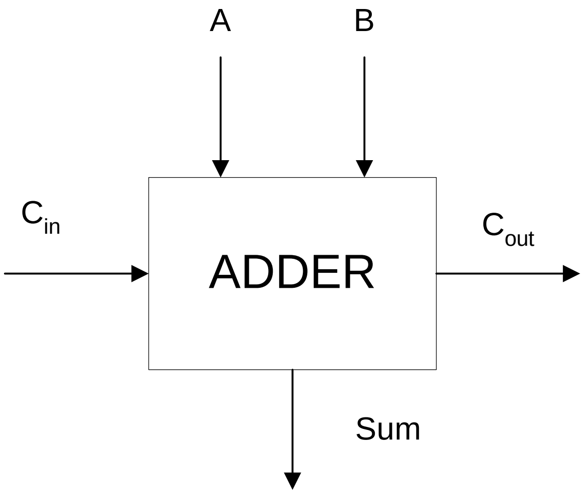
Binary Numbers

- MSB – Most Significant Bit
- LSB – Least Significant Bit
- Let’s build an adder:
  A+B=S where A,B,S are m bits wide:
  A: $A_mA_{m-1}\ldots A_1A_0$

Dec	Binary	Hex		Dec	Binary	Hex
0	0000	0		8	1000	8
1	0001	1		9	1001	9
2	0010	2		10	1010	A
3	0011	3		11	1011	B
4	0100	4		12	1100	C
5	0101	5		13	1101	D
6	0110	6		14	1110	E
7	0111	7		15	1111	F

Binary Adder – mth bit

C_{in}	A	B	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



Sum =

C_{out} =

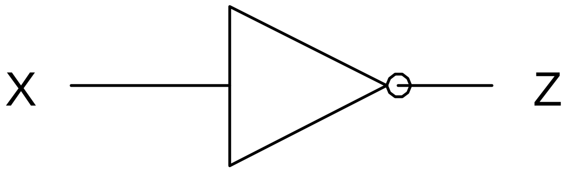
Signed Numbers – Twos Complement

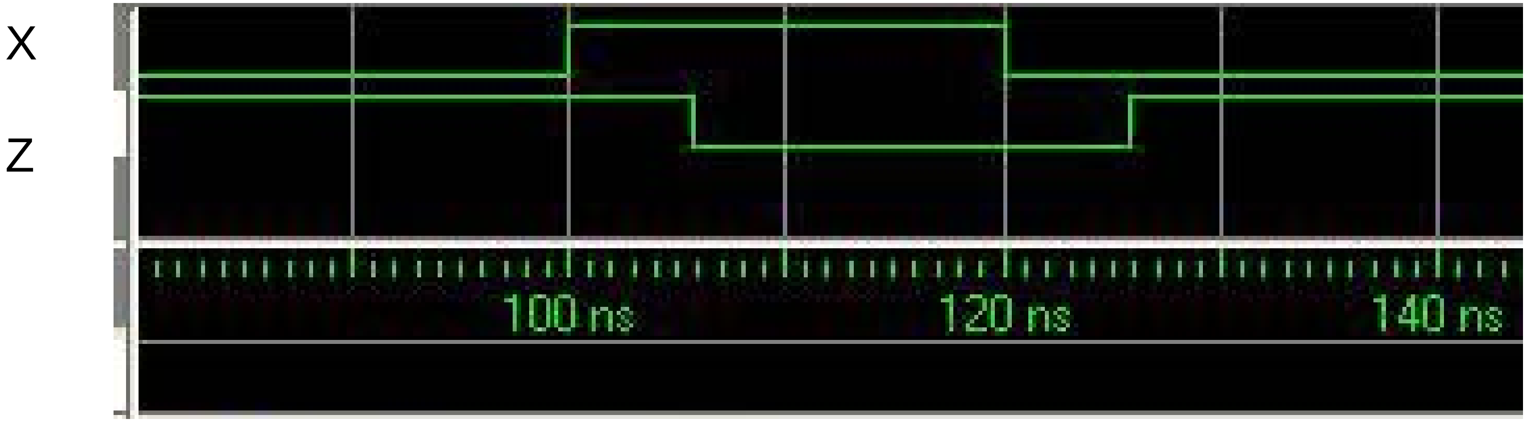
- Positive Number: MSB=0
- Negative Number: MSB=1
- 4 Bit example
- Simple addition & subtraction
- Most common notation

MSB			LSB	Decimal
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	-8
1	0	0	1	-7
1	0	1	0	-6
1	0	1	1	-5
1	1	0	0	-4
1	1	0	1	-3
1	1	1	0	-2
1	1	1	1	-1

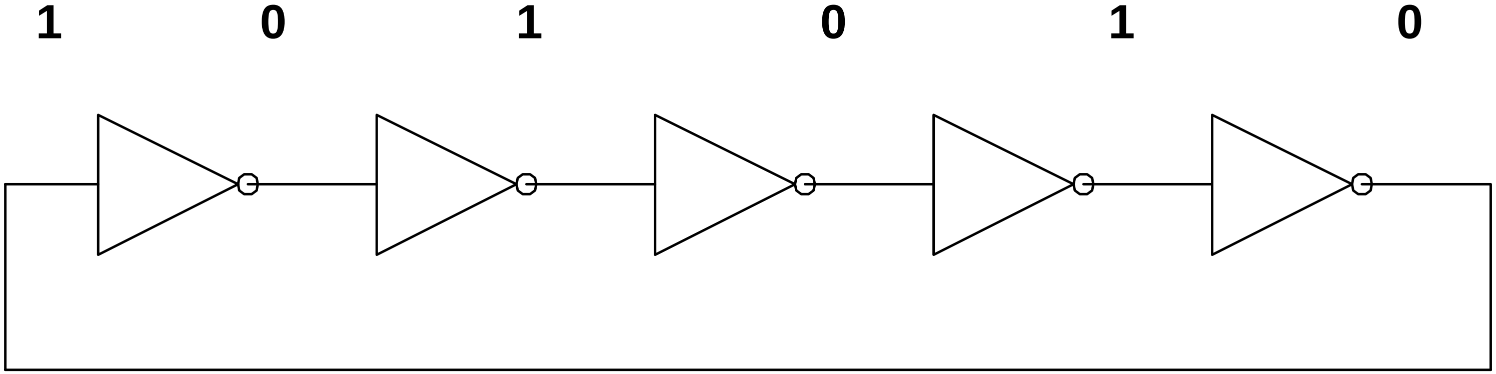
Propagation Delays

- All digital logic have propagation delay
- Typical discrete logic gate propagation delay ~10ns





Lab Exercise Ring Oscillator



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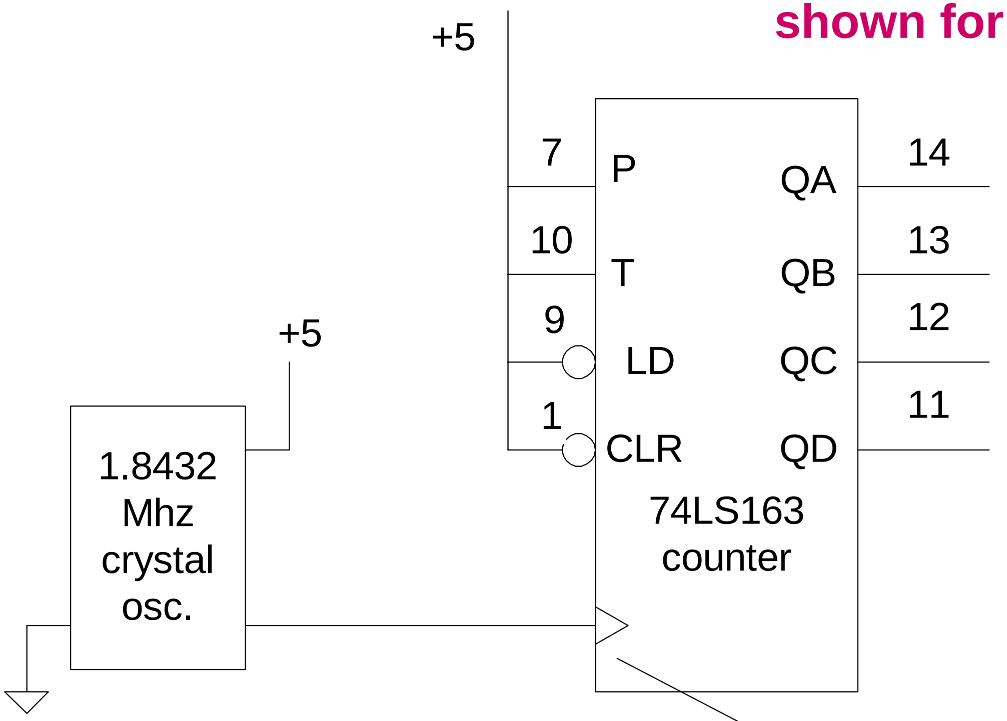
Lab Exercise
4 Bit Counter – Logic Analyzer

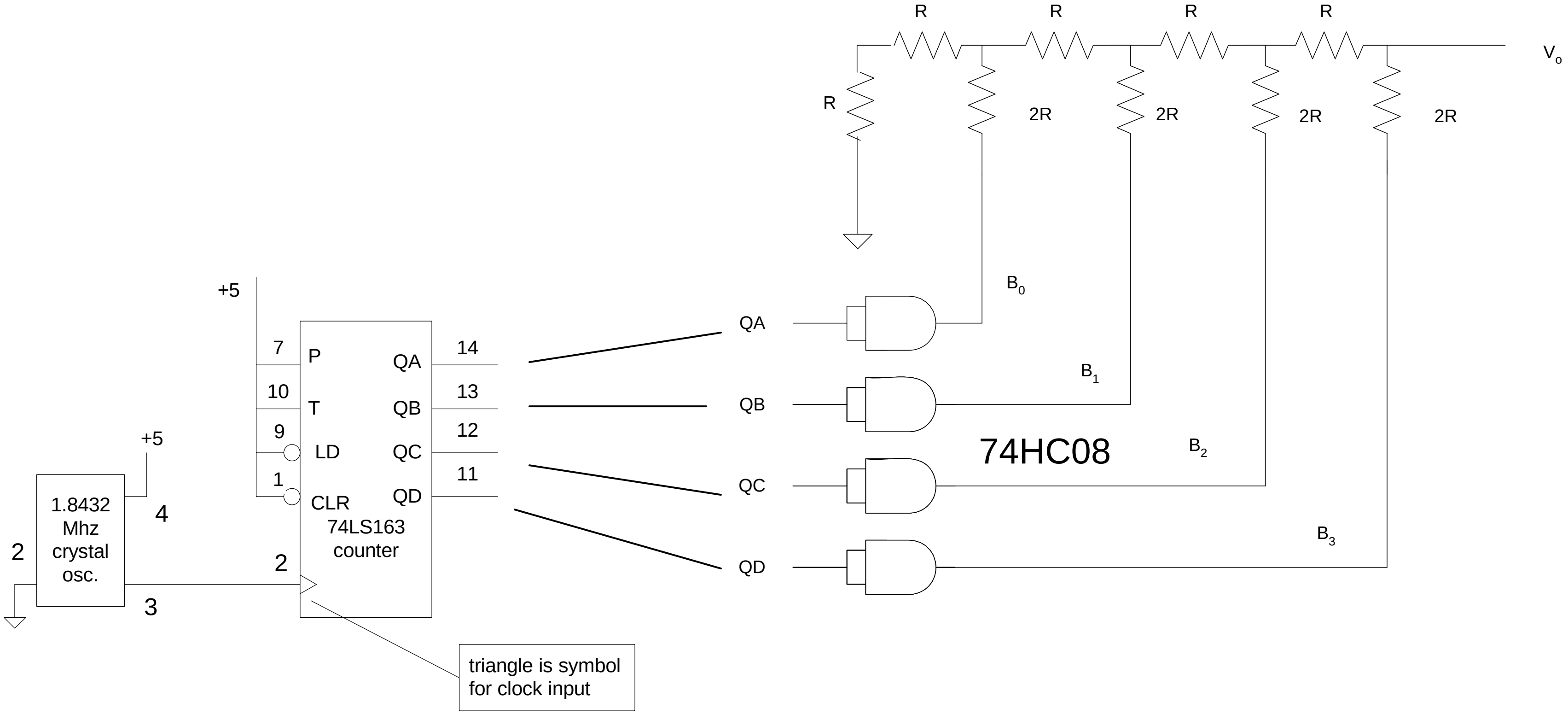
Power connections not shown for 74LS163



Attach LA probe A2 to QA-QD

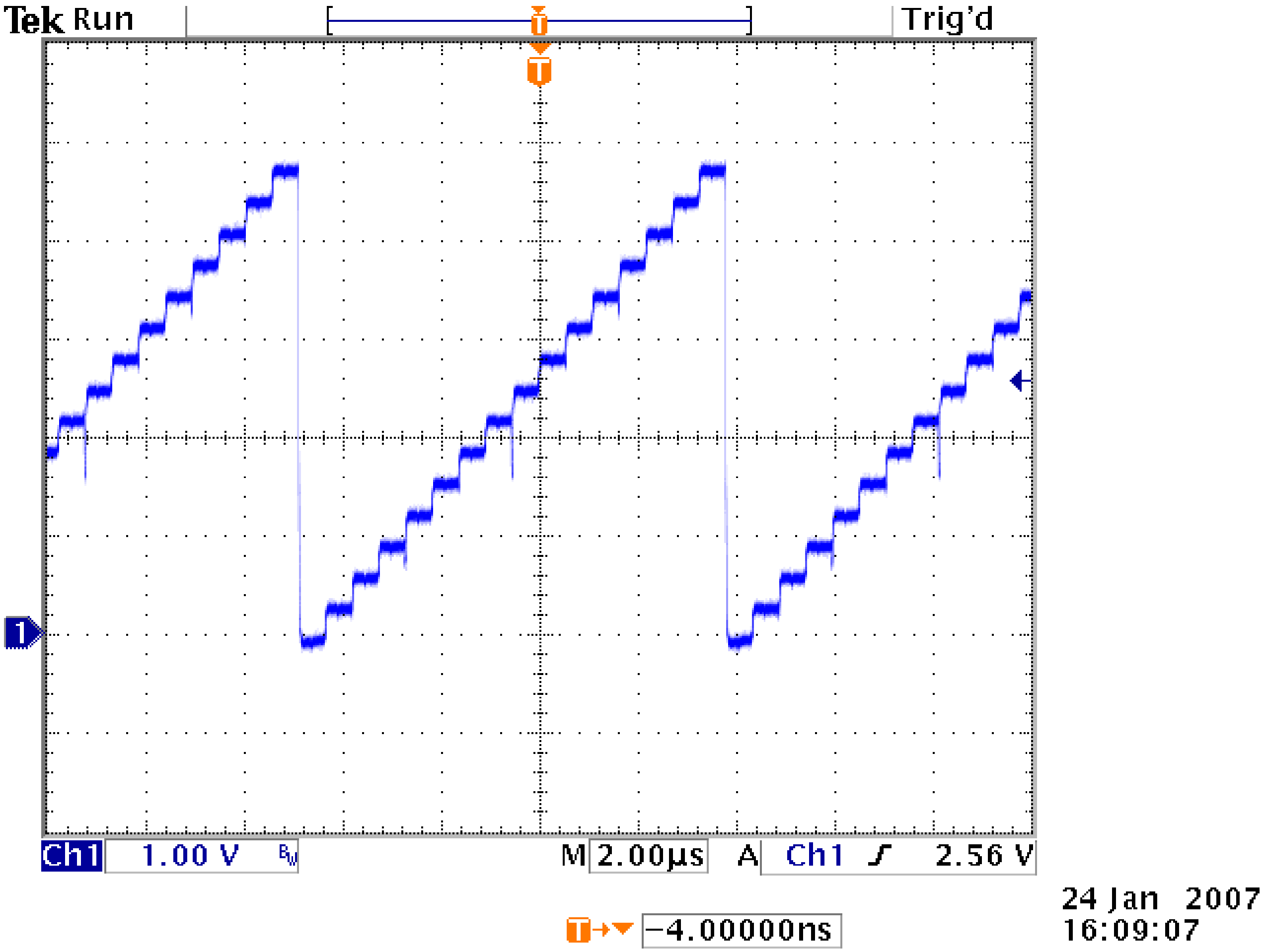
triangle is symbol for clock input

Lab Exercise
Ramp Generator



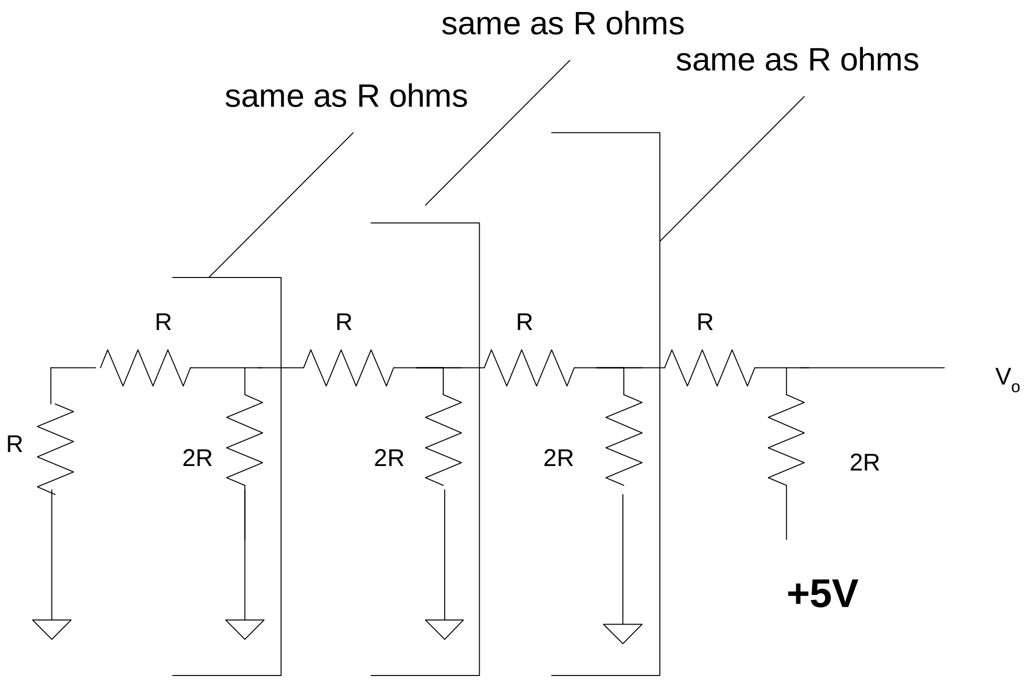
triangle is symbol for clock input

RAMP Generator Output



R-2R Theory

- For linear circuits, superposition applies. Calculate contribute of bit n by setting all other inputs to zero.
- Equivalent resistance looking left or right is R ohms!
- Use Thevenin equivalent to show division by 2^n



DA Summary

- Output from digital to analog conversion are discrete levels.
- More bits means better resolution.
- An example of DA conversion
  - Current audio CD’s have 16 bit resolution or 65,536 possible output levels
  - New DVD audio samples at 192 khz with 24 bit resolution or 2^{24} = 16,777,216

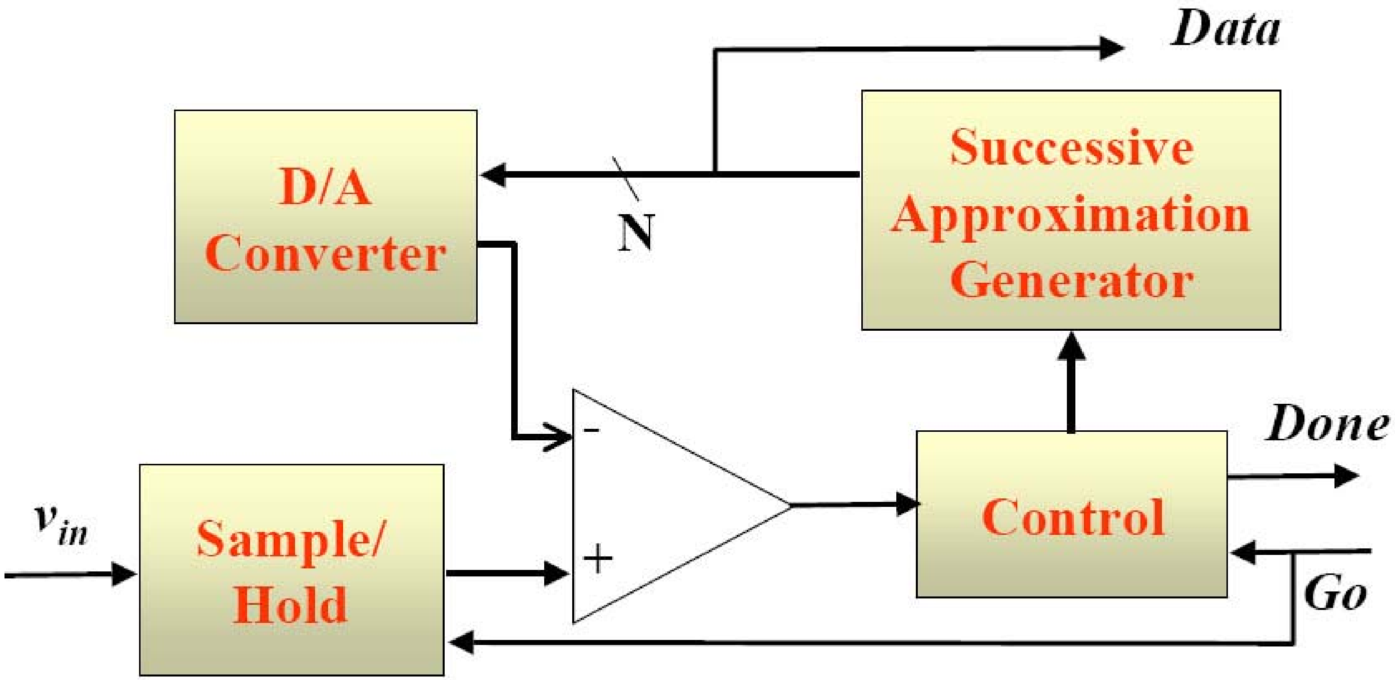
Analog to Digital Conversion (ADC)

- Successive approximate conversion steps
  - Scale the input to 0-3 volts (example)
  - Sample and hold the input
  - Internally generate and star case ramp and compare

- Flash Compare
  - Compare voltage to one of 2^n possible voltage levels. 8 bit ADC would have 255 comparators.

- Note that by definition, ADC have quantizing errors (number of bits resolution)

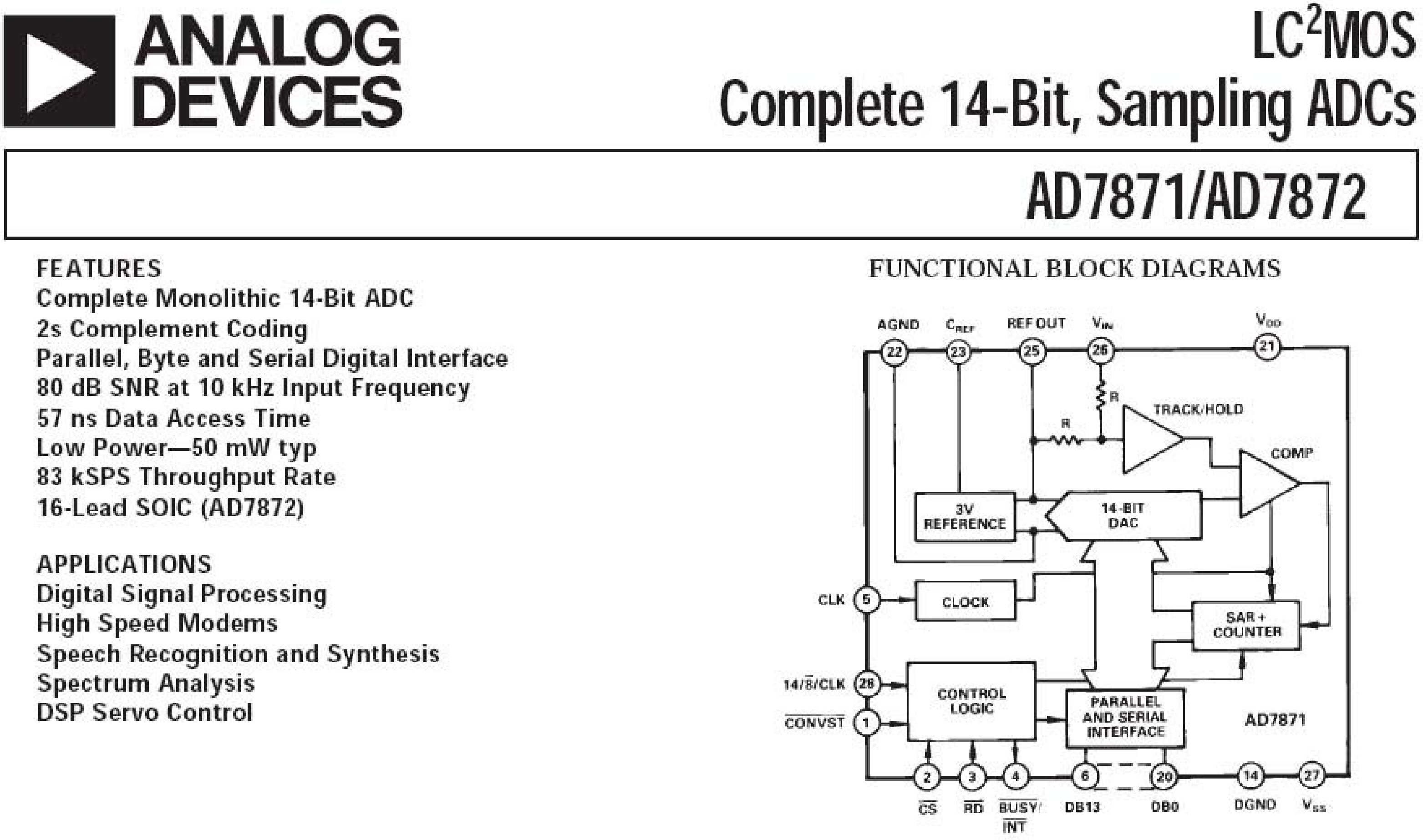
Successive Approximation AD



Serial conversion takes a time equal to $N(t_{D/A} + t_{comp})$

6.111 L14, Fall ‘05

AD7871



ANALOG DEVICES

LC²MOS
Complete 14-Bit, Sampling ADCs

AD7871/AD7872

FEATURES
Complete Monolithic 14-Bit ADC
2s Complement Coding
Parallel, Byte and Serial Digital Interface
80 dB SNR at 10 kHz Input Frequency
57 ns Data Access Time
Low Power—50 mW typ
83 kSPS Throughput Rate
16-Lead SOIC (AD7872)

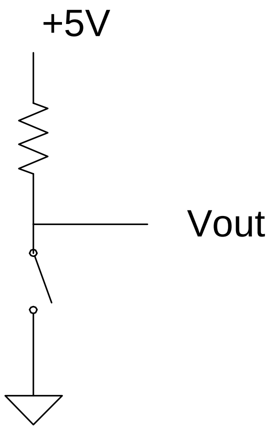
APPLICATIONS
Digital Signal Processing
High Speed Modems
Speech Recognition and Synthesis
Spectrum Analysis
DSP Servo Control

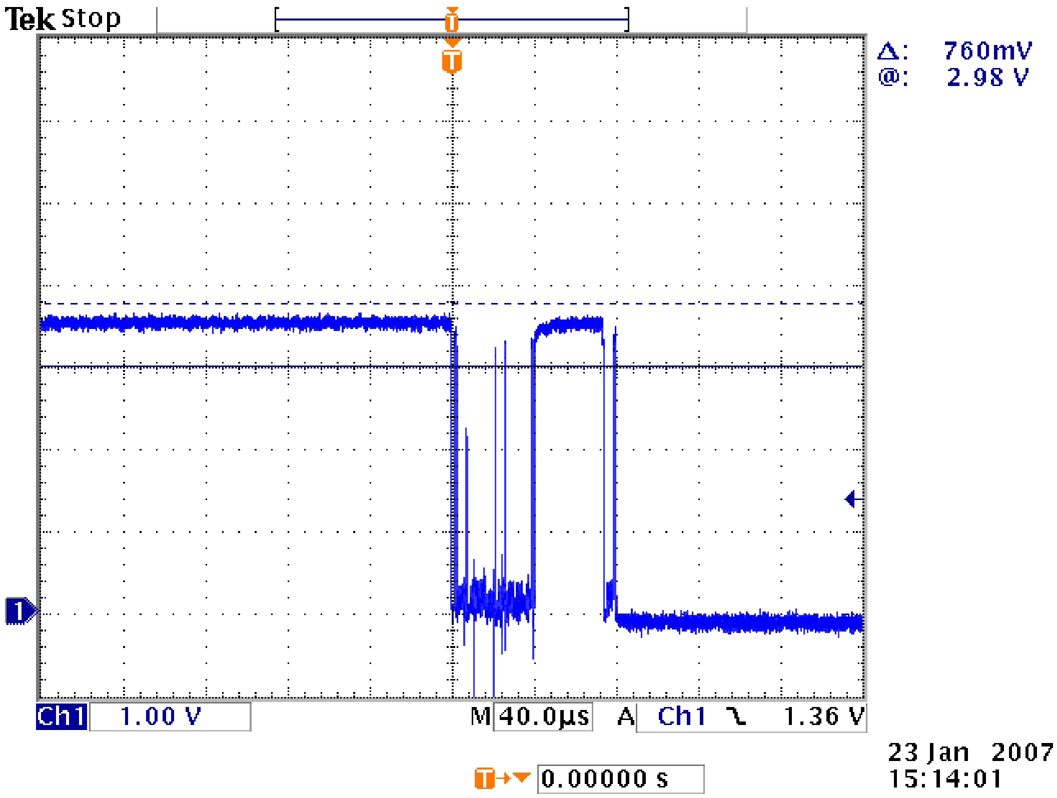
FUNCTIONAL BLOCK DIAGRAMS

Courtesy of Analog Devices. Used with permission.

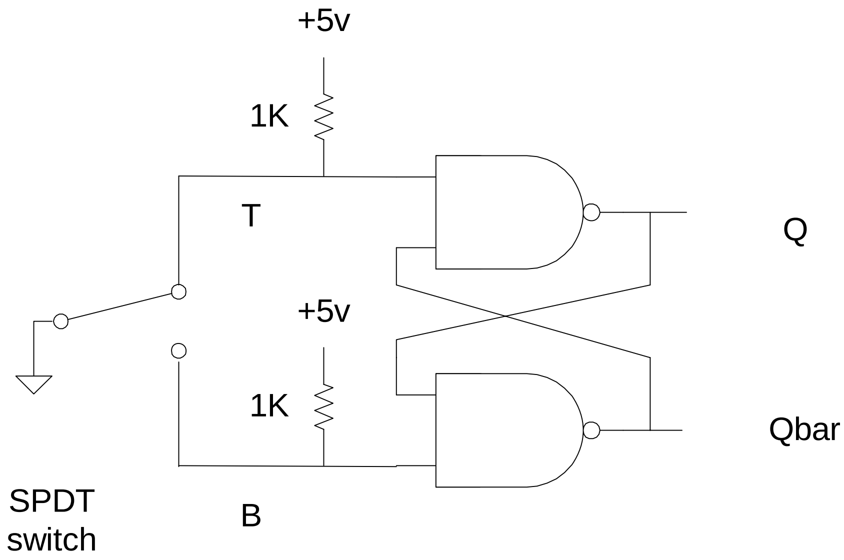
Switch Bounce

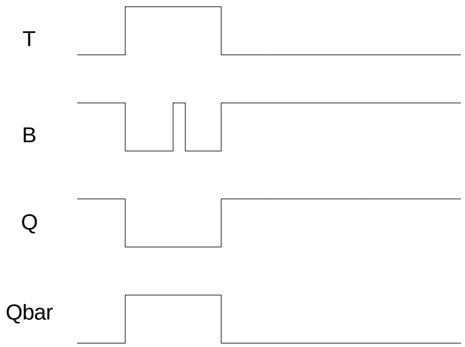
- All mechanical switches have “switch bounce”





Debounce Circuit





Requires SPDT switch

Lab 4

- Use last three aisles on the left at the end of the 6.111 lab
- Pick up IC’s and tools from LA’s.
- Return IC’s and tools to LA’s at the end of the lab

Lab 5

- Design, build and keep the electronics for a digital lock.
- Unlock key based on sequence of 0, 1.