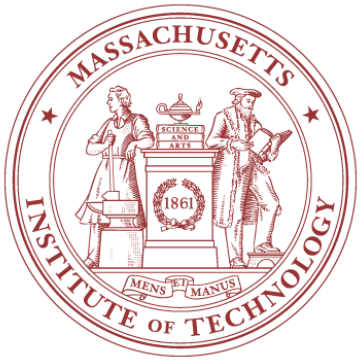
Viterbi Algorithm
Survivor Path Decoding

Lecture 16

Vladimir Stojanović



6.973 Communication System Design – Spring 2006

Massachusetts Institute of Technology

Decision memory organization

- Survivor paths always merge L=5K steps back
  - K= $\log_2$(number of states) = (constraint length – 1)

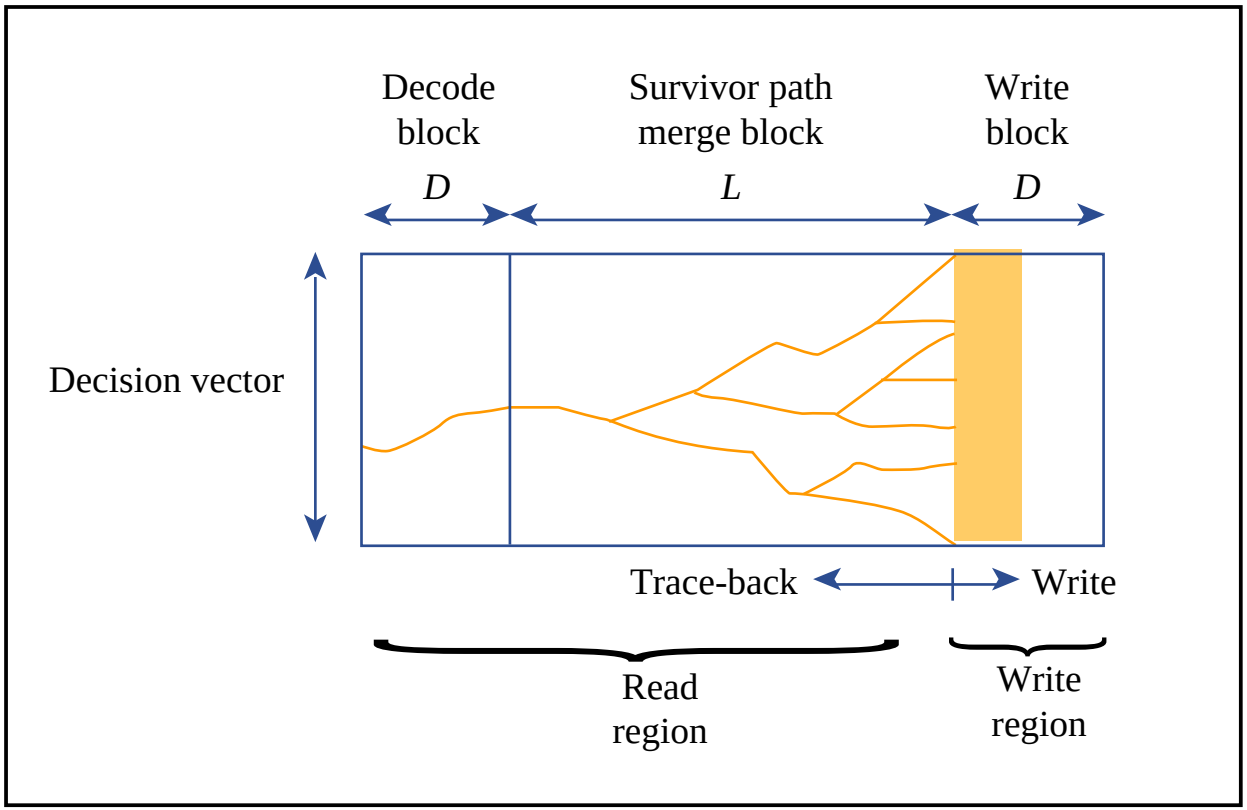


Figure by MIT OpenCourseWare.

Survivor path decoding

- Essentially two ways to perform the decode
  - Register exchange
  - Trace-back
- A set of registers equal to the number of states (for the duration of the survivor path)

- Register exchange
  - Registers keep the values of the decoded data directly
    - Decoded data are the ACS decisions
- Trace-back
  - Registers keep track of the survivor path
    - Just keep the pointers and figure out decisions on the fly

The role of decision bits

- Decision d_n points to the previous state
  - $S_{n-1}=d_n^{Sn}(S_n>>1)$ (for example 1x=1 (x0>>1))

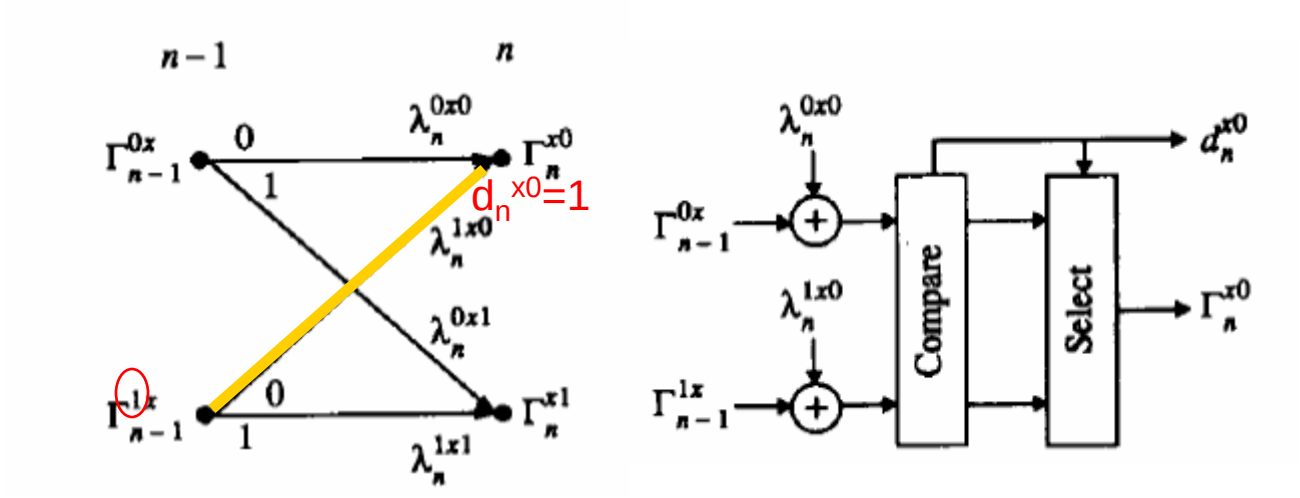
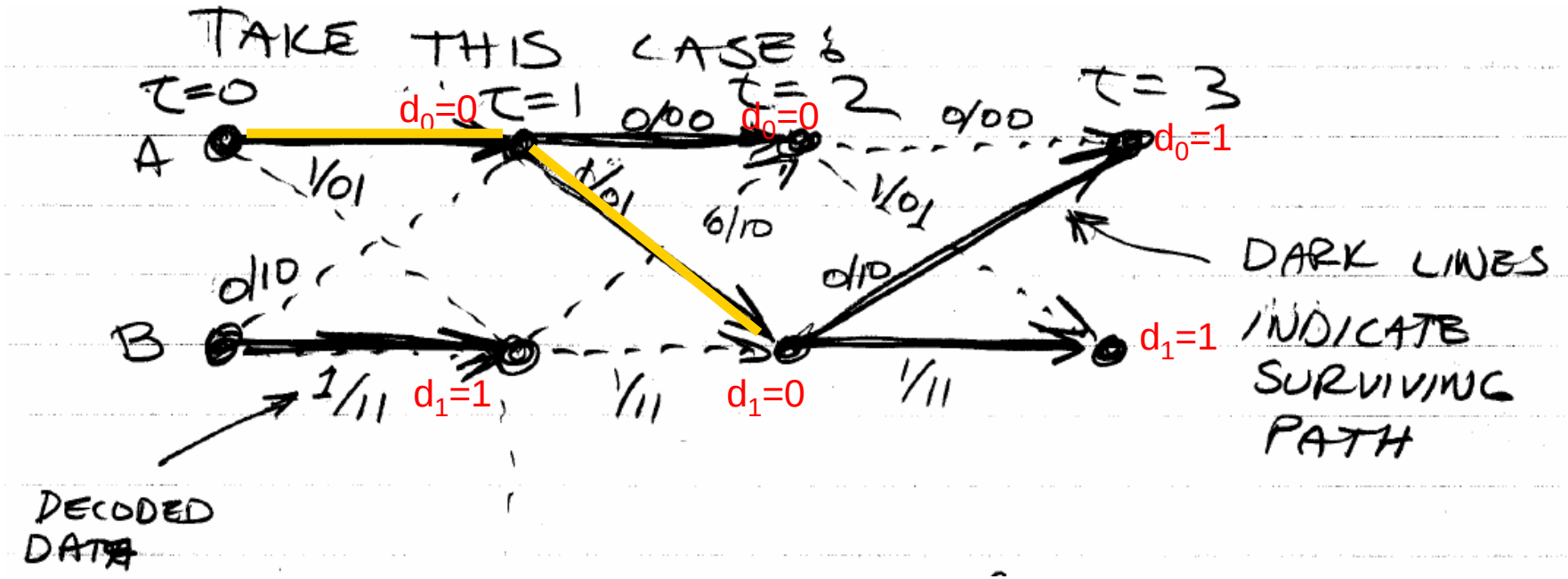
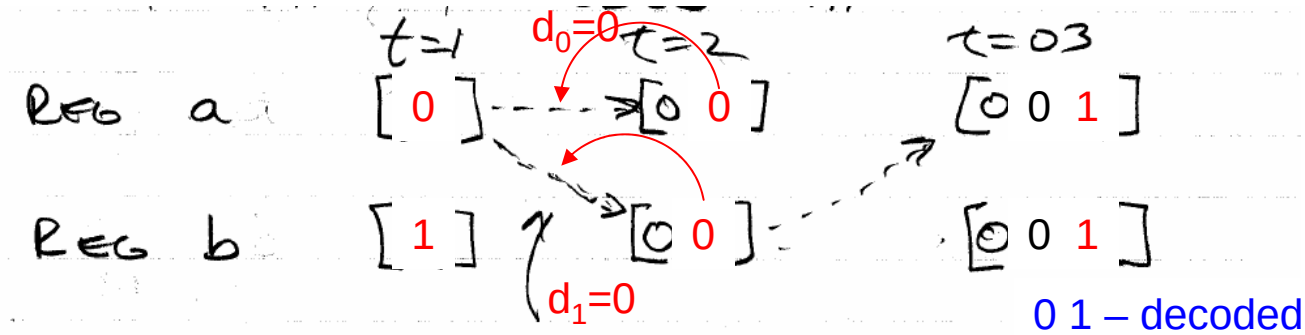


Figure from Black, P. J., and T. Y. Meng. "A 1-Gb/s, Four-state, Sliding Block Viterbi Decoder." *IEEE Journal of Solid-State Circuits* 32 (1997): 797-805. Copyright 1992 IEEE. Used with permission.

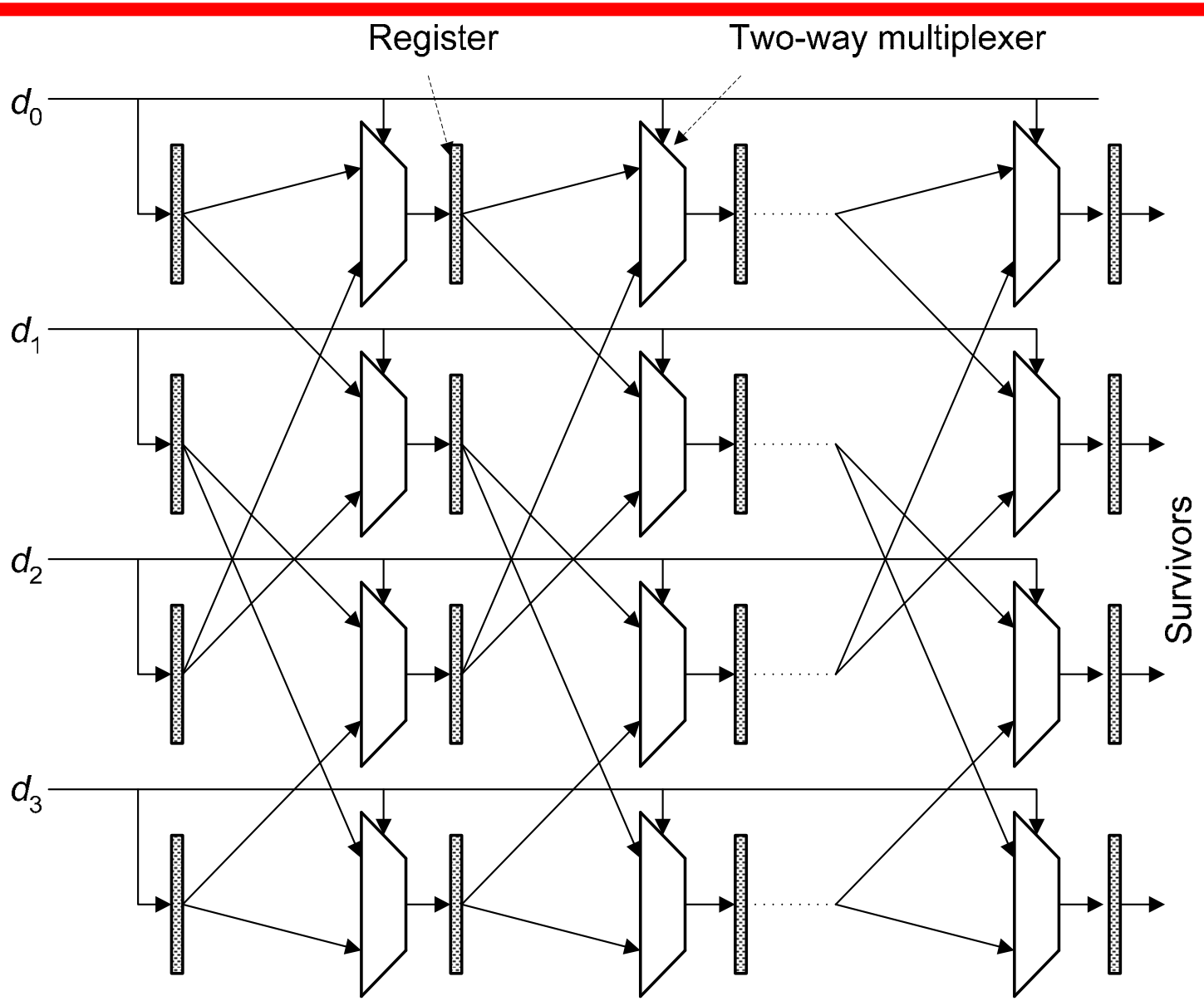
Register exchange example



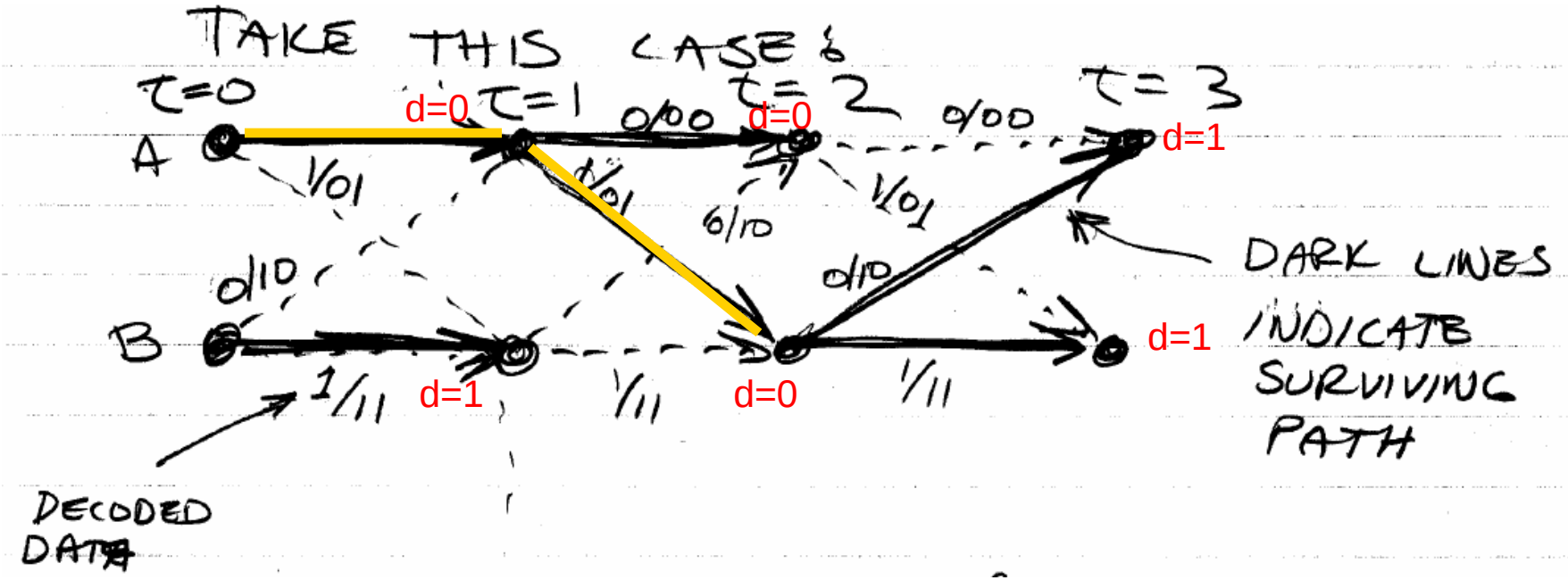
- Every state has a register of length of the whole survivor path
- Contents of register at each time is the decoded data



Register exchange implementation



Trace-back example



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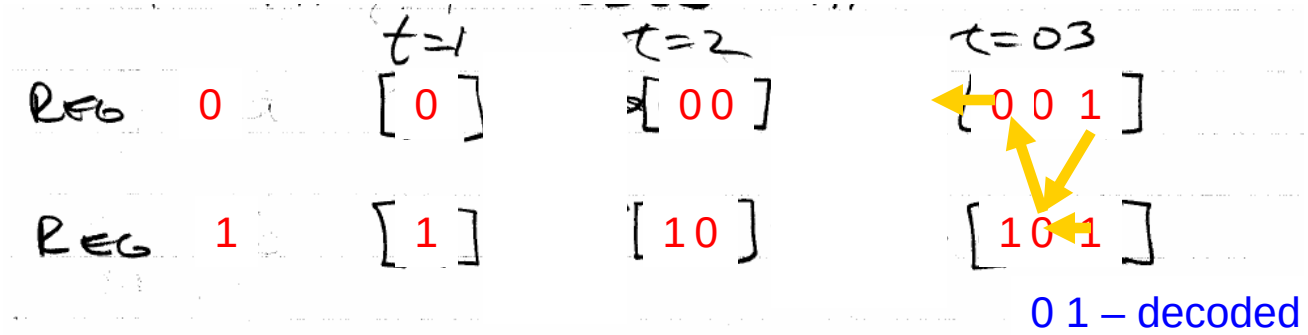
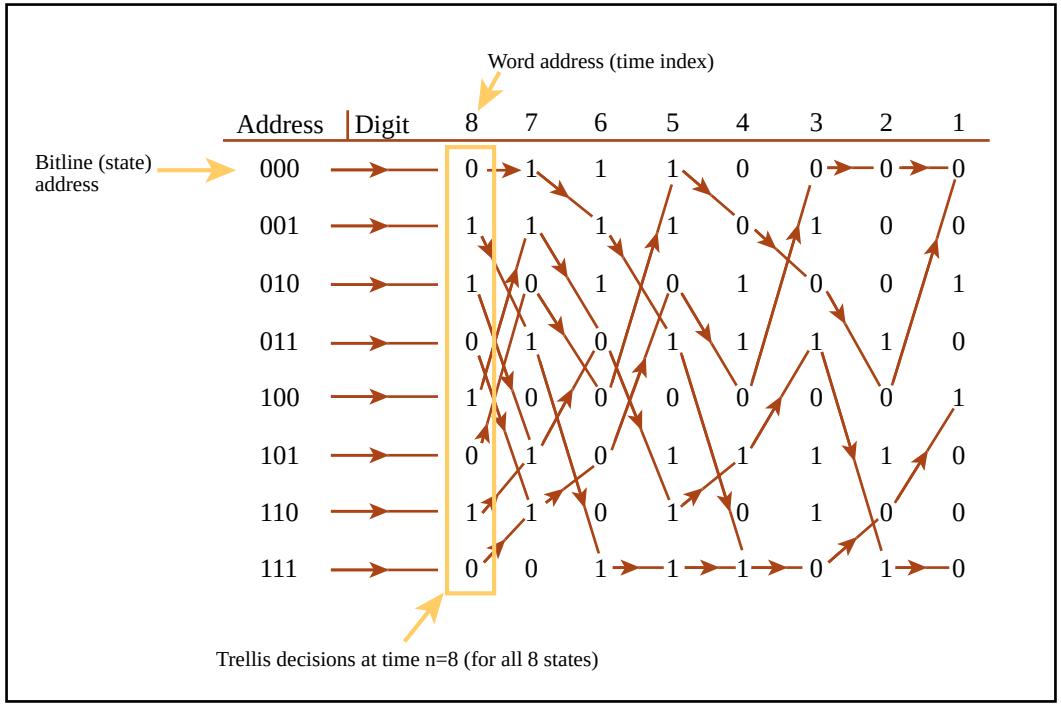


Trace-back contd.

- Proposed by Rader in ’81



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Trace-back contd.

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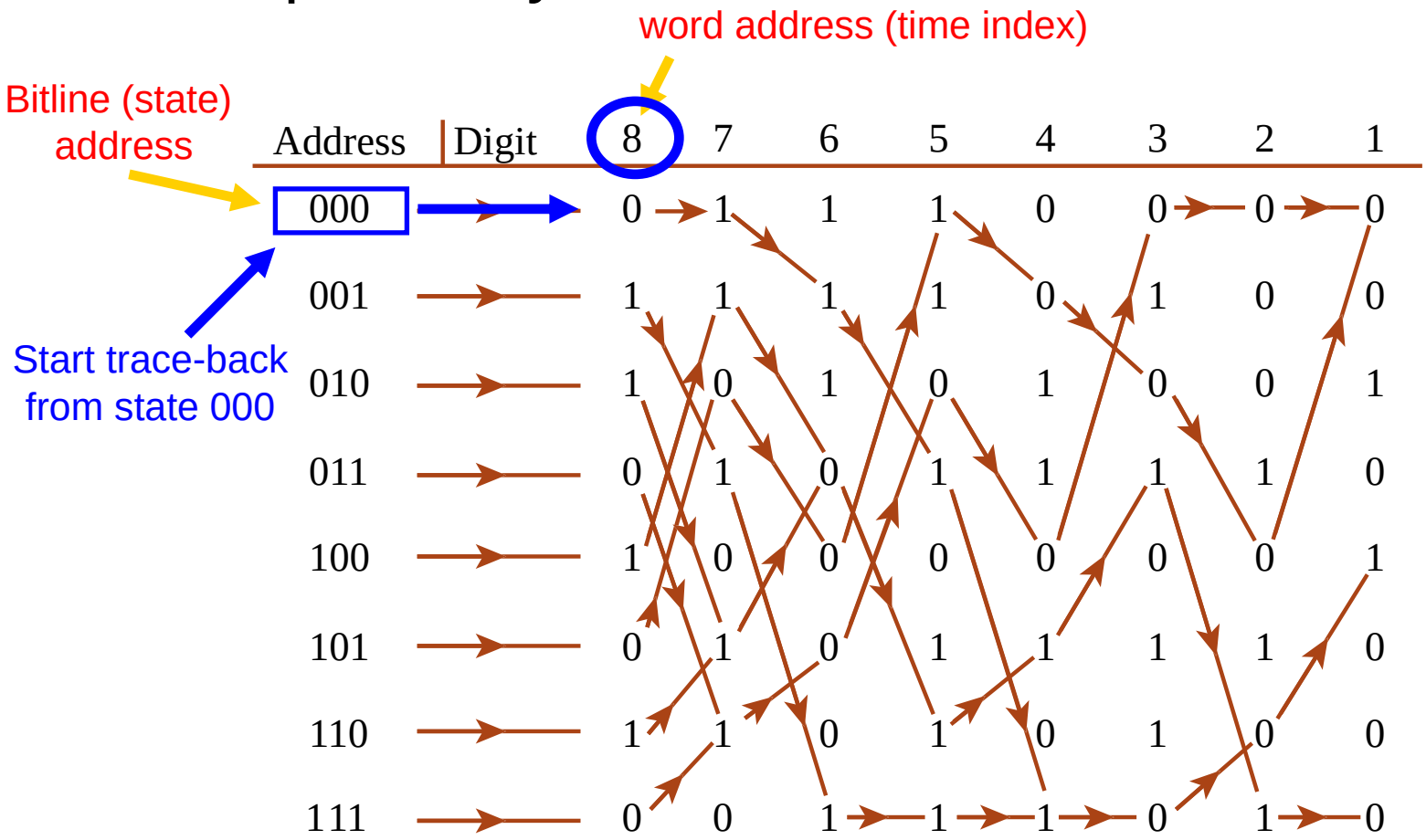

Figure by MIT OpenCourseWare.

Trellis decisions at time n=8 (for all 8 states)

Trace-back contd.

- Proposed by Rader in ’81

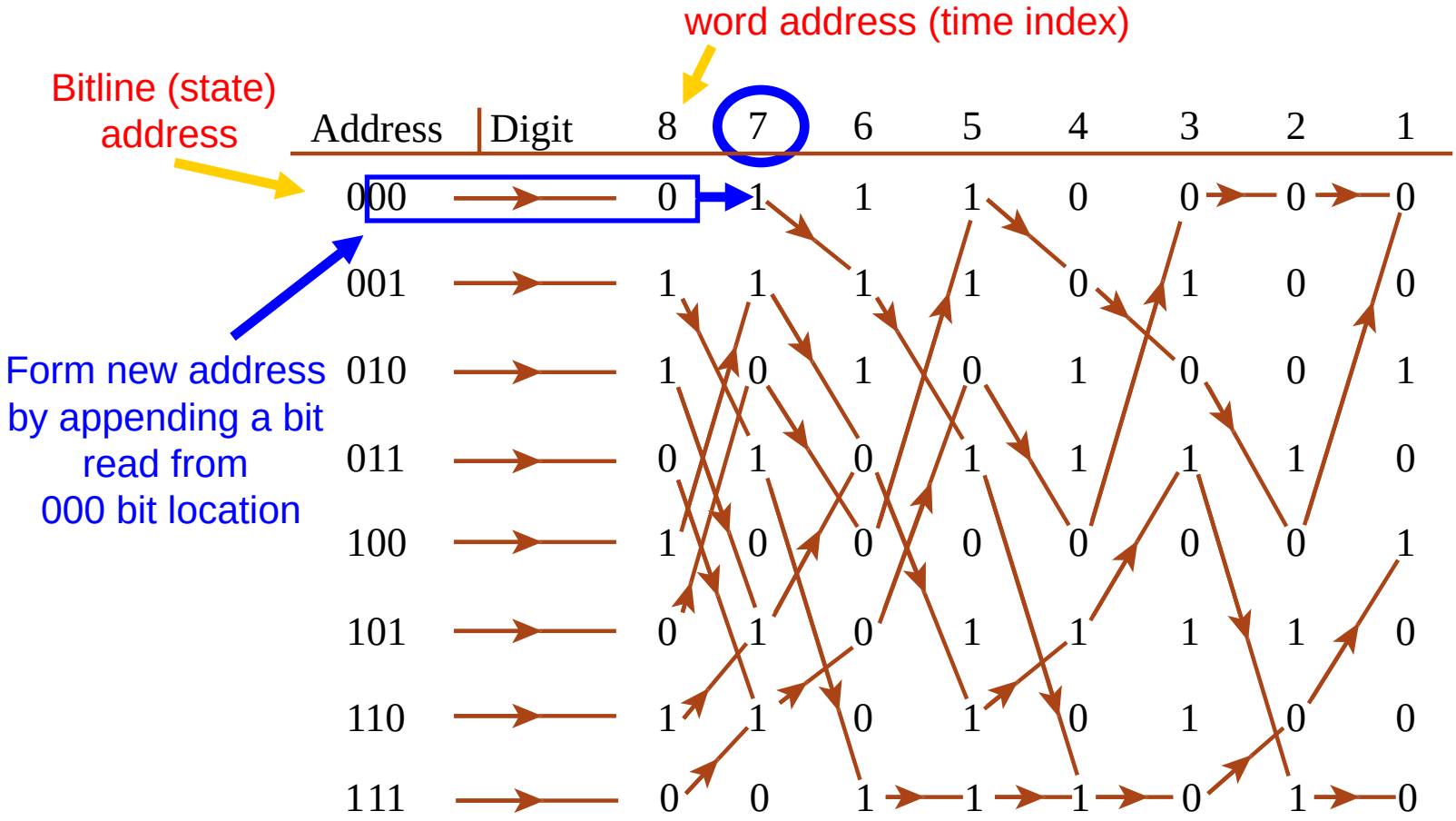

Figure by MIT OpenCourseWare.

Trellis decisions at time n=8 (for all 8 states)

Trace-back contd.

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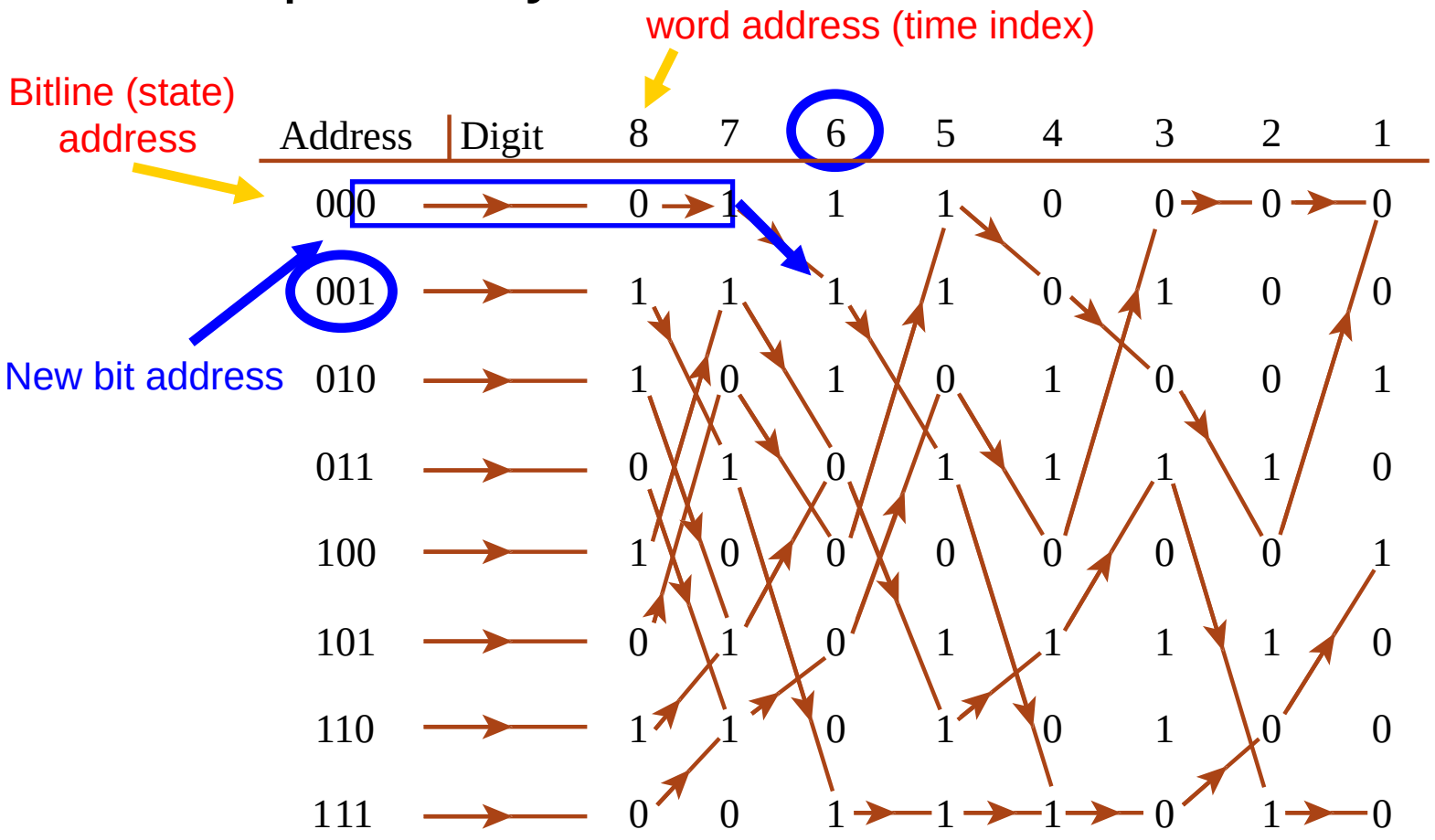

Figure by MIT OpenCourseWare.

Trellis decisions at time n=8 (for all 8 states)

Trace-back contd.

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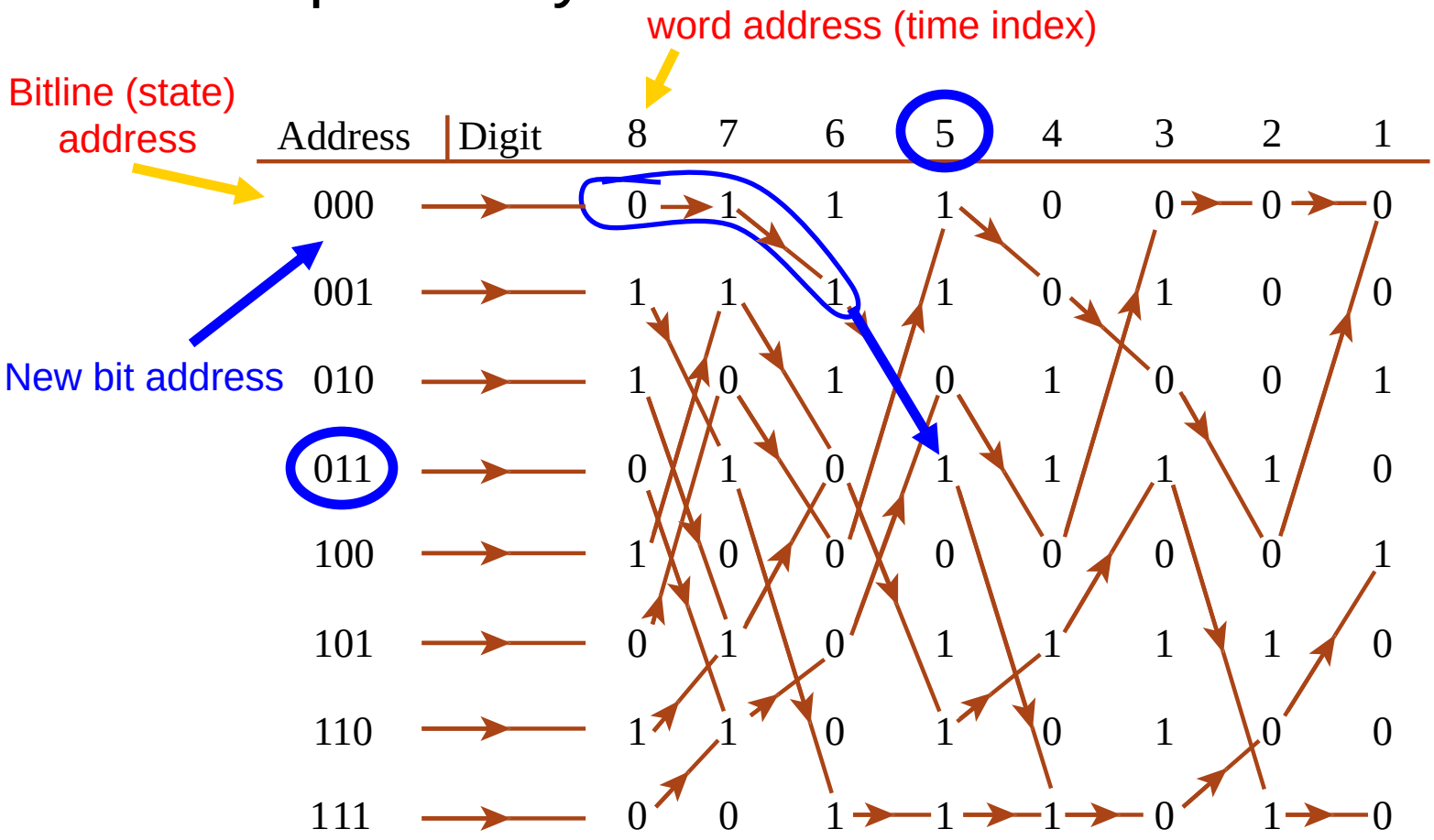


Figure by MIT OpenCourseWare.

Trellis decisions at time n=8 (for all 8 states)

Radix-4 and Radix-16 trace-back

- Radix-2

$$S_{n-1} = d_n^S (S_n >> 1)$$

- Radix-4

$$S_{n-2} = d_n^S (S_n >> 2)$$

- Radix-16

$$S_{n-2} = d_n^S (S_n >> 2)$$
$$S_{n-4} = d_{n-2}^S (S_{n-2} >> 2)$$

$$S_{n-4} = d_{n-2}^S (d_n^S (S_n >> 2) >> 2)$$
$$= d_{n-2}^S d_n^S (S_n >> 4)$$
$$= d_{n,n-2}^S (S_n >> 4)$$

1 bit decision

2 bit decision

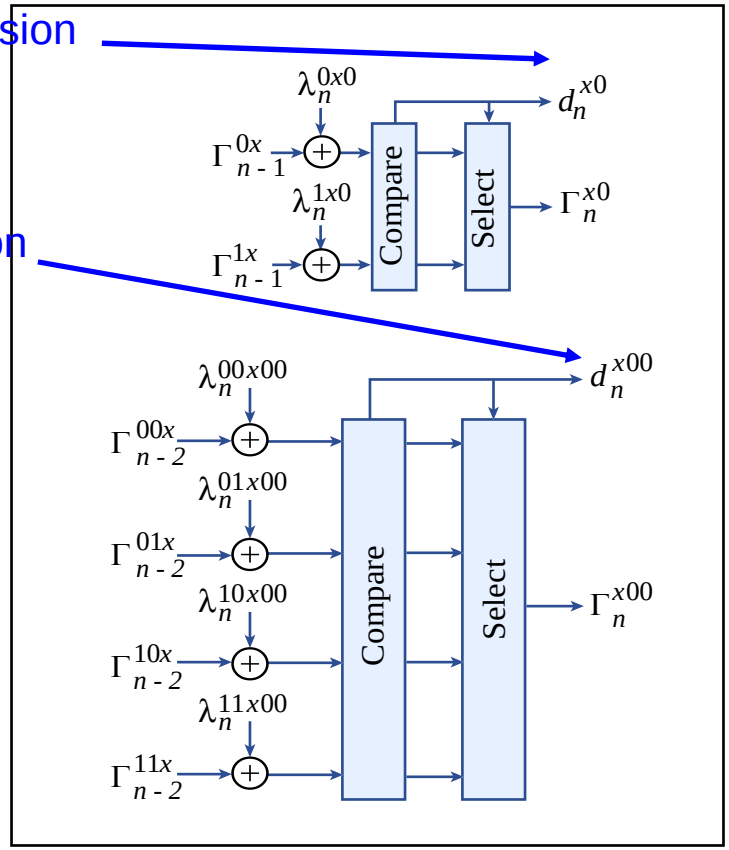


Figure by MIT OpenCourseWare.

Unrolling useful when memory access slow

Allows to read/write memory every other ACS computation

4 bit composite decision

Pretrace-back unit

- Pretrace-back is calculation of composite decisions

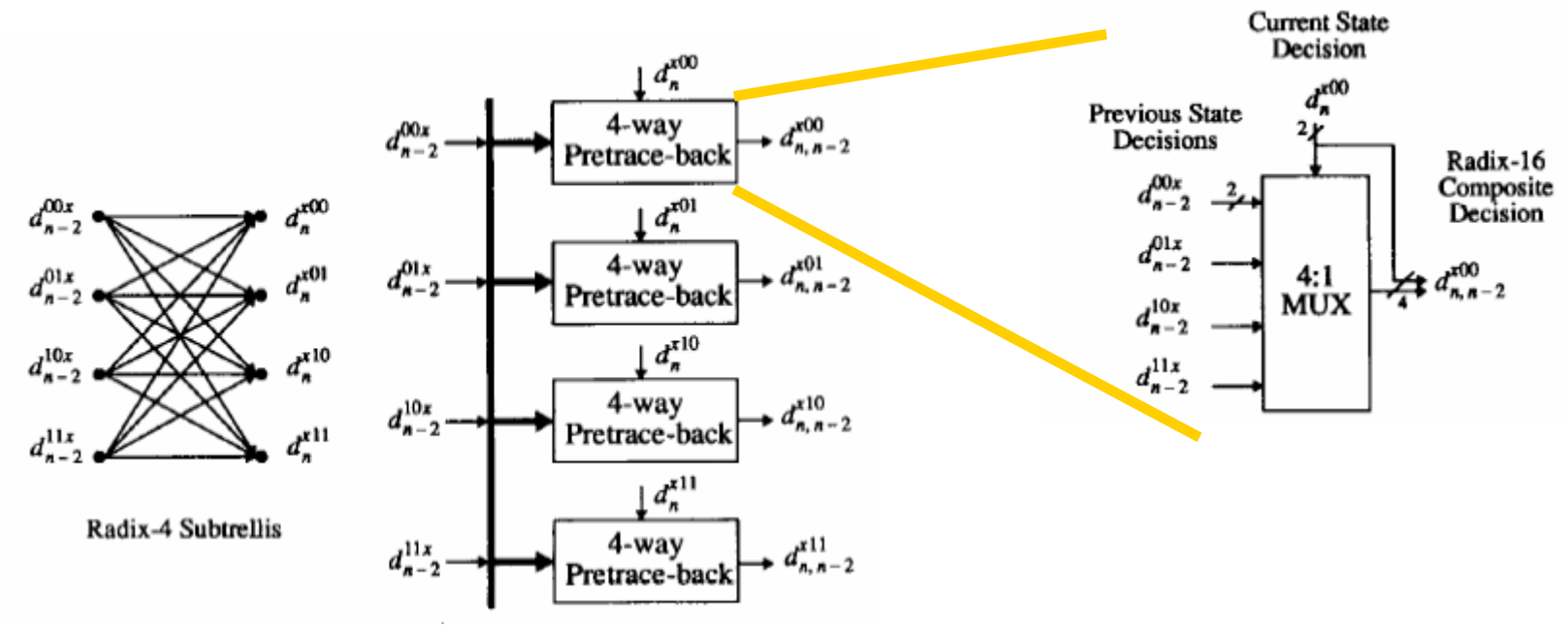


Figure from from Black, P. J., and T. H. Meng. "A 140-Mb/s, 32-state, Radix-4 Viterbi Decoder." *IEEE Journal of Solid-State Circuits* 27 (1992): 1877-1885. Copyright 1992 IEEE. Used with permission.

- The size of decision memory is unchanged
  - 4b decisions stored for each state, for every other radix-4 ACS computation (Radix-16 trace-back)
  - 2b decisions stored for each state, for every radix-4 ACS computation (Radix-4 traceback)

Trace-back unit implementation

- To match the ACS throughput, for radix-2^k trellis
  - Need L/k trace-back recursions per ACS iteration
    - L is the survivor path length
  - For every ACS iteration need to trace-back the whole survivor path of length L (L/k steps in radix-2^k trellis)
- Example (32-state, radix-4 => L=32, k=2)
  - Trace-back recursion rate (TRR) is 16 per ACS iteration
    - Problem since typically can't do more than 2 reads/cycle
    - TRR=1/2(1+L/D)

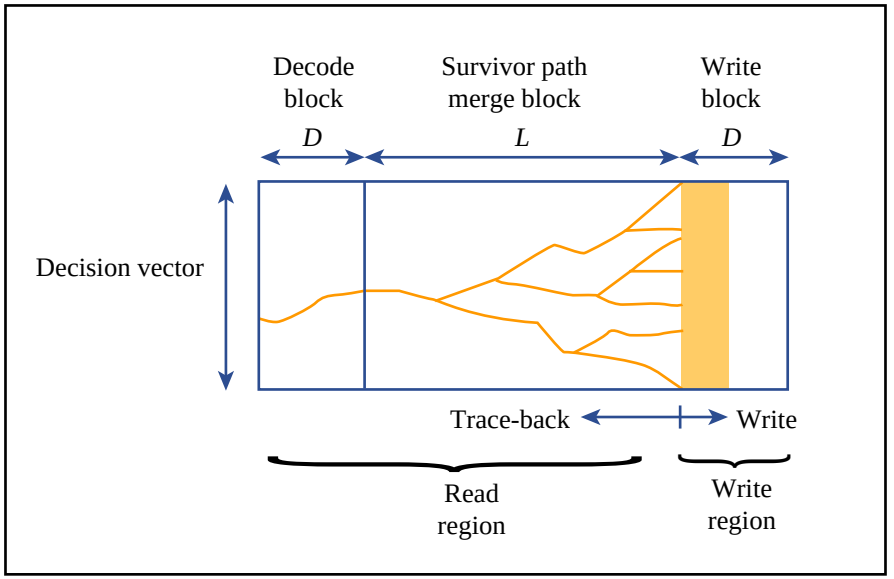
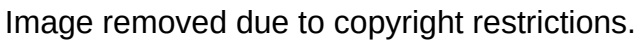


Figure by MIT OpenCourseWare.

For L=D and memory of length L and pretrace-back, TRR=1 and can use single-ported decision memory

Trace-back implementation



- For radix-2 survivor path length is L=32 (for 32 state trellis)
  - L=16 for radix-4 and L=8 for radix-16 (pretrace-back)
  - Hence total memory length is 3*8=24 in radix-16 case

Trace-back algorithms [3]

- k-pointer even (k read pointers and 1 write pointer)
  - 2k number of banks
  - T trace-back length
  - N number of states
  - T/(k-1) columns/bank
  - Example k=3
- Need to reorder dec bits
  - Use LIFO (two stack)
- Overall latency
  - 2kT/(k-1)

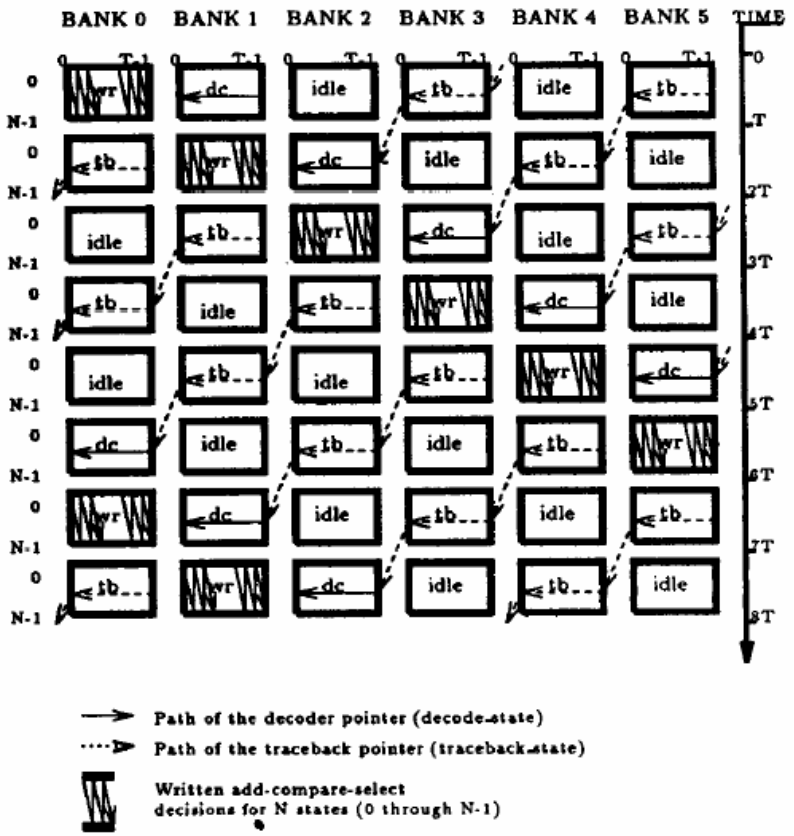
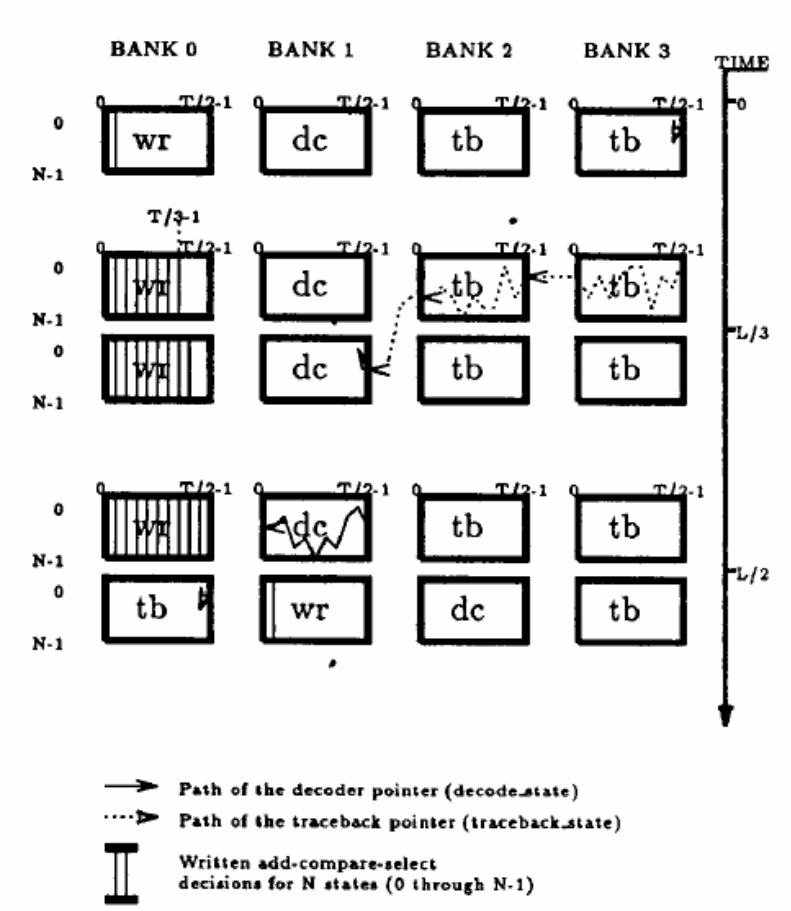


Figure from Feygin, G., and P. G. Gulak. "Survivor Sequence Memory Management in Viterbi Decoders." *IEEE International Symposium on Circuits and Systems* 5 (1991): 2967-2970. Copyright 1991 IEEE. Used with permission.

- Allows same speed reads and writes

Trace-back algorithms

- 1-pointer (1 read pointer and 1 write pointer)
  - k reads per 1 write
  - K+1 memory banks
  - T trace-back length
  - N number of states
  - T/(k-1) columns/bank
  - Read k-1 banks, decode 1
    - Decoding in bursts
  - Example k=3
- Need to reorder dec bits
  - Use LIFO (two stack)
  - Also takes care of bursts
- Overall latency
  - (k+1)T/(k-1)



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- More efficient for all except fully parallel ACS schemes

A little math [2]

- Can generalize these k-pointer schemes for different read, write and decode times (W, T, R)
- Need to follow some rules
  - Immediately after colliding with the write pointer, each read pointer traces back X columns (X-survivor path length) and then decodes values from B columns. Then it collides again with write pointer and repeats the procedure.
  - Write pointer always collides with read pointer in the same order. Between collisions it writes out exactly B columns
  - Write pointer stores the pointers for trellis stage 0 in column 0 at time 0

A little math

- Can calculate the total number of columns (S) as a function of k, X, W, T, R
  - Consider a single read pointer (between collisions with write pointer, it traces back X columns and decodes B columns, while write pointer writes kB columns

$$XT + BR = KBW$$

$$B = TX/(KW - R)$$

$$KW > R$$

$$i(KW - R) = TX$$

  - Number of columns S given by the number of columns traversed by single read and write pointer between collisions

$$S = (X + B) + KB$$

$$S = X + (K + 1)B = (1 + \frac{(K + 1)T}{KW - R})X$$

Discussion

- Let's see what this formula means

$$S = X + (K+1)B = (1 + \frac{(K+1)T}{KW - R})X$$

  - When k=1, constraint kW>R forces W>R and single-speed implementation is impossible
  - With k=3, W=R=T get familiar S=2k/(k-1)X
  - With k=1, W=8R=8T, S=9/7X [5]
    - For 64-state trellis, X~30, so S=40 will work

example	K	W	T	R	memory size
1	2	1	1	1	$4X$
2	3	1	1	1	$3X$
3	4	1	1	1	$\frac{8}{3}X$
4	5	1	1	1	$\frac{5}{2}X$
5	2	2	1	1	$2X$
6	2	4	1	2	$\frac{3}{2}X$

Readings

- [1] C. Rader "Memory Management in a Viterbi Decoder," *Communications, IEEE Transactions on [legacy, pre - 1988]* vol. 29, no. 9, pp. 1399-1401, 1981.
- [2] R. Cypher and C.B. Shung "Generalized trace back techniques for survivor memory management in the Viterbi algorithm," *Global Telecommunications Conference, 1990, and Exhibition. 'Communications: Connecting the Future', GLOBECOM '90., IEEE*, pp. 1318-1322 vol.2, 1990.
- [3] G. Feygin and P.G. Gulak "Survivor sequence memory management in Viterbi decoders," *Circuits and Systems, 1991., IEEE International Sympoisum on*, pp. 2967-2970 vol.5, 1991.
- [4] P.J. Black and T.H. Meng "A 140-Mb/s, 32-state, radix-4 Viterbi decoder," *Solid-State Circuits, IEEE Journal of* vol. 27, no. 12, pp. 1877-1885, 1992.
- [5] M. Anders, S. Mathew, R. Krishnamurthy and S. Borkar "A 64-state 2GHz 500Mbps 40mW Viterbi accelerator in 90nm CMOS," *VLSI Circuits, 2004. Digest of Technical Papers. 2004 Symposium on*, pp. 174-175, 2004.