MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Sciences

Analysis and Design of Digital Integrated Circuits (6.374) - Fall 2003 Quiz #2
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Student Name: _____

Problem 1 (30 Points): _____

Problem 2 (24 Points): _____

Problem 3 (22 Points): _____

Problem 4 (24 Points): _____

Total (100 Points): _____

For the entire quiz, ignore body effect (γ=0) and leakage effects. Also assume that all NMOS device bulks are connected to 0V and PMOS well terminals are connected to V_{DD}.

STATE ANY ASSUMPTIONS YOU MAKE IN SOLVING PROBLEMS and SHOW YOUR WORK

There are 13 pages in total

Problem 1: Carry Skip Adder: In this problem, we will explore the addition of two numbers based on the Carry Skip (or Carry Bypass) technique.

a) Consider the following 16-bit Carry Skip Adder. Assume that the Sum Logic (SL) block for stage *i* has as inputs P_i, G_i, and $C_{in,i}$. Assume the following delays:

- Delay to produce the P_i, G_i signals from the A_i, B_i inputs is 1 (i.e., the delay of the PG_L block)
- Delay to compute C_{out_i} from P_i, G_i and $C_{in,i}$ inputs is 1 (i.e., the delay of the Carry Logic (CL) block)
- Delay to compute S_i from $C_{in,i}$, P_i, G_i being valid is 2 (i.e., the delay of the Sum Logic (SL) block)
- Delay for the 2:1 multiplexor is 2
- Delay to compute the group propagate, GP_i, is 1 (assume for the entire problem that this delay is independent of the fan-in)

Highlight the critical path for this 16-bit adder directly on Figure 1 **(4 points)**

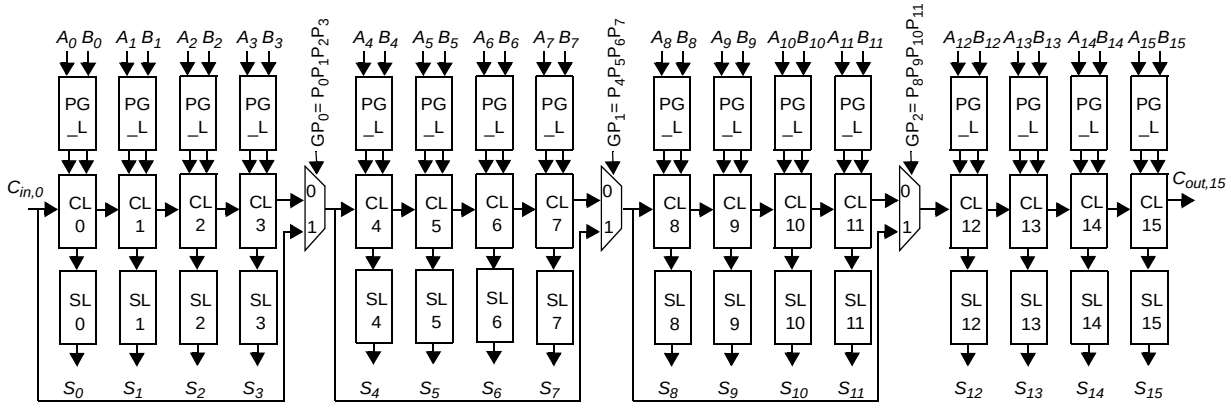


Figure 1: A 16 bit Carry Skip Adder with a block size M = 4.

(b) What is the delay for a 32-bit adder assuming equal block sizes of 4 and making the same assumptions of delay as 1 (a)? **(4 points)**

(c) Consider an *N*-bit Carry Skip adder with equal block sizes of *M*-bits. With the same timing assumptions of 1(a), derive the optimum block length *M*, for an *N*-bit adder. **(6 points)**

(d) Consider a transmission gate implementation of a 4-bit Carry-Skip section. Derive the signals S_1, S_2, and S_3 as a function of P_i and G_i. Will this circuit work if $P_i = A + B$? Explain. **(8 points)**

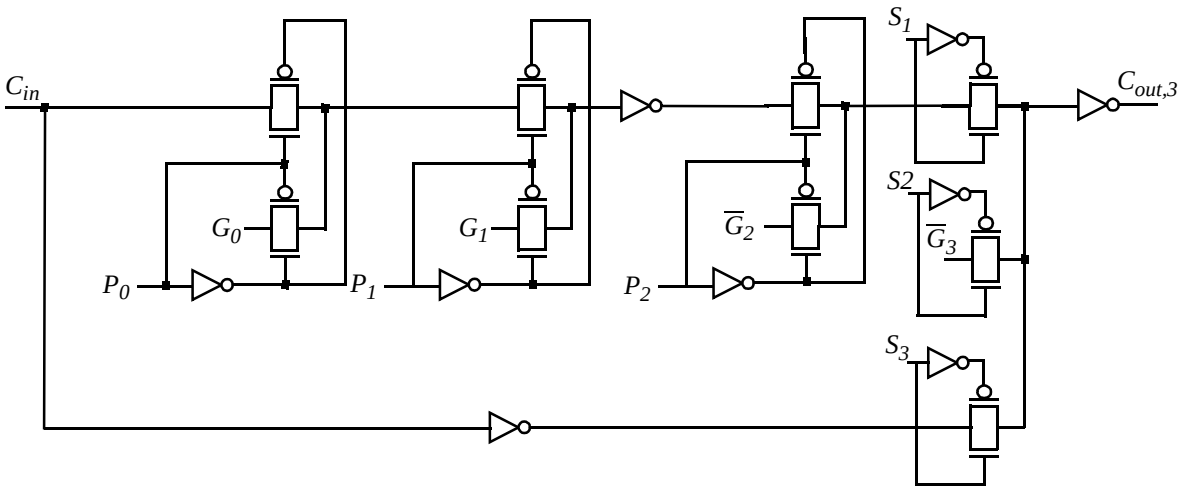


Figure 2: A transmission gate implementation of a 4-bit Carry Skip section.

(e) Consider the following 32-bit adder variation where the block sizes of each stage are not equal. Highlight the critical path directly on Figure 3. What is the delay of the critical path? **(8 points)**

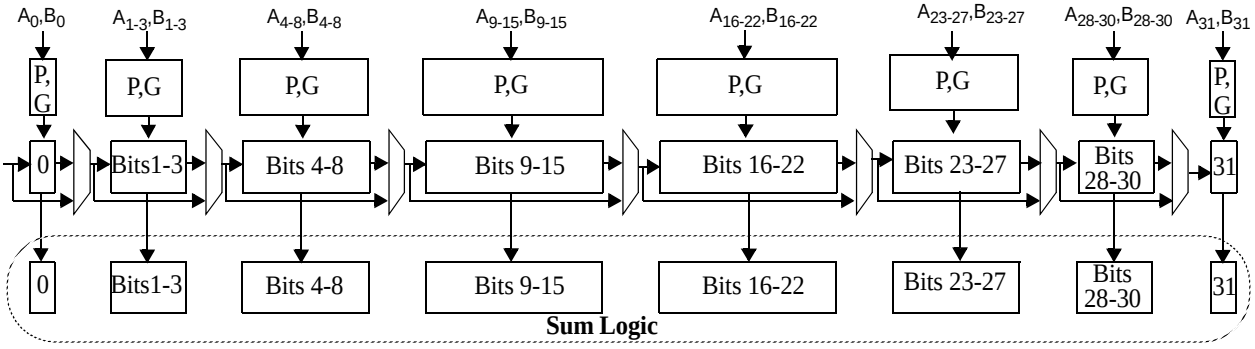


Figure 3: A 32-bit Carry Skip Adder with a variable block size.

Problem 2: Sequential Element: Consider the following circuit. Assume that each inverter takes 1 time unit for a *low-to-high* or *high-to-low* transition. Assume that it takes 1 time unit for a pull-up path or pull-down path to pull-up or pull-down, respectively. Ignore any leakage effects. Assume $V_{DD} >> V_T$. Also assume that there is no skew between *CLK* and $\overline{CLK}$ and assume that the rise/fall times on all signals are zero.

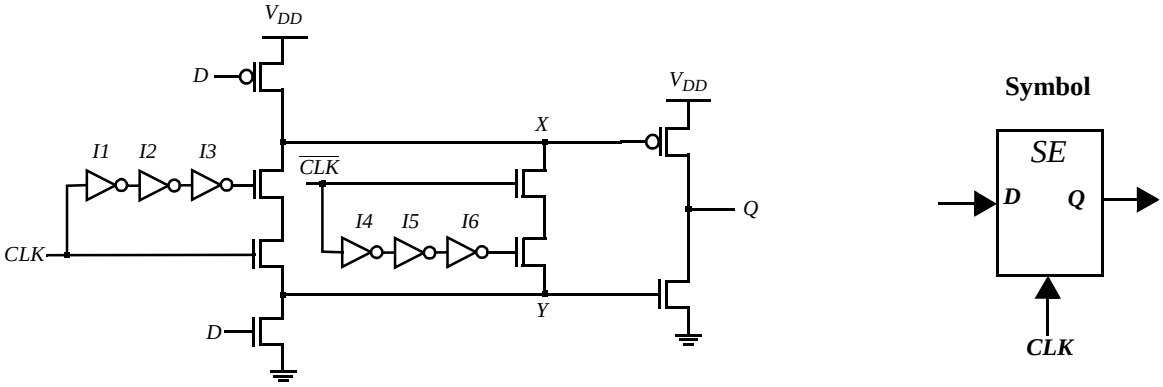
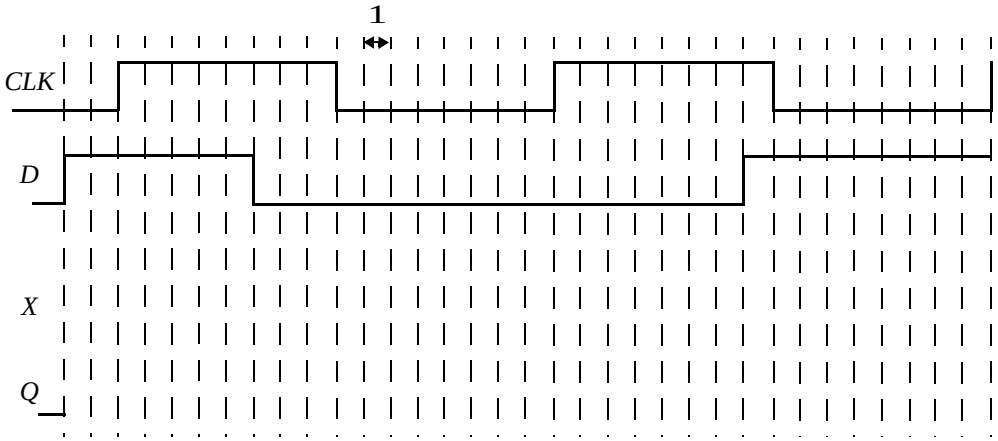


Figure 4: Sequential Element.

(a) Complete the timing diagram below. What type of sequential element is the above circuit? Be specific. **(8 points)**



(b) What is the setup time, t_{su}, hold time, t_{hold} and propagation delay, t_p of this sequential building block relative to the appropriate edge(s)? Explain. **(6 points)**

(c) Consider the following simple sequential system built using the sequential element in Figure 4. Assuming that there is no skew in distributing the clock, what is the **minimum possible clock period** for which this sequential system will function? Assume that the primary input *In* is setup before the appropriate clock edge(s). **(6 points)**

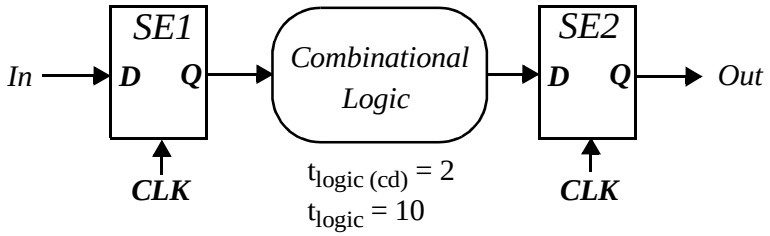


Figure 5: Simple Sequential System.

(d) What is the maximum positive skew on the clock to SE2 such that the circuit still functions? **(4 points)**

Problem 3: Sequential Circuit: Consider the following circuit. Assume that each inverter takes 1 time unit for a *low-to-high* or *high-to-low* transition. Also assume that it takes 1 time unit for a pull-up path or pull-down path to pull-up or pull-down, respectively. Assume that ratioed circuits are properly sized (i.e., assume that the devices in the cross-coupled inverters are weak and can be overpowered). Assume that the rise/fall times on all signals are zero.

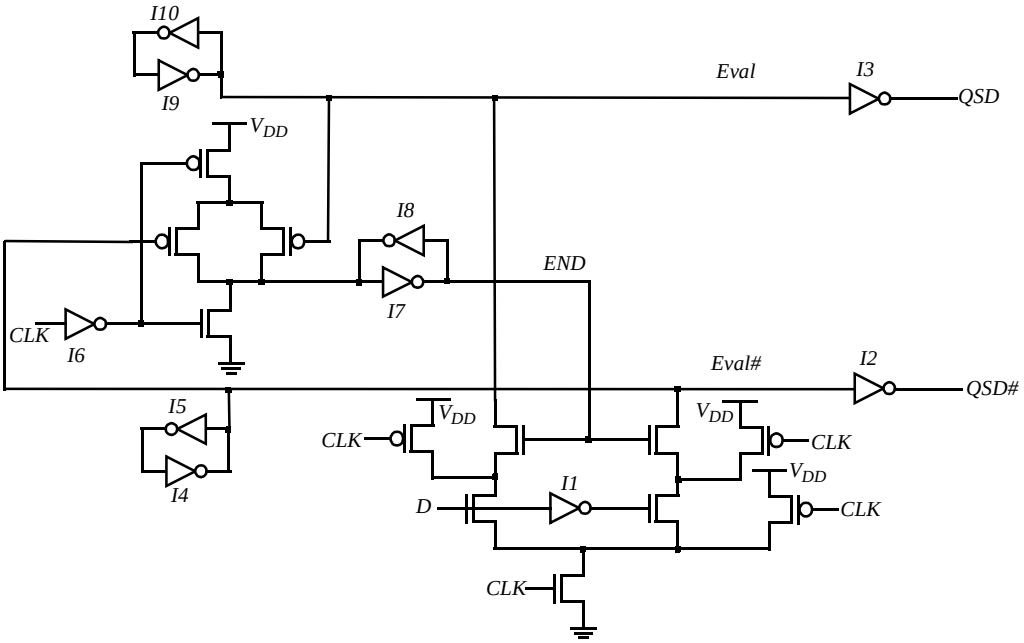
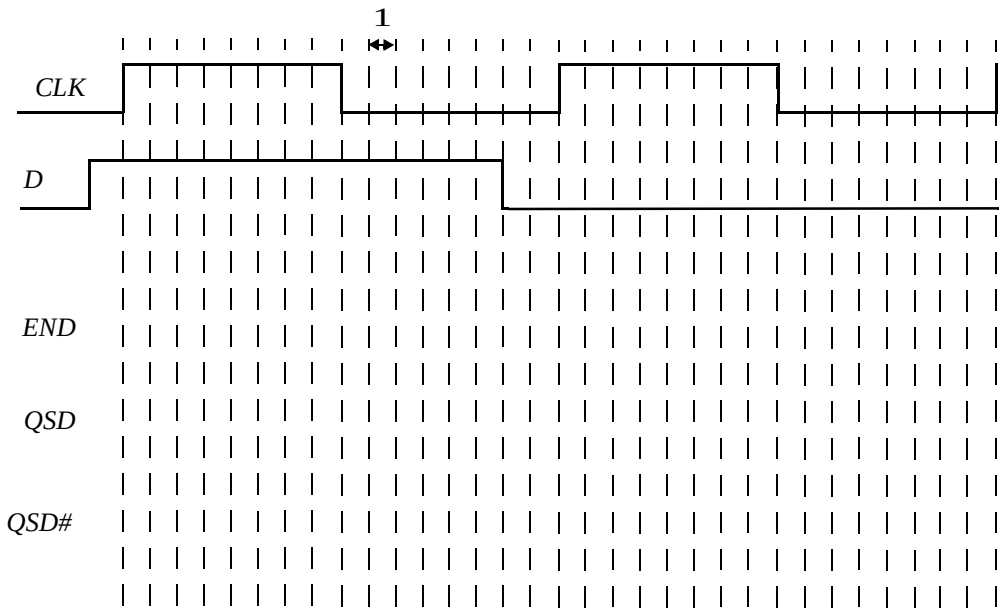


Figure 6: Sequential Circuit.

(a) Complete the following timing diagram for *QSD, QSD#, END*. **(8 points**)



(b) Assuming that the circuit of Figure 6 directly drives a dynamic DCVSL gate (i.e., differential N-type dynamic logic clocked by *CLK*), what is the setup time of the circuit in Figure 6 relative to the appropriate clock edge? Explain. **(4 points)**

(c) What is the hold time, t_{hold} and propagation delay, t_p, of the circuit in Figure 6 relative to the appropriate clock edge? **(4 points)**

(d) Consider the following sequential implementation which includes both differential dynamic logic and static logic. The circuit below has a major problem. Identify the problem and propose a solution (draw a gate level schematic). **(6 points)**

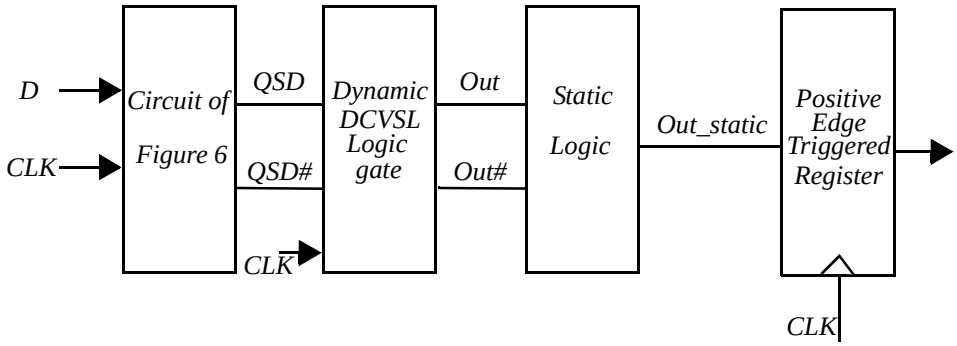


Figure 7: Sequential System.

Problem 4: Interconnect Issues: For this entire problem assume $C_I/C_L = 5$. (C_I is the interwire capacitance and C_L is the line capacitance to the substrate). An inverter is modeled using resistors and an ideal switch. The switch is connected either to the top resistor or the bottom resistor.

(a) Consider the 2-line bus shown in Figure 8. Compute the **total** energy drawn from the power supply V_{DD} for the transition of (In_0, In_1) from 01 to 10. **(6 points)**

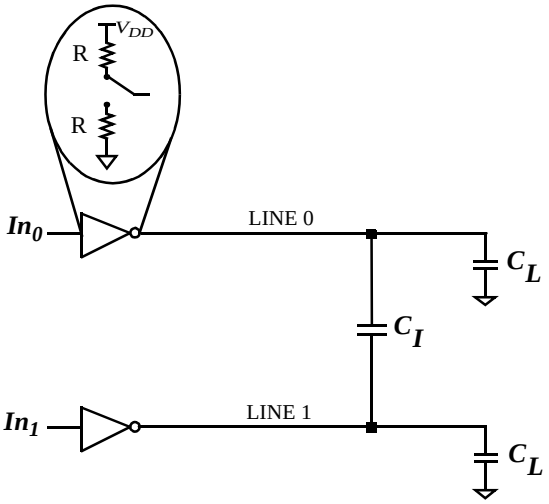


Figure 8: 2-bit bus.

(b) Consider the following modification in which the inverters are replaced by tri-state inverters. When the enable signal *En* is low, the tri-state does not drive the LINE. In addition, a switch with a small resistance R is added in parallel with C_I which is closed when the control signal $S = 1$. Consider the same transition as 4(a) in which (In_0, In_1) switches from 01 to 10. However, before the transition happens, the switch is shorted and then opened. Assume that the time period when the switch is closed is long enough for all the transients to settle. Compute the **total** energy drawn from the power supply V_{DD}. **(8 points)**

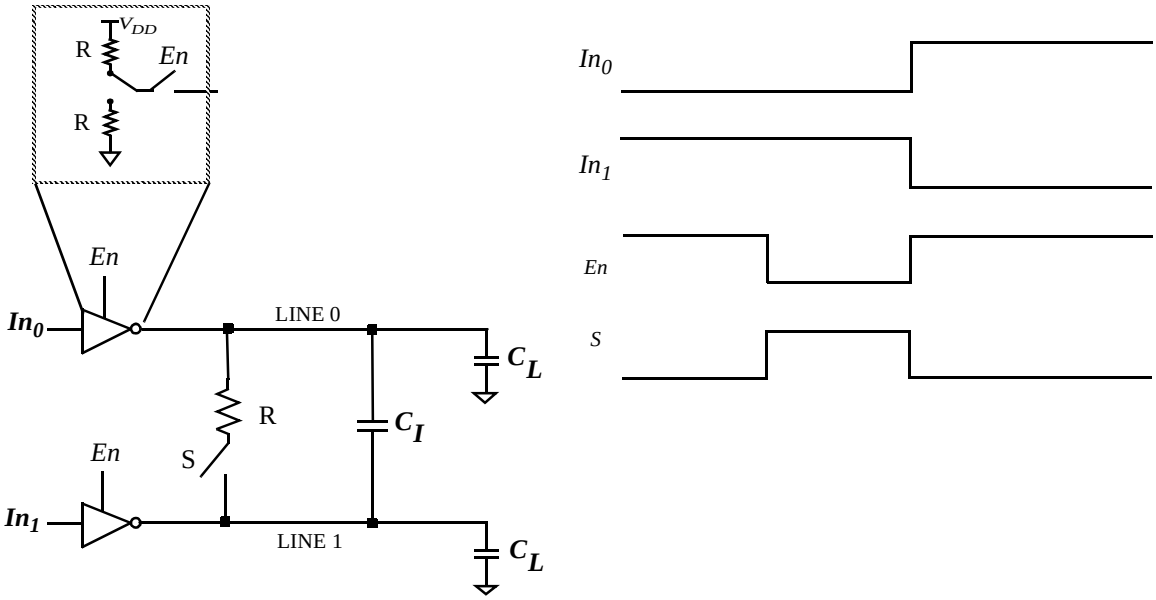


Figure 9: Modified driving scheme for a 2-bit bus.

(c) Consider the following input sequence, which represents all the possible transitions for 2 input bus.

Transition Sequence: 00→00→01→10→11→00→10→10→01→11→01→01→00→11→11→10→00

What is the **difference** in energy drawn from the power supply for the above sequence using the approach in 4(b) vs. 4(a). For the scheme in part 4 (b), assume that you may choose on a transition by transition basis if the switch should be closed before the transition happens. If the switch is closed between transitions, assume that the tri-state driver is off during that period. **(10 points)**