MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Sciences

Analysis and Design of Digital Integrated Circuits (6.374) - Fall 2003 Quiz #1
Prof. Anantha Chandrakasan

Student Name: _____

Problem 1 (30 Points): _____

Problem 2 (24 Points): _____

Problem 3 (18 Points): _____

Problem 4 (28 Points): _____

Total (100 Points): _____

Use the following device parameters unless otherwise specified:

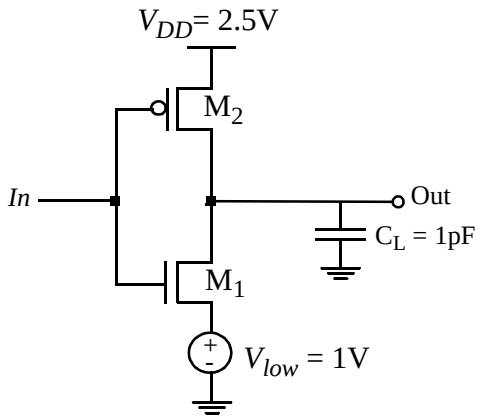
Parameter	NMOS	PMOS
V_{T0}	0.4 V	-0.4V
$K' = \mu C_{ox}$	75 $\mu A/V^2$	-25 $\mu A/V^2$
V_{DSAT}	0.5V	-0.75V
γ	$0.3V^{1/2}$	$-0.3V^{1/2}$
$\|2\varphi\|$	0.6V	0.6V
λ	0	0

Also assume that all NMOS device bulks are connected to 0V and PMOS well terminals are connected to V_{DD}.

STATE ANY ASSUMPTIONS YOU MAKE IN SOLVING PROBLEMS and SHOW YOUR WORK. Points might be taken off if you don't explain how you arrived at your answer.

There are 13 pages in total

Problem 1: Driver Circuit: Consider the following circuit driving a capacitive load of 1pF.



(a) Assuming that *In* swings from rail-to-rail (0 to 2.5V), what is the swing on the node *Out*? **(2 points)**

(b) At the switching threshold V_M = 1.75V, what is the mode of operation for M_1 and M_2. Show your work **(4 points)**

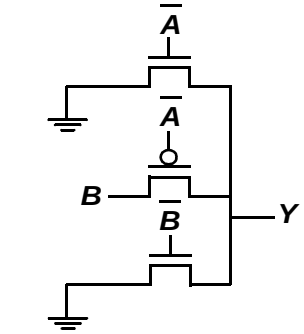
(c) Assuming $(W/L)_2$ = 25µm/0.25µm, determine $(W/L)_1$ such that V_M = 1.75V. (**6 points**)

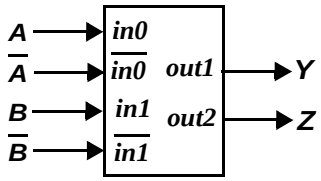
(d) Assuming $(W/L)_2 =$ 25µm/0.25µm, determine the low-to-high propagation delay using the method of equivalent RC. Assume that the input switches from 2.5V to 0V with a zero fall time **(8 points)**

(e) Assuming that the input switches at a clock frequency of 100MHz with a swing of 0 to V_{DD} (with zero rise and fall times) what is the average power dissipation of this circuit? Show your work **(10 points).**

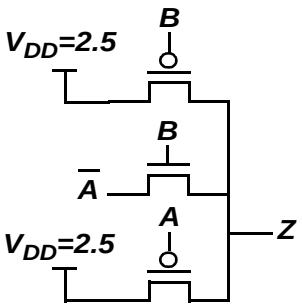
Problem 2: Pass Transistor Logic

(a) Consider the following circuit implemented using NMOS and PMOS pass transistors. Assume that the inputs and their complements (A, $\overline{A}$, B, $\overline{B}$) swing rail-to-rail (0 to V_{DD}). What is the function implemented by the two circuits. **(6 points)**



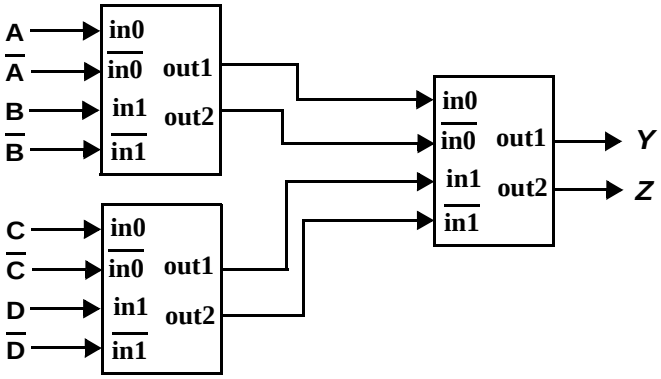


Y =



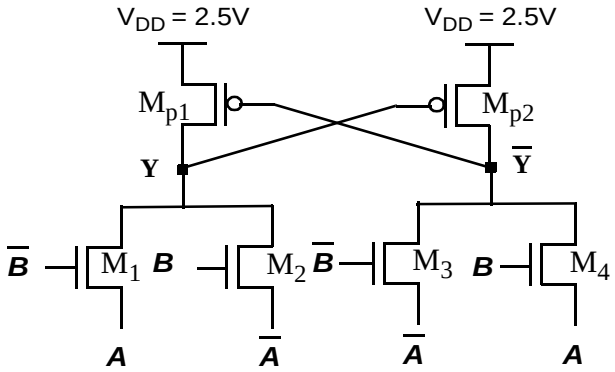
Z =

(b) Assuming that the primary inputs (A, B, C, D) and their complements are have rail-to-rail swing (0 to V_{DD}), what is the voltage swing on outputs Y and Z? **(4 points)**



(c) Using the same style of logic in part 2(a) (i.e., using NMOS, PMOS pass transistors connected to signal or V_{DD}/ GND), create the minimal transistor implementation of the OR/NOR function. Your implementation should have the same swing as the circuits in 2(a) **(6 points)**

Consider the following cross-coupled complementary pass-gate logic

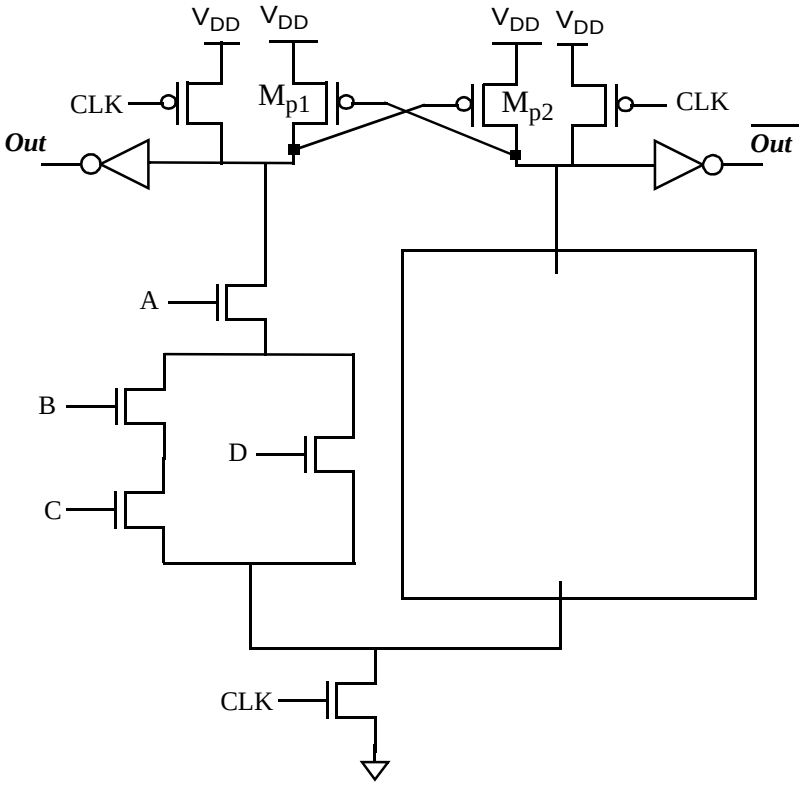


(d) What is the logic function Y implemented by the above gate? What is the voltage swing on nodes Y and $\overline{Y}$?
(4 points)

(e) Assume that A, $\overline{A}$, B, $\overline{B}$ are from ideal voltage sources and have a rail-to-rail swing (0 to V_{DD}). Also assume (just for this part) that there is no body effect ($\gamma = 0$) and ignore sub-threshold conduction. Is this a ratioed circuit? Explain.
(4 points).

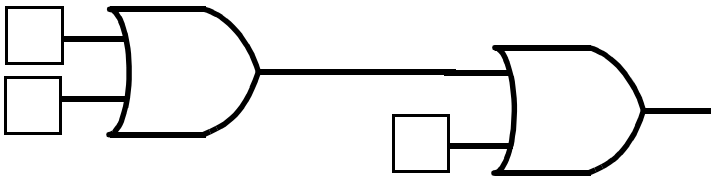
Problem 3: Dynamic Logic

(a) Complete the circuit schematic of the DCVSL gate below **(6 points)**



(b) What is the function of M_{p1} and M_{p2}? Is this a ratioed circuit? **(4 points)**

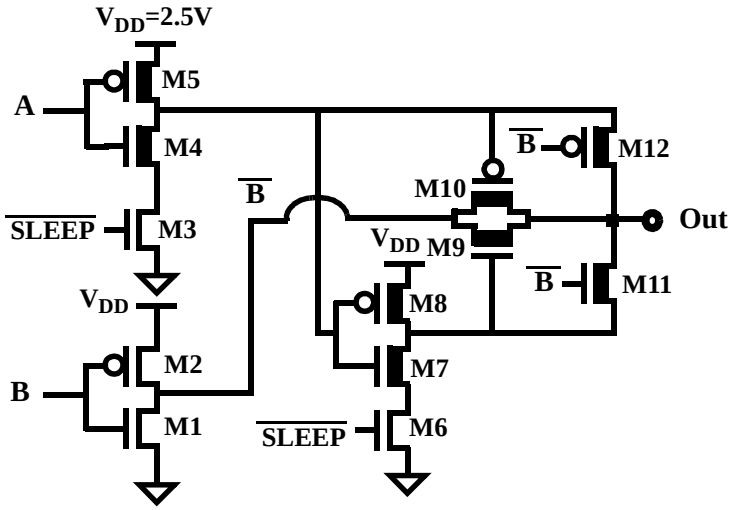
(c) Consider the following function Y= A+ B+ C implemented using a cascade of two 2-input DOMINO OR gates. Assume that $p_{(A=1)} = 0.1$, $p_{(B=1)} = 0.2$, $p_{(C=1)} = 0.5$. Determine the order of inputs to minimize power dissipation (show numerical analysis). Explain. Fill in the empty boxes with the appropriate inputs. **(8 points)**



Problem 4: Multiple Threshold CMOS Circuits: This problem explores issues related to leakage in MTCMOS circuits. **Just for this problem**, assume that the low threshold NMOS and PMOS devices have the following device properties (ignore DIBL). All low-V_T and high-V_T devices are 1µm/0.25µm.

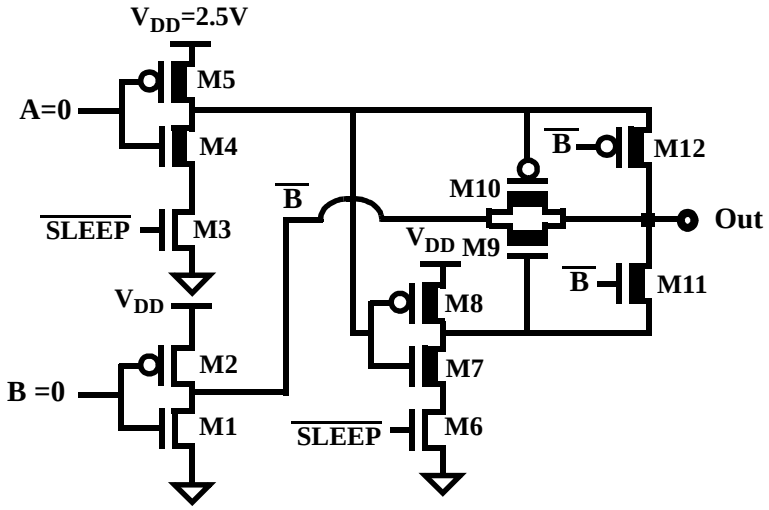
Parameter	NMOS	PMOS
V_{Tlow}	0.3V	-0.3V
V_{Thigh}	0.5V	-0.5V
$\|I_o\|$ for a 1µm/0.25µm Device (Drain current when $V_{GS}=V_T$)	1µA	1µA
|S| (Sub-threshold slope)	100mV/Decade	100mV/Decade

Consider the circuit shown below (**low threshold devices are shaded**).

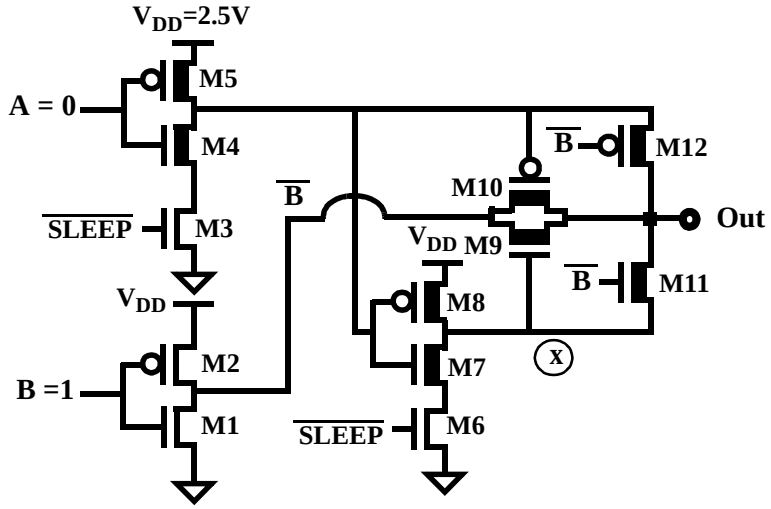


(a) During active mode (SLEEP = 0), provide the logic function for *Out* (**4 points)**

(b) Assuming SLEEP = 0 (Active mode), compute the total leakage when A=0, B=0? **A numerical result is expected**. Draw all the contributing leakage paths on the figure below **(10 points)**



(c) Assuming SLEEP = 1 (Sleep mode) and A=0, B=1. In the Sleep mode, ideally, the leakage should be small and be set by high-threshold devices. Unfortunately, this is not always the case for distributed sleep devices as shown below. Identify **(but do not compute)** any leakage path(s) from V_{DD} to ground which are determined by low-threshold devices (i.e., not cut-off by high-threshold devices). **(8 points)**



(d) For the same assumption of part (c), what do you expect the leakage through device M9 to be:

(1) 10pA
(2) 1nA
(3) >> 1nA

Briefly explain why (**6 points**)