MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

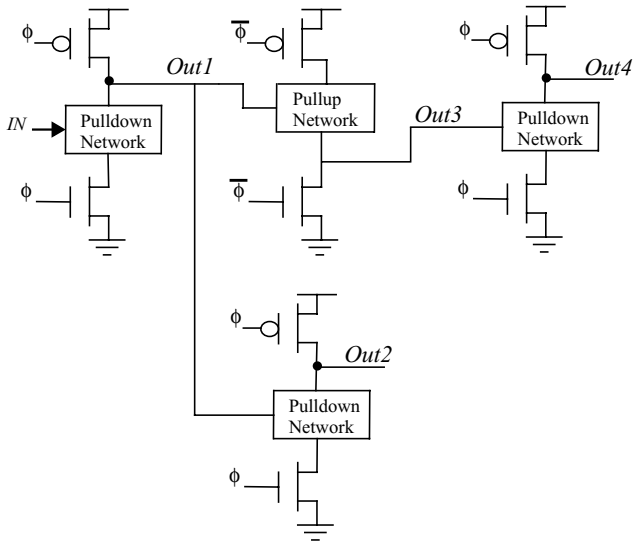
6.374: Analysis and Design of Digital Integrated Circuits
Problem Set # 3 Solutions

Fall 2003 Issued: 10/14/03

For these problems you can use the process parameters for the 0.25 technology- see the Process Parameters file in the assignments section.

Problem 1: Dynamic Logic I

Consider the conventional N-P CMOS circuit below in which all precharge and evaluate devices are clocked using a common clock ϕ and its complement. For this entire problem, assume that the pulldowown/pullup network is simply a single NMOS/PMOS device, so that each Domino stage consists of a dynamic inverter followed by a static inverter. Assume that the precharge time, evaluate time, and propagation delay of the static inverter are all *T*/2. Assume that the transitions are ideal (zero rise/fall times)



a) Do any problems occur when the input makes a 0->1 transition? What about a 1->0 transition? If so, describe what happens and insert one inverter somewhere in the circuit to fix the problem.

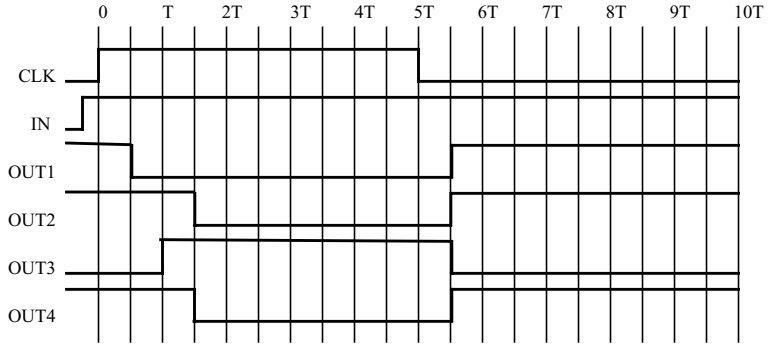
Solution

There is no problem if the input makes a 1->0 transition, as long as the input is stable when the evaluate phase begins. However, if the input makes a 0->1 transition, *Out1* will initially be precharged to 1 and then go to 0 at some time after the evaluate phase begins. In our case this time is T/2. This could allow the next

PDN to pull *Out2* low before Out1 goes low and cause an error in Out2. Insert the inverter before the PDN generating *Out2* to solve the problem.

b) For your corrected circuit, complete the timing diagram for signals Out_1, Out_2, Out_3 and Out_4, when the *IN* signal goes high before the rising edge of the clock ϕ. Assume that the clock period is 10 T time units

Solution



b) Suppose that there are no evaluate switches at the 3 latter stages. Assume that the clock ϕ is initially in the precharge state (ϕ=0 with all nodes settled to the correct precharge states), and the block enters the evaluate period (ϕ=1). Is there a problem during the evaluate period, or is there a benefit? Explain.

Solution

There is no problem during the evaluate stage. The precharged nodes remain charged until a signal propogates through the logic, activating the pull-down network and discharging the node. In fact, this topology improves the circuit's robustness in terms of charge sharing affecting the output for any generic pull-down network, and reduces the body effect in the pull-down network.

c) Assume that the clock ϕ is initially in the evaluate state (ϕ=1), and the block enters the precharge state (ϕ = 0). Is there a problem, or is there any benefit, if the last three evaluate switches are removed? Explain.

Solution

There is a problem during the precharge stage. If all precharged nodes are discharged during the evaluate stage, when the precharge FETs simultaneously turn on, the pull-down networks will initially remain on, creating a short circuit. This continues in each gate until the previous gate charges, disabling its pull-down network.

Problem 2: Leakage Power

Consider the circuit shown below:

a) What is the logic function implemented by this circuit? Assume that all devices (M1-M6) are 0.5µm/0.25µm.

Solution

$\overline{(AB)+C}$

b) Let the drain current for each device (NMOS and PMOS) be 1μA for NMOS at $V_{GS}= V_{Tn0}$ and PMOS at $V_{GS}= V_{Tp0}$. What input vectors cause the worst case leakage power for each output value? Explain (state all the vectors, but do not evaluate the leakage). Ignore DIBL**.**

Solution

When the output is high, the worst-case leakage occurs when two transistors leak in parallel: ABC = 100 or 010. When the output is low, the worst-case leakage also occurs when two transistors leak in parallel: ABC =110.

c) Suppose the circuit is active for a fraction of time *d* and idle for *(1-d)*. When the circuit is active, the inputs arrive at 100 MHz and are uniformly distributed ($Pr_{(A=1)} = 0.5$, $Pr_{(B=1)} = 0.5$, $Pr_{(C=1)} = 0.5$) and independent. When the circuit is in the idle mode, the inputs are fixed to one you chose in part (b). What is the duty cycle *d* for which the active power is equal to the leakage power?

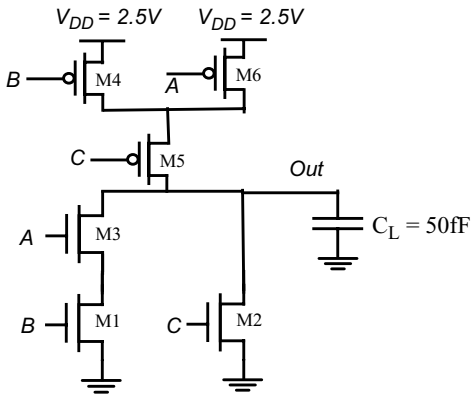
Solution

Choose the case where ABC=100.

$d*P_{active} = (1-d)\ P_{leakage}$. $P_{active} = \alpha_{0->1}*f*C_L*V_{DD}^2 = (3/8 * 5/8)*(100*10^6)*(50*10^{-15})*(2.5^2) = 7.3\,\mu$ W.

$P_{leakage}$ (ABC = 100) $= V_{DD}*2*I_{leakM1} = 5*I_o 10^{\frac{-V_T}{S}} = 5*1uA\,10^{\frac{-0.43}{0.1}} = 251$pW.

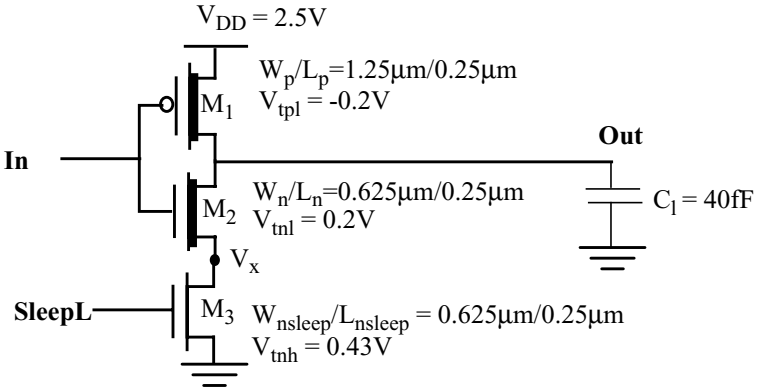
Plugging the power numbers into the activity equation and solving for d gives $d = 3.4*10^{-5}$.



Problem 3: Multi Threshold CMOS

Multi Threshold CMOS is a circuit technique that utilizes multiple threshold devices to provide both low leakage and high performance operation. The following problem explores some of the issues involved in MTCMOS circuits, although a more realistic circuit would be more complicated (like an adder or multiplier) instead of the single inverter shown in Figure 1. For hand calculations, ignore body effect, lambda, and parasitic capacitances.

In the sleep mode, M3 is turned off, and this high Vt device limits the subthreshold leakage current. On the other hand, when the circuit is active, M3 is turned on hard for fast switching operation. For the rest of the



problem, assume that M3 is turned on. (i.e. $V_{SleepL} = V_{DD}$)

Parts a) through f) do not require HSPICE.

a) What is the desired region of operation for M3 during the active mode?

Solution

$(V_{GS} - V_t) > V_{DSAT} > V_{DS}$, therefore M3 is in the linear mode (i.e., M3 acts like a linear resistor).

b) Calculate the effective resistance looking into the drain of transistor M3.

Solution

The effective resistance is just the output resistance of M3 from its corresponding small-signal model:

$$G = \frac{\partial I}{\partial V_{DS}} = k_n' \frac{W_3}{L_3}(V_{GS} - V_t - V_{DS}) = 115\times10^{-6} \times \frac{0.625}{0.25} \times (2.5 - 0.43) = 595 \times 10^{-6} \qquad \text{and} \quad R = G^{-1} \text{ so}$$

R = 1680 Ω. Notice that we assumed the V_{DS} term was negligible. That may not be too valid, but it works for providing an approximation of R.

c) Now assume the effective resistance of M3 is 0. What is the peak current (saturation current) that discharges C_l during an output high to low transistion?

Solution

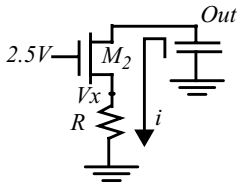
The peak discharge current with the effective resistance of M3 set to 0 is simply the initial discharge current through M2 when M2 is velocity saturated

$$I_{peak} = k_n' \frac{W_2}{L_2} \cdot V_{DSAT} \cdot (V_{GS} - V_t - 0.5 V_{DSAT}) = 115\times10^{-6} \cdot \frac{0.625}{0.25} \cdot 0.63 \cdot (2.3 - 0.315) = 360\mu A$$

d) What is the peak current taking into account the finite sleep resistance (computed in part b)

Solution

With a non-zero effective resistance the voltage at Vx becomes a function of the discharge current and we need to take this into account when determining the peak discharge current**.**



$$V_x = iR = 1680i$$

$$i = k_n'\left(\frac{W}{L} \cdot V_{DSAT} \cdot (2.5 - V_x - V_t - 0.5V_{DSAT})\right)$$

Solving for *i* and V_x , V_x = 0.41V, *i* = 244μA.

e) As W_{nsleep} increases, qualitatively how does t_{PHL} vary? How does t_{PLH} vary?

Solution

t_{PHL} *decreases*,because average current gets bigger. t_{PLH} *is unaffected*

f) If there is a large parasitic capacitance at node Vx, what is the effect on switching performance?

Solution

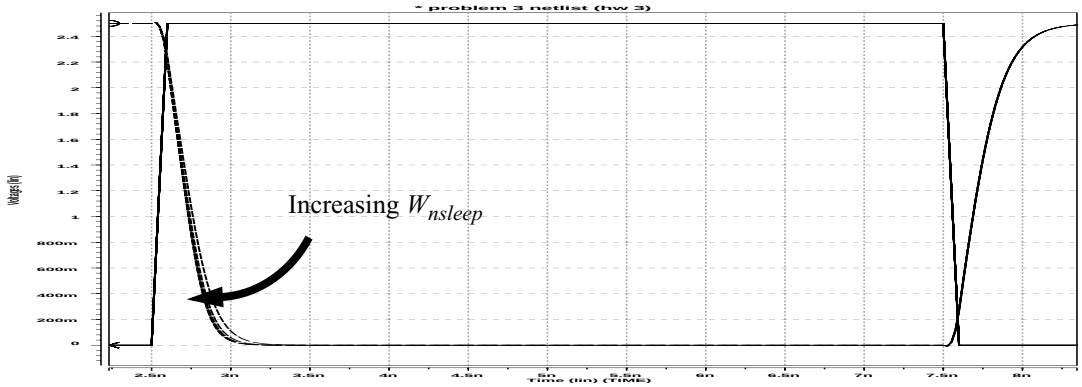
The switching performance improves (i.e., t_{PHL} decreases) if there is big capacitance at x. This is because the average current gets larger. If there's a capacitance at node x then the discharge current entering node x sees a first order RC circuit and as a result Vx increases slowly. This results in a larger $V_{GS,M2}$ which results in a larger peak current (another way to think about this is to consider the large parasitic capacitor at Vx as a local sink for the charge from *Out*). The larger the value of the capacitor, the more slowly that Vx will charge and hence the smaller t_{PHL} becomes.

For Hspice simulations use the models' file "logiclvt.l". Include two .lib statements, one with
TT and one with TT_LVT and use nchlvt, pchlvt, and nch as the three device types in your netlist

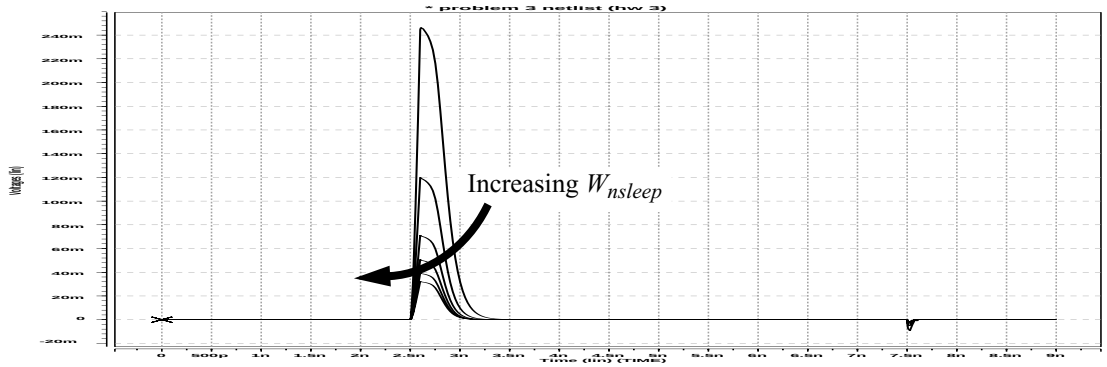
g) Using HSPICE, simulate the circuit for varying Wnsleep values of (0.625, 1.5u, 3u, 5u, 7u, 9u, 11u). Turn in plots showing output voltage as a function of time and Vx as a function of time (with the varying Wnsleep curves superimposed on the same graph). Note if done correctly, HSPICE need only be run once. For the input specification, use the piecewise linear option: "Vin node1 node2 pl 0v 0n, 0v 2.5n, 2.5v 2.6n, 2.5v 7.5n, 0v 7.6n".

Solution

Figure 2 shows the required plot generated by Hspice.



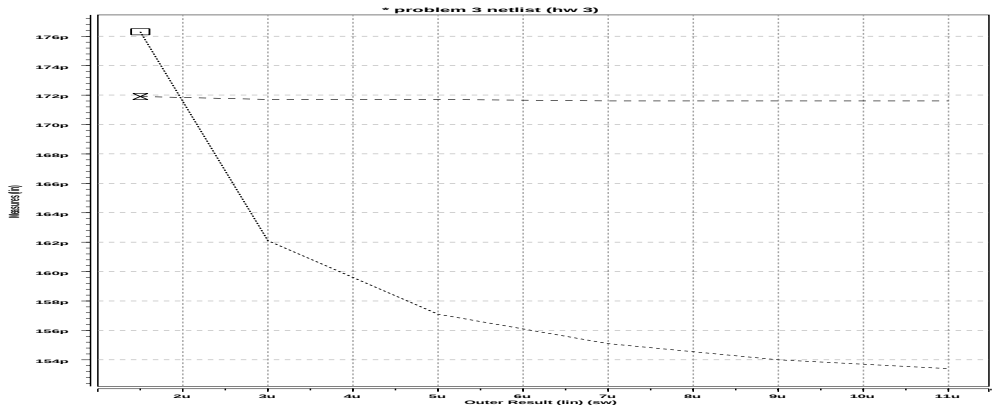
We can see from the above graph that (f) is verified. (i.e., as parasitic capacitance (W) gets bigger t_{PHL} decreases) Notice that our calculation for Vx overestimated the value. That is because we assumed Vx was



small enough to neglect when solving for R. In reality, that approximation caused us to underestimate the resistance.

h) Plot t_{PHL} and t_{PLH} for each of these choices of Wnsleep.

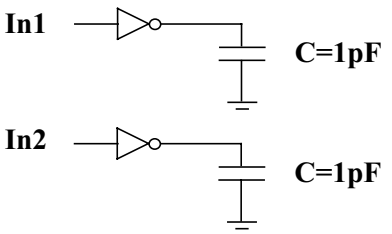
Solution



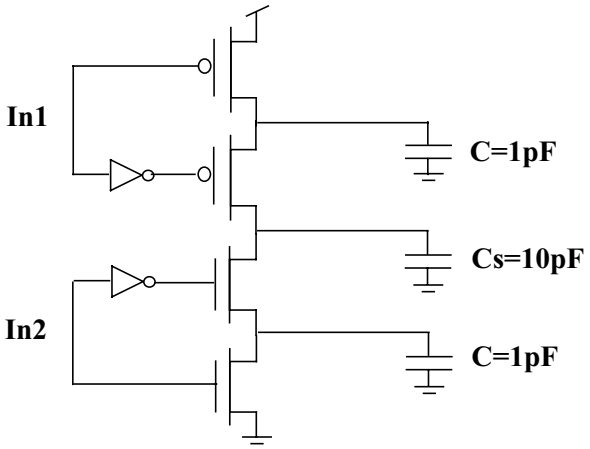
Problem 4: Low-Swing Bus Drivers

Consider the two possible bus driver circuits shown below:

Use 0.25 um technology: VDD=2.5 V



Circuit A



Circuit B

a) First consider circuit A. Assume an ideal inputs with zero rise time are available. Assuming Wp/Wn=3, find the minimum sized inverters such that tp will be less than 10% of the period for switching frequencies of 10 MHz, 100 MHz, and 1 GHz. (To make this easy, you can specify wn='0.375u*scale' and wp='1.125u*scale', specify the areas and perimeters similarly, and just vary the parameter 'scale'.) What is the leakage power consumed by inverters of each of these sizes when the input is low? What is the average total power consumed by the 2-bit bus if the inputs are tied together and switch at a frequency of 100 MHz? (For this very last question, just give a hand calculation based on switching power only and neglecting parasitics.)

Solution

Using HSPICE and parameterizing the device sizes in terms of the scale factor it is relatively easy to iterate and find a solution. We find that scale must be about 1 for 10 MHz operation, 7 for 100 MHz operation, and 80 for 1 GHz operation. The leakage currents/powers, measured by placing a zero volt test source between VDD and the PMOS device, are118 pA/295 pW, 18 pA/45 pW, and 8 pA/20 pW for the required scale factors. (These values for scale and resulting current/power are somewhat subjective The average power of the 2-bit bus can be found by the following method. Each time a capacitor charges from 0->VDD, the required charge is $Q=CV_{DD}$. For each of the two capacitors this will happen 100E6 times per second, so $I_{tot}=2*100E6*CV_{DD}$. Then multiply this by VDD since P=IV. The result is that the switching power for the bus is 1.25 mW.

b) Circuit B shows a simplified version of a purposed low-swing bus driver circuit. ["Low-swing charge recycle bus drivers" Karlsson, M.K.; Vesterbacka, M.; Wanhammar, L.; Circuits and Systems, 1998. ISCAS '98. Proceedings of the 1998 IEEE International Symposium on , Volume: 2 , 31 May-3 June 1998; Page(s): 117 -120 vol.2] Explain how this circuit works. Theoretically, what should be the percentage power saved by using this circuit instead of Circuit A?

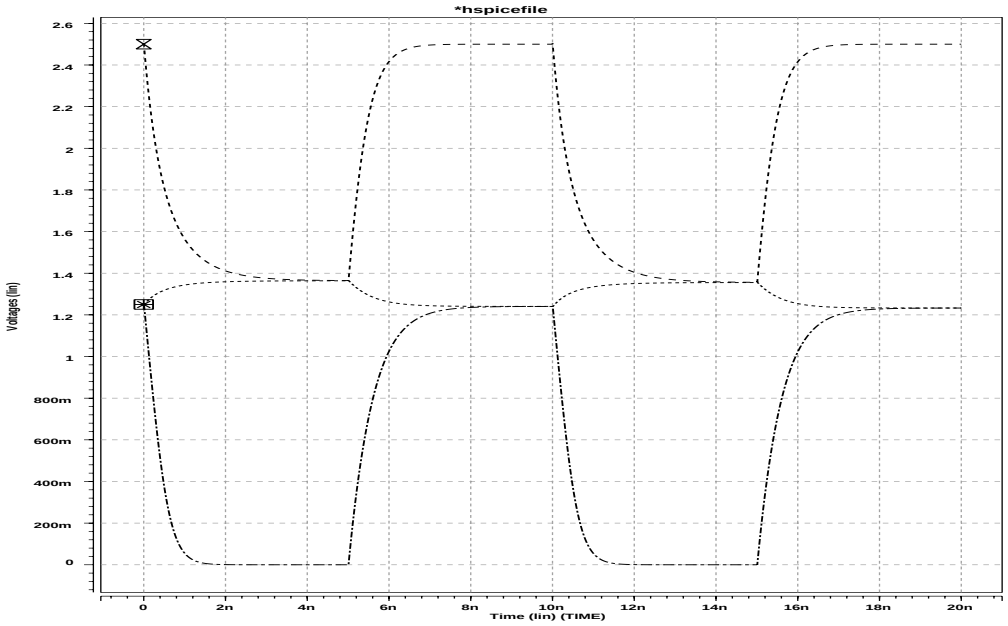
Solution

This circuit works by lowering voltage swing and recycling charge to conserve power. The large capacitor at the middle node acts as a virtual ground at VDD/2 which stores and reuses charge and each of the buses has a swing of VDD/2. The power can be calculated by recognizing that when the two buses make a simultaneous 0->1 transition, the only charge drawn from the supply is $Q=C\Delta V$, where ΔV is the change in voltage on the upper bus and is equal to $V_{DD}/2$. Then $I=100E6*C*\Delta V$ and $P=100E6*C*\Delta V*V_{DD}=50E6*C*V_{DD}^2$. This is a factor of 4 reduction in power or 75% savings.

c) Now simulate Circuit B with the inputs tied together and switching at 100 MHz. Size the NMOS and PMOS as above and with scale=10. Be sure to initialize Cs to VDD/2 using a .ic statement. In a real circuit you would probably need to use progressively scaled buffers, but for this case you may assume that you have IN1, IN2 and their complements available at the gate inputs with zero rise/fall times. (This means you DO NOT need to implement the two inverters at the input.) How much power do we actually save by using this low-swing driver? Submit your output waveform.

Solution

The output waveform is shown below. The power, found by averaging the current sourced by VDD, is 294 uW for Circuit B. This is approximately 76.5% percent savings from the theoretical power used by the simple dual inverter bus driver which matches well with the calculated result.



d) What problem might occur in Circuit B if the two inputs had different activity factors?

Solution

If the circuits two inputs had different activity factors the virtual ground capacitor would start to move away from VDD/2 until the circuit failed. For this reason, the actual circuit proposed in the paper has additional biasing circuitry to guarantee that the virtual ground node will remain within a predetermined voltage range.

Problem 5: Dynamic Logic II

Figure 5 shows a dynamic CMOS circuit in Domino logic. In determining source and drain areas and perimeters, you may use the following approximations: $AD = AS = W \times 0.625\mu m$ and $PD = PS = W + 1.25\mu m$. Assume 0.1 ns rise/fall times for all inputs, including the clock. Furthermore, you may assume that all the inputs and their complements are available, and that all inputs change during the precharge phase of the clock cycle.

a) What Boolean functions are implemented at outputs F and G? If A and B are interpreted as two-bit binary words, $A = A_1A_0$ and $B = B_1B_0$, then what interpretation can be applied to output G?

Solution

$F = A_0B_0 + \overline{A}_0\overline{B}_0$, $G = F(A_1B_1 + \overline{A}_1\overline{B}_1)$

If A and B are interpreted as two-bit binary words, output G is high if $A = B$: a comparator

b) Which gate (1 or 2) has the highest potential for harmful charge sharing and why? What sequence of inputs (spanning two clock cycles) results in the worst-case charge-sharing scenario? Using SPICE, determine the extent to which charge sharing affects the circuit for this worst case.

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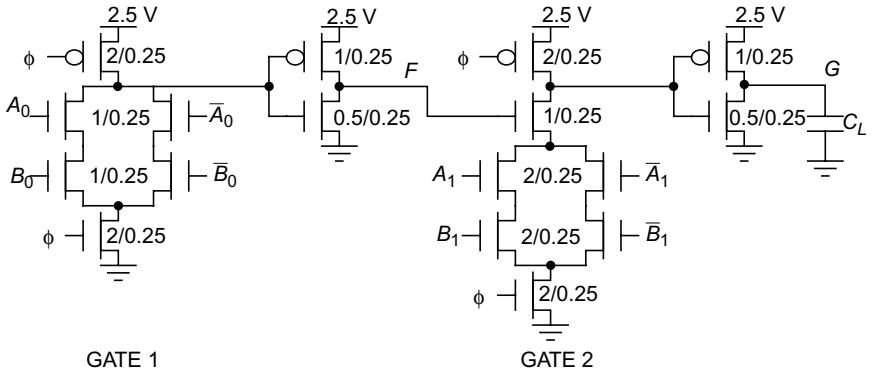
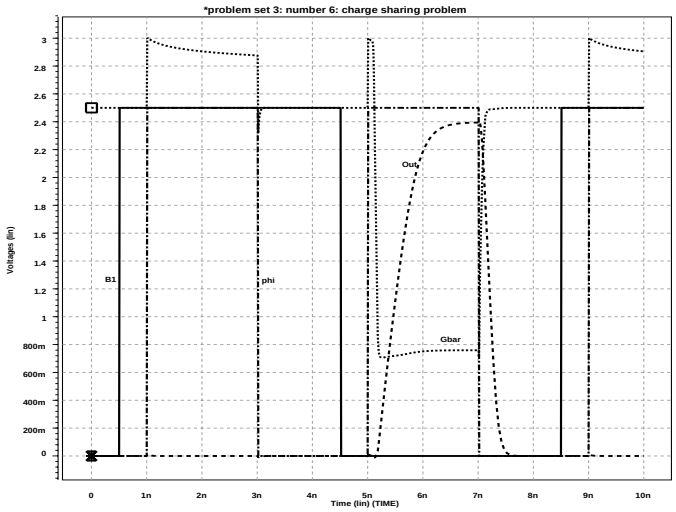


Solution

Gate 2 has the higher potential for harmful charge sharing because the capacitance that contributes to charge sharing is larger than in gate 1.

The sequence of inputs resulting in the worst-case charge sharing is $A_0 \neq B_0$ and $A_1 = B_1$ for the first cycle. Then $A_0 = B_0$ and $A_1 \neq B_1$ for the second cycle such that $A_1/\overline{A}_1$ transistor that is on during the second cycle is the same as in the first cycle. For example, $A_1 = B_1 = V_{DD}$ in cycle 1 and $A_1 = V_{DD}$, $B_1 = 0$ V in cycle 2. This will cause the charge at the output of gate 2 to be shared with the total parasitic capacitance at the drains of the A_1, $\overline{A}_1$, and B_1 transistors.

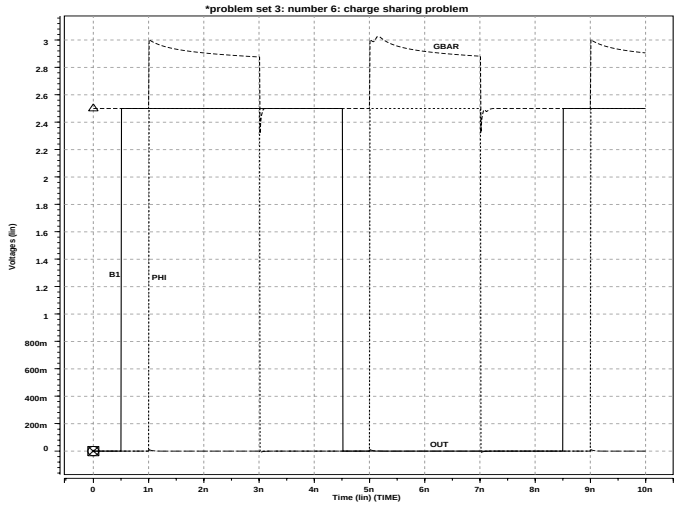


c) In part b you determined which gate (1 or 2) suffers the most from charge sharing. Add a single 2/0.25 PMOS precharge transistor (with its gate driven by the clock ϕ and its source connected to V_{DD}) to one of the nodes in that gate to maximally reduce the charge-sharing effect. What effect (if any) will this

addition have on the gate delay? Use SPICE to demonstrate that the additional transistor has eliminated charge sharing for the previously determined worst-case sequence of inputs.

Solution

The additional precharge transistor should charge the node that is shared by the A_1 and $\overline{A}_1$ transistor drains and the F transistor source. Assuming the gate delay is dominated by the precharge stage, this will reduce the gate delay by briefly aiding the precharging of gate 2. SPICE output with additional precharge transistor.



d) For the new circuit (including additional precharge transistor), find the sequence of inputs (spanning two clock cycles) that results in the worst-case delay through the circuit. Remember that precharging is another factor that limits the maximum clocking frequency of the circuit, so your input sequence should address the worst-case precharging delay.

Solution

The worst-case delay results from $A = B$ for two consecutive cycles. This results in the maximum charging and discharging of the internal nodes

e) Using SPICE on the new circuit and applying the sequence of inputs found in part (d), find the maximum clock frequency for correct operation of the circuit. Remember that the precharge cycle must be long enough to allow all precharged nodes to reach ~90% of their final values before evaluation begins. Also, recall that the inputs (A, B and their complements) should not begin changing until the clock signal has reached 0 V (precharge phase), and they should reach their final values before the circuit enters the evaluation phase.

Solution

The maximum clock frequency is ~4.4 GHz if you didn't include parasitic capacitance. If you did, it is around 2 GHz depending on the assumptions you made.

Problem 6: Dynamic Power

For parts a and b of this problem, assume independent, identically-distributed uniform white noise inputs.

a) What logical function is implemented by the Circuit A? Does this schematic contain reconvergent fan-out? Explain your answer. Find the exact signal (P_1) and transition ($P_{0\to 1}$) formulas for nodes *X*, *Y*, and *Z* for: (1) a static, fully complementary CMOS implementation, and (2) a dynamic CMOS implementation. Assume an np-CMOS implementation with an n-tree first stage.

Solution

This schematic has reconvergent fan-out because both inputs of the or gate depend on the value of S. However, due to the special nature of this particular case, conditional probablity is NOT required to complete the solution.

Assuming a fully complementary CMOS implementation:

X is the output of an AND gate with independent, identically-distributed uniform white noise inputs. As only when both inputs are equal to 1 the output is 1, $P_1 = 0.25$. On the other hand $P_{0\to 1} = P_0P_1 = 0.25(1-0.25) = 0.1875$.

Y is also the output of an AND gate with independent, identically distributed uniform white noise inputs. The analysis is the same as with X.

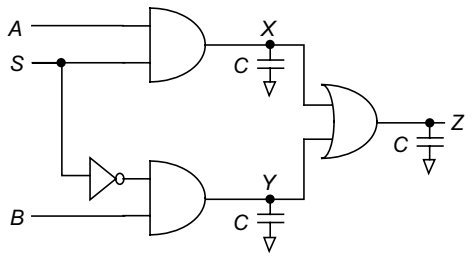
If we represent the truth table of the schematic we will see that $P_1 = 0.5$. Then $P_{0\to 1} = P_0P_1 = 0.5(1-0.5) = 0.25$.

Assuming a dynamic CMOS implementation:

In the same way as before, for X, $P_1 = 0.25$. In order to obtain the transition probability, an n-tree dynamic gate will be assumed. In this case: $P_{0\to 1} = P_0 = 0.75$.

The analysis for Y is equal to the analysis for X.

For Z, using the truth table of the schematic we obtain, again , $P_1 = 0.5$. For the transition probability, it will be assumed that a np-CMOS structure is used.. Then, Z is the output of a p-tree dynamic gate. Then: $P_{0\to 1} = P_1 = 0.5$.



b) Compute the switching power consumed by Circuit A, assuming that all significant capacitances have been lumped into the three capacitors shown in the figure, where C = 0.3 pF. Also, assume that VDD = 2.5 V and that input events occur at a frequency of 100 MHz. Perform this calculation for a static, fully-

complementary CMOS implementation and a dynamic CMOS implementation. Assume np-CMOS again for the dynamic implementation, but find the power for both orders of trees.

Solution

i)A static, fully-complementary CMOS implementation.

Switching power is:

$$P_{SW} = \alpha \cdot f \cdot C \cdot V_{DD}^2 = (\alpha_{X0\to1} + \alpha_{Y0\to1} + \alpha_{Z0\to1}) \cdot f \cdot C \cdot V_{DD}^2$$

We calculated previously the probabilities of a 0->1 transistion for each node: $P_{0\to1}$ for X and Y is 0.1875 and $P_{0\to1}$ for Z is 0.25.

Thus, P_{SW} = (2*0.1875+0.25)*100MHz*0.3pF*2.5^2 = 117.2uW.

ii)A dynamic CMOS implementation

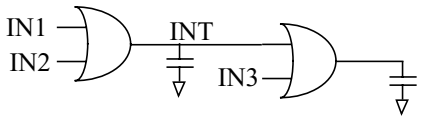
In part b) for a dynamic np-CMOS gate, we calculated the probabilities: $P_{0\to1}$ for X and Y is 0.75 and $P_{0\to1}$ for Z is 0.5. Thus, P_{SW} = (2*0.75+0.5)*100MHz*0.3pF*2.5^2 = 375uW.

When the first stage is implementated with a p-tree, $P_{0\to1}$ is equal to P_1 = 0.25. The output stage has $P_{0\to1}$ equal P_0=0.5. Thus,

P_{SW} = (2*0.25+0.5)*100MHz*0.3pF*2.5^2 = 187.5uW.

c) Now consider the implementation of a 3-input OR gate shown in Circuit B. Assume that you have 3 inputs A, B, and C and where P(A=1)=0.5, P(B=1)=0.2, P(C=1)=0.1. For a static CMOS implementation of this circuit and neglecting any glitches that may occur, what is the best order to place these inputs in order to minimize power consumption? What is the activity factor at the internal node (INT) in this case? What is the worst order and the activity factor of the internal node in this case?

Circuit B



Solution

	P(0) for INT	P(1) for INT	Alpha(0->1)
AB	0.4	0.6	0.24
AC	0.45	0.55	0.248
BC	0.72	0.28	0.201

So, to minimize power comsuption we should place B and C at the first stage. The worst case occurs when A and C placed at the input stage. The activity factors for each case are shown in the table above.

Problem 7: Dynamic Logic III

Consider the circuit shown below:

a) Give the logic function of *x* and *y* in terms of *A*, *B*, and *C*. Sketch the waveforms at *x* and *y* for the given inputs. Do *x* and *y* evaluate to the values you expected from their logic functions? Explain.

Solution

x = $\overline{AB}$ and y = AB$\overline{C}$

The circuit does not correctly implement the desired logic function. This stems from the fact that x is pre-charged high, and thus node y is discharged as soon as the evaluation phase starts. Although x is eventually discharged by the first stage, y cannot be charged high again since it is a dynamic node with no low-impedance path to Vdd (during evaluate). Common solutions to this problem are to place an inverter between the two stages (thus allowing only 0-to-1 transitions on the inputs to each stage during evaluate) as in Domino logic or employ np-CMOS. The latter is presented in (b).

b) Redesign the gates using *np*-CMOS to eliminate any race conditions. Sketch the waveforms at *x* and *y* for your new circuit

Solution.