Code No: 125EB

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD B. Tech III Year I Semester Examinations, November/December - 2017

LINEAR AND DIGITAL IC APPLICATIONS

| Time: 3 hours Note: This question paper contains two parts A and B. Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units: Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions. PART - A (25 Marks) 1.a) Define input offset voltage. List features of 741 op-amp. Discuss about all pass filters. List different ADC and DACs. List specifications of DAC. Which of the parameters decide the fan out and how? Explain noise margin and propagation delay with respect to CMOS logic. What is race around condition? How is it avoided? Explain one application of SR latch. PART - B (50 Marks) 2. Draw the circuit diagram of a two input non-inverting type summing amplifier and derive the expression for the output voltage. OR 2. Draw the block diagram of 565 PLL and explain about each block. Make circuit connections to track the input signal and explain its operation. Draw the block diagram of 565 PLL and explain about each block. Make circuit connections to track the input signal and explain its operation. OR Design a wide band pass filter with f _L =500 Hz and f _H = 2KHz, and a pass band again = 5 for both sections of filter. Also determine the value of Q for the filter. OR Which is the fastest ADC? Explain the operation and discuss its merits and de-merits. OR | | (Common to ECE, ETM) | *** |
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| b) List features of 741 op-amp. [3] c) Discuss about all pass filters. [2] d) List the application of 565 PLL. [3] e) List different ADC and DACs. [2] f) List specifications of DAC. [3] g) Which of the parameters decide the fan out and how? [2] h) Explain noise margin and propagation delay with respect to CMOS logic. [3] i) What is race around condition? How is it avoided? [2] j) Explain one application of SR latch. [3] PART - B (50 Marks) 2. Draw the circuit diagram of a two input non-inverting type summing amplifier and derive the expression for the output voltage. [10] OR 3. Explain the working of instrumentation amplifier with suitable diagram. [10] 4. Draw the block diagram of 565 PLL and explain about each block. Make circuit connections to track the input signal and explain its operation. [10] OR 5. Design a wide band pass filter with f _L =500 Hz and f _H = 2KHz, and a pass band again = .5 for both sections of filter. Also determine the value of Q for the filter. [10] 6. Which is the fastest ADC? Explain the operation and discuss its merits and de-merits. [10] | | | Marks) |
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| OR [10] | 5. | | |
| | .6. | | |
| | 7. | OR With a neat diagram explain the working principle of R-2R ladder type DAC. | [10] |

| | 8. | With neat circuit diagram explain the working of a 4-bit odd parity generator. OR Design 16×1 multiplexer using 4×1 multiplexer. | | | | | [10] |
|--|-----|--|-----------|--|-----------|-------------|---------|
| | 9. | | | | | | [10] |
| | 10. | Design a modulo 12 ripple counter using 74×74. | | | | | [10] |
| | 11. | How many address and data lines are required to access all the locations of dy RAM cell arrays specified below? | | | | | |
| | | a) 4M × 4 | b) 1M × 1 | c) 1M × 4 | d) 4M × 1 | | |
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