Code No: 114AF

R13

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year II Semester Examinations, November/December - 2015

DIGITAL DESIGN USING VERILOG HDL

(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a) What is System Tasks. [2M]
b) Explain the Levels of Design Description. [3M]
c) What is Tristate Gates? [2M]
d) Write about Assignment to Vectors. [3M]
e) Define Parallel Blocks. [2M]
f) Write the syntax for While Loop. [3M]
g) Define Bi Directional Gates. [2M]
h) Write about User Defined Primitives. [3M]
i) What is a Design Verification? [2M]
j) Write short note on Feedback Model. [3M]

PART-B

(50 Marks)

2.a) List and explain different keywords of verilog HDL.
b) Design module to illustrate use of the wand-type net and test bench with stimulation results. [5+5]

OR

3.a) Explain about Programming Language Interface with example.
b) Write short notes on concurrency and functional verification. [5+5]

4.a) Design a JK-Flip-Flip with gate primitives, and write verilog code for that.
b) Explain RS Flip-Flop with Verilog module and Test Bench. [5+5]

OR

5.a) Explain simple latch with Verilog module.
b) Write about Assignment to Vectors. [5+5]

6.a) Define While loop, write syntax with flow chart.
b) Explain FOR loop example with Verilog code. [5+5]

OR

7.a) Design Verilog module Event construct for a serial data receive and test bench for the same.
b) Explain about Blocking and Non- Blocking Assignments. [5+5]

8.a) Design CMOS switch of parallel combination.
b) Briefly explain combinational and sequential UDPs in Verilog. [5+5]

OR

9.a) Classify delays and explain.
b) Explain delays with Tristate Gates. [5+5]

10.a) Write the Verilog code for basic functional unit of a dynamic shift register.
b) Briefly explain any one method used for sequential circuit testing. [5+5]

OR

11.a) Write a short note on Test Bench Techniques.
b) Discuss in detail about Static Machine Coding. [5+5]

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