Code No: 5157S

R13

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech II Semester Examinations, October - 2015
SYSTEM ON CHIP ARCHITECTURE
(VLSI System Design/VLSI Design)

Time: 3 Hours **Max. Marks: 60**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 8 marks and may have a, b, c as sub questions.

PART - A

5 × 4 marks = 20

1.a) Draw the diagram of pipelined processor model and explain. [4]
b) What are the causes for pipeline delays or breaks? [4]
c) Give a comparison of various flash memories. [4]
d) What is SOC customization? What are the two main approaches for providing customized processors? [4]
e) Write short notes on JPEG compression. [4]

PART - B

5 × 8 marks = 40

2. Compare the salient features of Array and Vector Processors. [8]

OR

3.a) Give the classification of processors by their application and their architecture.
b) Explain about various SOC system level interconnection methods. [4+4]

4. Explain about various dynamic branch prediction methods. [8]

OR

5. Explain the various blocks in an instruction unit with the help of a diagram. [8]

6. Draw the diagram of a two-way set associative TLB and explain the virtual to real address translation. [8]

OR

7. Explain the internal configuration of DDR SDRAM with the help of a diagram. [8]

8. Explain the architecture of IBM's Core Connect bus in a SOC system with the help of a diagram. [8]

OR

9. Explain about the different reconfigurable interconnect architectures. [8]

10. Explain the following Case study giving the algorithm, requirements, design and evaluation : Advanced Encryption Standard (AES). [8]

OR

11. Draw the block diagram of a simplified approach for designing SOC devices and explain. [8]

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