Code No: 5157K

R13

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech II Semester Examinations, October - 2015

LOW POWER VLSI DESIGN

(VLSI System Design /VLSI Design)

Time: 3 Hours **Max. Marks: 60**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 8 marks and may have a, b, c as sub questions.

PART-A

5 × 4 Marks = 20

1.a) Minimal transistor sizing for reducing dynamic power could increase short circuit power. Why? How do you solve this problem? [4]

b) Compare VTCMOS circuit with MTCMOS circuit. [4]

c) Explain the principle of carry save adder. [4]

d) Describe the operation of Baugh-Wooley Multiplier. [4]

e) Give self-refresh circuit in DRAM. [4]

PART B

5 × 8 Marks = 40

2.a) Why does leakage current increase drastically as the device size shrinks below 250 nm in deep submicron (DSM) regime? Give the relation between I_L and V_{TH}.

b) Outline four different circuit techniques for leakage power reduction in DSM era with suitable examples. [4+4]

OR

3.a) Describe the principle of short circuit power dissipation.

b) Explain the principle of drain induced barrier lowering and punch through. [4+4]

4. It is required to reduce the power consumption of a CMOS circuit by a) self reverse bias and b) Dynamic voltage scaling (DVS) techniques. Give suitable schemes and briefly explain how they satisfy this requirement. [8]

OR

5. Describe one switched capacitance minimization approach. [8]

6. Consider a simple data path with (32 bit adder + comparator). The data path works at half the speed due to voltage scaling by a factor of 40 %. To maintain the throughput, a student proposes to use parallel architecture while his friend proposes pipeling. Estimate the power reduction in both cases. Compare both architectures with respect to dynamic power reduction and area. [8]

OR

7.a) Describe the principle of carry select adders.

b) What are low-voltage low-power styles? [4+4]

8. Offer a hybrid modified Booth and Wallace Tree multiplier cell structure for low power and high speed requirement. List out the features of such a structure. [8]

OR

9. Write any two types of multiplier architectures. [8]

10. Give the architecture of a shared bit line (BL) SRAM system and explain how it reduces power consumption significantly when compared to a traditional SRAM system? [8]

OR

11. Explain the operation of two different low power SRAM architectures. [8]

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