

Code No: 5157P

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech II Semester Examinations, October - 2015

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

(VLSI System Design/VLSI Design)

Time: 3 Hours

Max. Marks: 60

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 20 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 8 marks and may have a, b, c as sub questions.

## PART - A

5 × 4 marks = 20

- 1.a) Classify discrete-time signals. [4]
- b) Compare DFT and FFT. [4]
- c) What is the advantage of using block floating point format to represent signals in DSP systems? Explain with a numerical example. [4]
- d) Summarize various data addressing modes in a DSP processor with examples. [4]
- e) Explain fixed-point format and Floating-point format for signals and coefficients in detail. [4]

## PART - B

5 × 8 marks = 40

- 2.a) Find the linear convolution of the sequences  $x(n) = \delta(n) + 0.6\delta(n-1)$ ;  $h(n) = 0.2\delta(n) + 3\delta(n-1)$  using DFT. [4+4]
  - b) Tabulate various window functions used for FIR filter design. [4+4]
- OR
- 3.a) Draw and implement DIT FFT algorithm in detail.
  - b) Explain about the number of real computations required for the direct computation of N Point DFT of a sequence  $x(n)$ . [4+4]
4. Design a digital filter equivalent of a 2nd order Butterworth low-pass filter with a cut-off frequency  $f_c = 100$  Hz and a sampling frequency  $f_s = 1000$  samples/sec. Derive the finite difference equation and draw the realization structure of the filter. Given that the analogue prototype of the frequency-domain transfer function  $H(s)$  for a Butterworth filter is:  $H(s) = 1/(s^2 + s + 2)$  [8]
- OR
- 5.a) What is zero overhead looping? How this feature is advantageous in DSP processor? Explain with an example.
  - b) Explain the following concepts of DSP processor i) Interlocking ii) Branching effects and iii) Interrupt effects. [4+4]

- 6.a) Explain the interfacing of PCM3002 codec with TMS320VC5416 DSK using block diagram and transmission formats.  
b) Explain the implementation of 8-point FFT on the TMS320C54XX with an assembly code. [4+4]

OR

7. Write the algorithm and program using TMS320C54XX for the following:  
a) Butterfly in Radix 2 DIT FFT  
b) Interpolation or decimation. [4+4]

- 8.a) Explain about the following DSP computational building blocks with neat Diagrams.  
i) Barrel shifter  
ii) MAC unit  
iii) ALU unit.

- b) Explain the bit reversed and circular addressing modes with suitable examples. [4+4]

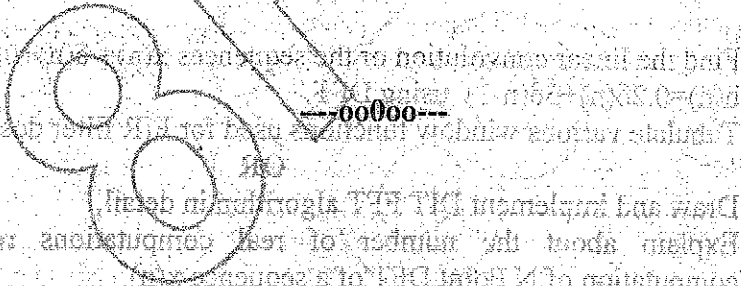
OR

- 9.a) What are the basic architectures for programmable DSP devices? Explain.  
b) Investigate the basic features that should be provided in the DSP architecture to be used to implement any  $N^{\text{th}}$  order FIR filter. [4+4]

10. Explain Memory interface, Parallel I/O interface, Programmed I/O. [8]

OR

11. Compare the following I/O interfacing methods:  
a) Programmed I/O with respect to DSP processor  
b) Interrupt I/O. [4+4]



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