Code No: 5157L

R13

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech II Semester Examinations, October - 2015
CAD FOR VLSI CIRCUITS
(VLSI System Design/VLSI Design)

Time: 3 Hours **Max. Marks: 60**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 8 marks and may have a, b, c as sub questions.

PART - A

5 × 4 marks = 20

1.a) Compare various design styles for Area, Performance and Fabrication layers. [4]
b) List the important procedures of K-L Algorithm. [4]
c) List the approaches that an extension to global routing algorithms for multi-terminal nets. [4]
d) Write the important steps involved in physical design cycle for FPGA. [4]
e) Mention the different models available for ESD testing. [4]

PART - B

5 × 8 marks = 40

2. Compare and differentiate the design cycle for Full Custom, Semi Custom and Gate Arrays based design styles. [8]

OR

3. Explain the major stages in physical design flow used in modern VLSI chip design. [8]

4. Briefly discuss the classification of Floorplanning algorithms and discuss the Rectangular Dualization technique. [8]

OR

5. Briefly discuss the classification of partitioning algorithms. [8]

6. Discuss:
a) Channel Routing Problem and
b) Single Layer Routing Algorithm. [4+4]

OR

7. Briefly classify global routing algorithms and discuss Maze Routing Algorithm. [8]

8. Explain the difference between segmented and Non-segmented routing n/w. Discuss the routing Algorithm for Segmented Model. [8]

OR

9. Explain the technique for performance driven placement and partitioning of MCMs. [8]

10.a) What are the causes of Latchup in CMOS fabrication?
b) Mention the guidelines to avoid latchup. [4+4]

OR

11. Discuss the considerations for clock generation and distribution for the high speed Digital System Design. [8]

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