Code No: 09A70412 R09

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech IV Year I Semester Examinations, November - 2013
VLSI Design
(Common to ECE, EIE, BME, IT, ETM, ECM, ICE)

Time: 3 Hours **Max. Marks: 75**

Answer any Five Questions
All Questions Carry Equal Marks

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1. Explain the fabrication of a CMOS transistor. [15]

2.a) Explain the working of a BiCMOS inverter.
b) Derive the equation for the drain current of a NMOS transistor. [7+8]

3.a) Explain the VLSI Design flow.
b) What is a stick diagram? Draw the stick diagram of a three input CMOS NAND gate. [7+8]

4. What is the problem encountered by VLSI circuits in driving large capacitive loads? Suggest and explain two solutions to overcome the problem. [15]

5. Design and explain the working of the following circuits using CMOS transistors
a) 2 bit counter b) zero cross detector [15]

6.a) Explain the working of a SRAM cell.
b) Explain the working principle of content addressable memory. [7+8]

7.a) Explain the parameters affecting the power dissipation of a circuit
b) Write short notes on CPLDs. [7+8]

8. Discuss a technique of testing a VLSI circuit under these levels
a) system level b) chip level. [15]

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