

Code No: 123CT

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations, March - 2017

DIGITAL LOGIC DESIGN

(Computer Science and Engineering)

Time: 3 Hours

Max. Marks: 75

**Note:** This question paper contains two parts A and B.

Part A is compulsory which carries 25 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit.

Each question carries 10 marks and may have a, b, c as sub questions.

**PART - A****(25 Marks)**

1. a) Using 10's complement subtract  $72532 - 3250$ . [2]
- b) State and prove the distributive property of Boolean algebra. [3]
- c) Define sum of products and product of sum. [2]
- d) Give the boolean expression for the following statement.  
Y is a 1 only if A is 1 and B is 1 or if a is 0 or B is 0. [3]
- e) What is a multiplexer? What is the function of multiplexer select inputs? [2]
- f) What is a combinational logic circuit? Explain the design procedure for combinational circuits. [3]
- g) What is a counter and what are the types of counters? [2]
- h) Draw the logic diagram for SR latch using two NOR gates. [3]
- i) How does static RAM cell differ from dynamic RAM cell? [2]
- j) Give the difference between RAM and ROM. [3]

**PART - B****(50 Marks)**

- 2.a) Prove that  $AB + (AC)' + AB'C(AB + C) = 1$ .
- b) What is a Hamming code and encode data bits 0101 into a 7-bit even parity Hamming code. [5+5]

**OR**

- 3.a) Describe the floating point representation of numbers and determine the number of bits required to represent in floating point notation the exponent for decimal numbers in the range of  $10^{\pm 86}$ .
- b) Give the comparison between 9's complement and 10's complement and perform the following subtraction by using 9's complement method.  
i)  $18 - 06$       ii)  $39 - 23$  [5+5]

- 4.a) Reduce the following function using K-Map Technique and implement using universal gate.  $f(P, Q, R, S) = \sum m(0, 1, 4, 8, 9, 10) + d(2, 11)$ .

- b) Design a logic circuits with inputs A, B, C so that output Y is high whenever A is zero or whenever  $B=C=1$  [5+5]

**OR**

- 5.a) Realize the following function  $Y = A + B\bar{C}\bar{D}$  using NAND gates only.

- b) Minimize the following multiple output function using K-map

$$f_1 = \sum m(0, 2, 6, 10, 11, 12, 13) + d(3, 4, 5, 14, 15)$$

$$f_2 = \sum m(1, 2, 6, 7, 8, 13, 14, 15) + d(3, 5, 12)$$

[4+6]

6.a) What is a decoder? Construct a 4x16 decoder with two 3x8 decoders.

b) Implement the following boolean function using 8:1 multiplexer.

$$f(A, B, C, D) = \bar{A}B\bar{D} + A\bar{C}D + \bar{B}CD + A\bar{C}D$$

[5+5]

OR

7.a) Explain a binary parallel adder with look a head carry scheme.

b) Design a combinational logic circuit with 3-input variables that will produce a logic 1 output when more than one input variables are logic 1. [5+5]

8.a) Design a 4-bit universal shift register and explain its operation?

b) Design a mealy type sequence detector to detect a serial input sequence of 101. [5+5]

OR

9.a) With the help of a neat block diagram explain the working of a JK Master-Slave flip-flop.

b) What are presettable counters? What is lockout of a counter? Show how to construct a MOD-13 counter using 74163 synchronous binary counter IC. [5+5]

10.a) Explain how a PLA is used for the realization of combinational function.

b) Describe the function of row-select decoder column-select decoder and output buffers in the ROM architecture. [5+5]

OR

11.a) Design binary to Gray and Gray to Binary converters in a single PLA

b) Design a memory decoder to select 1 number of 16KB EPROM IC and 1 number of 32KB RAM IC. [5+5]

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