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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD B.Tech III Year I Semester Examinations, February/March - 2016 LINEAR AND DIGITAL IC APPLICATIONS (Common to ECE, BME)

Time: 3 hours Max. Marks: 75

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, cas sub questions.

Part- A

202	1.a)	Give t	he idea	ıl values an	d practica	l values of	various o	p-amp	oaramet	ers.	(25	Marks)
	b)	Define	e therm	al drift and	slew rate		•				-	[3]
	c)	Write	the app	olications of	f 555 time	r in astabl	e mode.					[2]
Section 1	d)	What	are the	modes of o	peration of	of a timer?	au	55		64		[3]
	e)	Explai	n the p	rincipal of	weighted	resistor ty	pe DAC.	44	19 °C	6277°5.		[2]
	f)			fications of								[3]
	g)			ty Encoder.								[2]
24.24	h) '			ssification		ted Circuit	s. bre	4M	rne Eggi S Si	48. 38. 23. 38. 31 23. 38. 31		13 1
	i)	Name	differe	nt Types of	ROMS.							[2]
	j)	List th	e applic	cations of R	lOMs. 🏻 🗎							[3]
SOLTENA LESSON CO LESSON CO	٠.			1		Part-B		Ē.				
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What are the three differential amplifier configurations? Compare and contrast these 2.a) configurations.

Explain frequency compensator techniques used in op-amp. b)

[6+4]

Calculate the effect of variation in power supply voltages on the output offset voltage 3.a) for an op - amp circuit. au

OR

Explain the advantages and disadvantages of ICs. b)

[6+4]

Give the functional block diagram of VCO NE566 and explain its working and 4. necessary expression for free running or center frequency. T101

Explain the monostable operation of the 555 timer and derive the expression for the 5.a) period of a pulse generated by the Timera ide.

Design a circuit to generate square waveform using op-amp. b)

26, 246,

[5+5]

Draw the block diagram and explain the operation of dual slope A/D converter. What 6. are its advantages and disadvantages?

Explain the operation of the fastest analog to digital converter. What is the main 7.a) drawback of this converter? Compare this converter with other types.

Draw the circuit of a Ladder type DAC for 4 bits and derive expression for output **b**) voltage. [5+5]

SH.

31 M. P 40 S 1	8	a) Basic	comparate	n the follow or operatio	n.		望街		8	70.00 6 4 7	er Ere	äÄ
		b) Logic	c diagram	for compar	ison of 2	- bit bin OR	ary numbers	S.			[5+5]	
CARA CARA	9.a)	Design	a 2-input	NOR gat	eusing	CMOS	transistors.	Explain	the o	peration	of the	ARES AN ARESSE:
		circuit v	with the he	lp of funct O and LCD	ion table.		:				[7+3]	
2.25 1.77 -	b)					OWI MAN.	KM2 KREK		601	A ACTUAL Constitution	131 C	e e
	10.a)	Draw th	e internal	structure on 1T DRA	f synchro M Cell	onous SF	RAM and ex	plain the	opera	tion.	[5+5]	
	1.0					OR	5 110 OI	· · · · · · · · · · · · · · · · · · ·	12:-	معدده دستان	af-0\1	COLUMN .
		destin D	A TA II				M cell2 Sho					PATE TO
	b)	Design	an 8-bit r	arallel-in	and seria	al-out sh	ift register.	Explain	the o	peration	of the [5+5]	
		above s	hift registe	r with the	help of ti	ming Wa	aveiorms.	AN MAZ	#25 823			ene.
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