Code No: 114CN

× · · · ·

× * * × * × × * * × * × * ×

× • • × × • • ×

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD B.Tech II Year II Semester Examinations, May - 2016 **COMPUTER ORGANIZATION**

* . * * . .

(Computer Science and Engineering)

Time: 3 Hours

Max. Marks: 75

R13

**** **** ****

1. CSC -65

Note: This question paper contains two parts A and B. Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

····· PAPT _ A.····

x x x x x x x x x x x x x x x x x x x	PART - A	(25 Marks)
1.a)	What is the role of PC, IR registers?	[2]
b)	How many references to memory are needed for direct address	instruction to
	bring an open and into a processor register?	[3]
c)	What are the advantages of DMA?	[2]
d)	Explain dairy-chain priority interrupt.	
e)	What is hit ratio?	[2]
f)	What is the transfer rate of an eight-track magnetic tape w	hose speed is
	120 inches per second and whose density is 1600 bits per inch?	[3]
g)	What is the function of 8086 index registers?	[2]
h)	What is non-maskable interrupt?	[3]
i)	What is the use of 'CMPS' 8086 instruction?	[2]
j)	Explain 'ROR' and 'ROL' 8086 instructions.	[3]
	PART - B	(50 Marks)
.2	Explain various instruction formats.	
**************************************	$\mathbf{OR} = \mathbf{OR} + OR$	0 X 0 W 0 A X X 0 4 X 2 A X 6 0 X 4 0 X 0 V 0 X 0 V 0 V 0 V 0 V 0 V 0 X 0 V 0 V 0 V 0 V 0 V 0 V 0 V 0 V 0 V
3.	Explain various addressing modes with examples.	[10]
4.	Draw and explain the block diagram of DMA controller.	[10]
~	OR	
2	Explain source-initiated and destination initiated data transfer using	, handshaking.
·×****	ີແມລີຂີ້ເ ີດແນ້ ນີ້ນີ້ ໃຫຍ່ ໃຫຍ່ ໃຫຍ່ ໃຫຍ່ ໃຫຍ່ ເ	**** * [*10]
6	The access time of a cache memory is 100 ns and that of main mem	1000 T
0.	is estimated that 80% of the memory requests for 'read' and remain	$\frac{1000 \text{ ns. ft}}{1000 \text{ ns. ft}}$
	'write' The hit ratio for read accesses only is 0.0. A write through	hing 20% for
* ****	used when a strain accesses only is 0.9. A white-thiough	i procedure is
× * × × * × * × * * *	a) What is the average access time of the system considering only	momorrand
	a) what is the average access time of the system considering only	memory read
	b) What is average access time of the system considering only	memory read
	evcles?	memory reau
	c) What is the hit ratio taking into consideration the write cycles?	[4+3+3]
· · · · · · · · · · · · · · · · · · ·	OR OR OR OR	
× * * *		* * * *

		Explain the set-a Write short notes	ssociative mapp s on virtual mem	ing of cache men ory.	nory.	[5+5]	
	8.	Explain the field	s in 8086 flag re	gister.		[10]	
4 2 2 4 4 4 5 4 4 5 4 4 6 4 7		Explain the pin d	iagram of 8086	OR with figure		····; [[10]	××* ×** × × * * * *
	10.	Write 8086 asser Equivalent BCD	mbly language p number.	orogram to conve	ert a 16-bit binar	y number into [10]	**** *
x 2 + + + + + + + + + + + + + + + + + + +	11 ***********************************	Write a 8086 asse	embly language i	orogram to find ty	wo 16-bit operand	ls. [10]	*** * * * * * * * * * * * * * * * * * *
			· · · · · · · · · · · · · · · · · · ·	00 0 00			
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0				стр. стр.	1004 34095 4 4 5 4 7 5 4 5 4 7 5 4 5 4 7 7 5 5 4 5		
		9000 - 2000 9000 - 2000 - 200	775 0484 275 0484 275 0484 275 048 275	**** **** **** ****			
	CE					974 K. NYKA 974 K. NYKA 974 K. SY 974 K. SY 97	
	C.R.		T.P.				4447 - 4344 244 - 444 244 - 444
	CR						