UNIT III - VLSI CIRCUIT DESIGN PROCESSES

VLSI Design Flow

- Typical VLSI design flow is shown in Fig. 3.1.

Fig. 3.1 VLSI design flow

i) Design Specifications

- Specification of a design is as a guide to choose the right technology and for knowing the needs of the vendor. Specifications allows each engineer to understand the entire design. It helps the engineer for designing correct interface with rest of the circuit or system. It reduces time required for design and also misassumptions if any.

Any specification includes following information :

1. A block diagram providing details how designed chip fit into the entire system.
2. Internal block diagram for every subsection and its function.
3. Input threshold levels of all input pins and driving capability of output pins.
4. Timing specifications like setup and hold times, propagation delays and clock-cycle time.
5. Package type required.
6. Total gate count of the system under design.
7. Total power consumption of the circuit.
8. Test procedures for different tests.
9. Total cost of the target design chip.

ii) Design Entry

- User can enter a design with a schematic editor or any other text-based software tool, either a hardware description language (VHDL or VERILOG).

Schematic Entry

- It provides a graphical interface for design entry. A design can be build by a user with individual gates or he can combine gates to create functional blocks.

HDL Entry

- This entry supports mixed level description where gate and netlist constructs both are used along with functional descriptions.

iii) Functional Simulation

- It is the process where logic in the design is checked before user implements it in a device. As the timing information is not available at this early stage of design flow, functional simulator tests the logic of design using unit delays.

iv) Logic Synthesis

- Here logic synthesis tool is used which produces Netlist (textual information) from synthesis process. Logic cells and their interconnections are described in detail in the Netlist. Netlist is an EDIF (Electronic Data Interchange Format) file. Thus during synthesis behavioural information in the HDL file is translated into a structural netlist.

v) System Partitioning

- System partitioning is the process of dividing a large and complex system into smaller modules.

vi) Prelayout Simulation

- This is required for verification of a circuit design through software programs. Here stimuli is applied to design over a specific time period and recording, analyzing the respective response from the model.

vii) Floorplanner

- The main function of floorplanner is to estimate the required chip area that will be used for each standard cell or module of the design. It is responsible for performance improvement of the design. Floorplanner is a tool that lets user generate and edit hierarchical floorplans.

viii) Place and Route

- After design mapping, flow engine places and routes the design. All logic blocks, including the Configurable Logic Blocks (CLB) and Input-Output Blocks (IOB) are assigned specific locations on the die at place stage.

- In the route stage, the logic blocks are assigned, particular interconnect elements on die.

ix) Circuit Extraction

- This process determines the resistances and capacitances of all the interconnections.

x) Post layout simulation

- After physical place and route, this simulation is carried out. While carrying out this simulation propagation delays of logic cells and interconnection delays of interconnect are taken into account. If post layout simulation results ful-fill the design specifications, designer can proceed for chip finishing part.

xi) Physical Verification

- After placement and routing and full custom editing physical verification is carried out. It is the process of interpreting the physical layout data to determine whether it conforms to the electrical design rules, physical design rules and source schematic. Design Rule Check (DRC), Electrical Rule Check (ERC), Antenna check and short circuit check are the processes which comes under physical verification.

xii) Testing

- During production of chips, it is necessary to have some sort of built-in tests for designed system which continuously tests the system over long period of time. Chip will fail because of some electrical or mechanical problems that will usually show up with such testing procedure.

xiii) Chip Fabrication

- Before submitting design for fabrication, input-output pads should be included in the design and it's connectivity should be verified.
- Then appropriate package selection for the design and selecting bonding plan for the package is required. Details of how each pad of design is connected to each pin of package is required.

MOS LAYERS

MOS design is aimed at turning a specification into masks for processing silicon to meet the specification. We have seen that MOS circuits are formed on four basic layers—*n-diffusion, p-diffusiqn, polysilicon*, and *metal*, which are isolated from one another by thick or thin (thinox) silicon dioxide insulating layers. The thin oxide (thinox) mask region includes

n-diffusion, p-diffusion, and transistor channels. Polysilicon and thinox regions interact so that a transistor is formed where they cross one another. In some processes, there may be a second metal layer and also, in some processes, a second polysilicon layer. Layers may deliberately joined together where contacts are formed. We have also seen that the basic MOS transistor properties can be modified by the use of an implant within the thinox region and this is used in nMOS circuits to produce depletion mode transistors.

We have also seen that bipolar transistors can be included in this design process by the addition of extra layers to a CMOS process. This is referred to as BiCMOS technology, and in this text it is dealt with in an n-well CMOS environment.

We must find a way of capturing the topology and layer information of the actual circuit in silicon so that we can set out simple diagrams which convey both *layer* information and *topology*.

STICK DIAGRAMS

Stick diagrams may be used to convey layer information through the use of a color code—for example, in the case of nMOS design, green for n-diffusion, red for polysilicon, blue for metal, yellow for implant, and black for contact areas. In this text the color coding has been complemented by monochrome encoding of the lines so that black and white copies of stick diagrams do not lose the layer information. The encodings chosen are shown and illustrated in color as Color plates l(a)–(d) and in monochrome form as Figures 3.1(a)–(d). When you are drawing your own stick diagrams you should use single lines in the appropriate colors, as in Color plate 1(d) noting that yellow lines are outlined in green for clarity only.

Note that mask layout information, which is also color coded, may also be hatched for monochrome encoding, also shown in Figures 3.1(a)–(c). Monochrome encoding schemes are widely illustrated throughout the text, and it will be noted that diagrams and mask layouts in this form are readily reproduced by copying machines.

The color and monochrome encoding scheme used has been evolved to cover nMOS, CMOS, and BiCMOS processes and to be compatible with the design processes of gallium arsenide. The color encoding is compatible with color terminals, printers, and plotters having quite simple color palettes. Using color workstations, the mask areas are usually color filled while pen plotters produce color outlines only. In this text, most color diagrams incorporate color outlines and color hatching (hatching as for the monochrome encoding) so that the detail of underlying areas may be easily discerned where layers intersect or are superimposed. This form of color representation is acceptable for those with color vision difficulties and may also be copied by a monochrome copier without losing the encoding. The various representations are indicated in Color plate 2.

In order to facilitate the learning and use of the encoding schemes, the simple set required for a single metal nMOS design is set out first as Figure 3.1(a) and Color plate l(a); for a double metal CMOS p-well process the required encodings are extended by those given as Figure 3.1(b) and Color plate l(b). Figure 3.1(c) and Color plate l(c) further extend the representations to cover a second polysilicon layer and BiCMOS technology.

COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
	MONOCHROME		MONOCHROME	
GREEN		n-diffusion (n$^+$ active) Thinox *	* Thinox = n-diff. + transistor channels	ND
RED		Polysilicon		NP
BLUE		Metal 1		NM
BLACK		Contact cut		NC
GRAY	NOT APPLICABLE	Overglass		NG
nMOS ONLY *YELLOW*		Implant		NI
nMOS ONLY *BROWN*		Buried contact		NB

FEATURE	FEATURE (STICK) (MONOCHROME)	FEATURE (SYMBOL) (MONOCHROME)	FEATURE (MASK) (MONOCHROME)
n-type enhancement mode transistor	D L:W S G; L:W S D G	GREEN outline (COLOR); S D G; RED line (COLOR)	(L:W = 1:1); S D G
Transistor length to width ratio L:W should be shown but source, drain and gate labeling will not normally be shown.			
n-type depletion mode transistor **nMOS ONLY**	L:W; L:W	GREEN outline (COLOR); S D G; YELLOW (COLOR); RED line (COLOR)	(L:W = 1:1)

FIGURE 3.1(a) **Encodings for a simple metal nMOS process (see Color plate 1(a) for nMOS color encoding details).**

In this chapter we will see how basic circuits are represented in stick diagram and in symbolic form. We will be using stick representation quite widely throughout the text. The layout of stick diagrams faithfully reflects the topology of the actual layout in silicon. To illustrate stick diagrams, inverter circuits are presented in Figure 3.1(d) and in Color plate l(d)—in nMOS, in p-well CMOS, and in n-well BiCMOS technology. A symbolic form of diagram is often most convenient and such diagrams are based on the simple symbol set included in Figures 3.1(a)–(c) and Color plates 1(a)–(c). The simplicity of symbolic form is illustrated in Figure 3.1(d), in Color plate l(d), and in Color plate 7.

Having conveyed layer information and topology by using stick or symbolic diagrams, these diagrams are relatively easily turned into mask layouts as, for example, the transistor stick diagrams of Figure 3.2 stressing the ready translation into mask layout form.

In order that the mask layouts produced during design will be compatible with the fabrication processes, a set of design rules are set out for layouts so that, if obeyed, the rules will produce layouts which will work in practice.

COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
GREEN	MONOCHROME ENCODING AS IN FIGURE 3–1(a)	n-diffusion (n⁺ active) Thinox *	MONOCHROME * Thinox = n-diff. + p-diff.+ transistor channels ENCODING AS IN FIGURE 3–1(a)	CAA or CNA
RED		Polysilicon		CPF
BLUE		Metal 1		CMF
BLACK		Contact cut		CC
GRAY		Overglass		COG
GREEN IN P+ (MASK) YELLOW (STICK)		p-diffusion (p^+ active)	p^+ mask	CAA or CPA
YELLOW	NOT SHOWN IN STICK DIAGRAM	p^+ mask		CPP
DARK BLUE OR PURPLE		Metal 2		CMS
BLACK		VIA		CVA
BROWN	DEMARCATION LINE p-well edge is shown as a demarcation line in stick diagrams	p-well		CPW
BLACK		V_{DD} or V_{SS} CONTACT	V_{DD} V_{SS}	CC

FEATURE	FEATURE (STICK) (MONOCHROME)	FEATURE (SYMBOL) (MONOCHROME)	FEATURE (MASK) (MONOCHROME)
n-type enhancement mode transistor (as in Figure 3–1(a))	DEMARCATION LINE L:W	GREEN RED	S D G
Transistor length to width ratio L:W may be shown.			
p-type enhancement mode transistor	L:W S D G DEMARCATION LINE	YELLOW S D G RED	S D G p^+ mask
Note: p-type transistors are placed above and n-type transistors below the demarcation line			

The same well encoding and demarcation line are used for an n-well process.
For p-well process, the n features are in the well. For an n-well process, the p features are in the well.

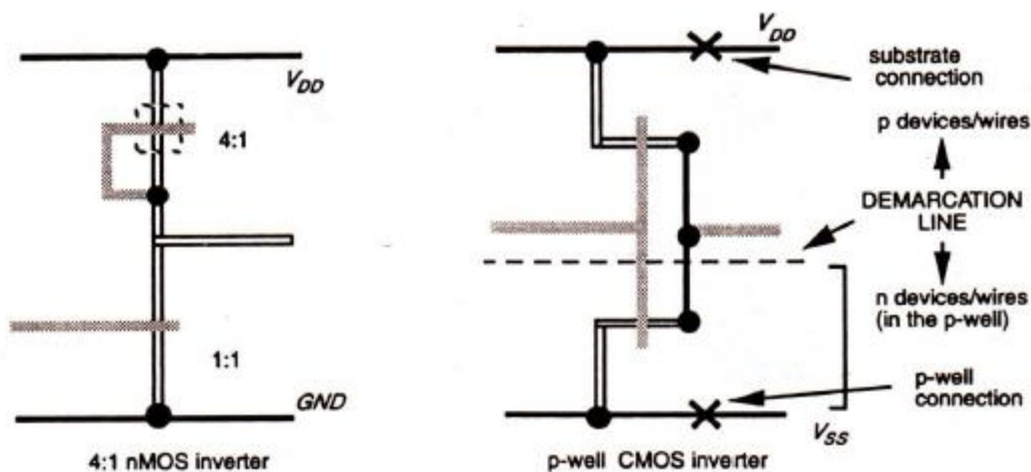
FIGURE 3.1(b) Encodings for a double metal CMOS p-well process (see Color plate 1(b) for CMOS color encoding details).

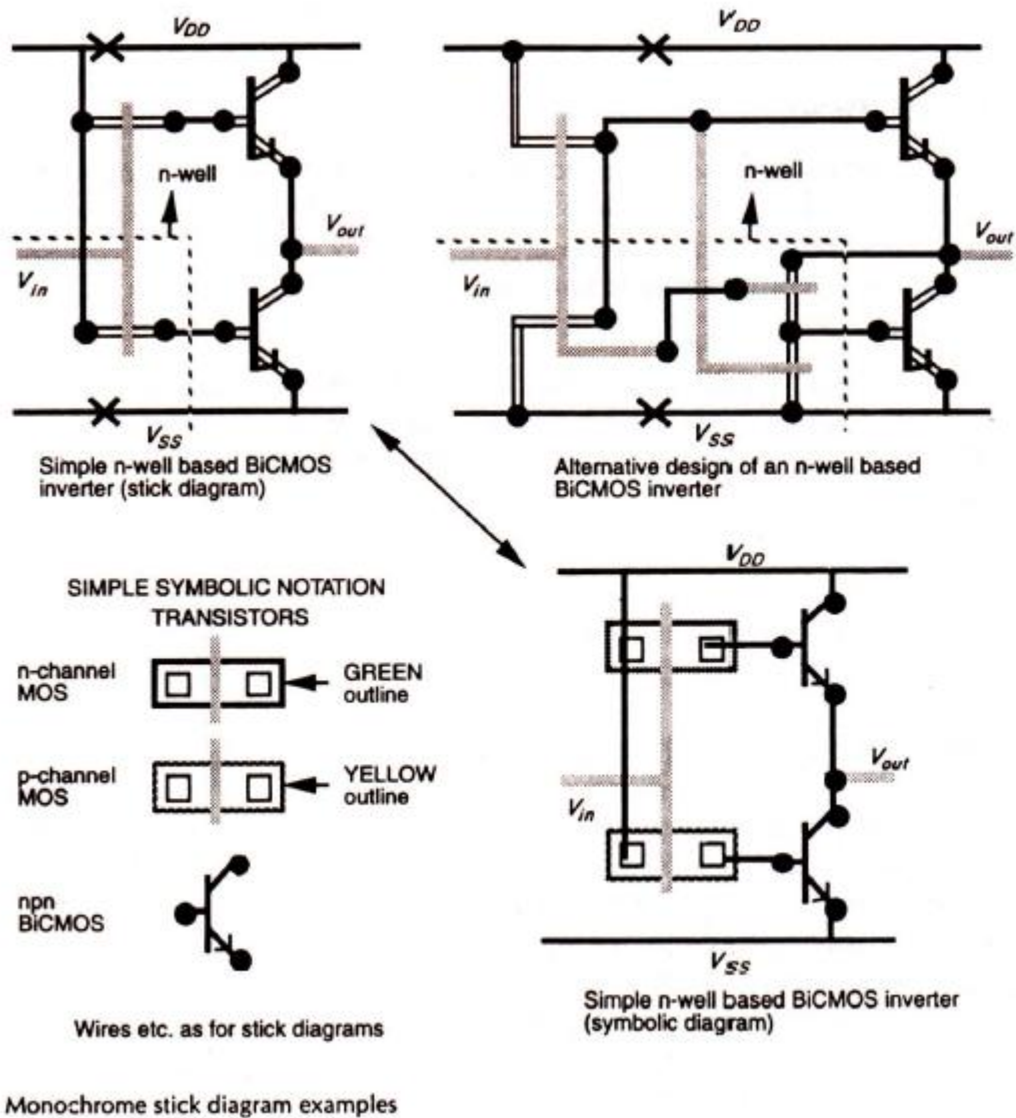
COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
	MONOCHROME		MONOCHROME	
ORANGE		Polysilicon 2		CPS
SEE COLOR PLATE 1(c)		Bipolar npn transistor	see Figure 3–13(f)	Not applicable
PINK	Not separately encoded	p-base of bipolar npn transistor		CBA
PALE GREEN	Not separately encoded	Buried collector of bipolar npn transistor	n-well	CCA

FEATURE	FEATURE (STICK) (MONOCHROME)	FEATURE (SYMBOL) (MONOCHROME)	FEATURE (MASK) (MONOCHROME)
n-type enhancement poly. 2 transistor	DEMARCATION LINE; L:W; S; D; G	GREEN; S; D; G; ORANGE	S; D; G
Transistor length to width ratio L:W may be shown.			
p-type enhancement poly. 2 transistor	L:W; DEMARCATION LINE	YELLOW; ORANGE	
Note: p-type transistors are placed above and n-type transistors below the demarcation line.			
npn bipolar transistor			See Figure 3–13(f) and Color plate 6

The same well encoding and demarcation line as in Figure 3–1(b) are used for an n-well process. For a p-well process, the n features are in the well. For an n-well process, the p features are in the well.

FIGURE 3.1(c) Additional encodings for a double metal double poly. BiCMOS n-well process (see Color plates 1(c) and 6 for additional CMOS and BiCMOS color encoding details).





Monochrome stick diagram examples

FIGURE 3.1(d) Stick diagrams and simple symbolic encoding (see also Color plate 1(d)).

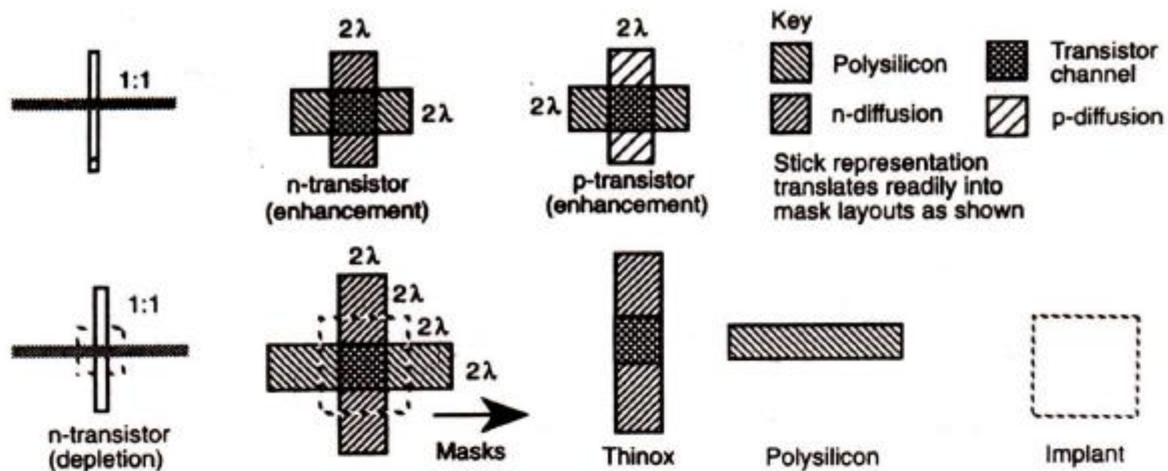


FIGURE 3.2 Stick diagrams and corresponding mask layout examples.

nMOS Design Style

In order to start with a relatively simple process, we will consider single metal, single polysilicon nMOS technology (see Figure 3.1(a) and Color plate l(a)).

A rational approach to stick diagram layout is readily adopted for such nMOS circuits and the approach recommended here is both easy to use and to turn into a mask layout. The layout of nMOS involves:

- n-diffusion [n-diff.] and other thinoxide regions [thinox] (green);
- polysilicon 1 [poly.]—since there is only one polysilicon layer here (red);
- metal 1 [metal]—since we use only one metal layer here (blue);
- implant (yellow);
- contacts (black or brown [buried]).

A transistor is formed wherever poly. crosses n-diff. (red over green) and all diffusion wires (interconnections) are n-type (green).

When starting a layout, the first step normally taken is to draw the metal (blue) V_{DD} and *GND* rails in parallel allowing enough space between them for the other circuit elements which will be required. Next, thinox (green) paths may be drawn between the rails for inverters and inverter-based logic as shown in Figure 3.3(a), not forgetting to make contacts as appropriate. Inverters and inverter-based logic comprise a pull-up structure, usually a depletion mode transistor, connected from the output point to V_{DD} and a pull-down structure of enhancement mode transistors suitably interconnected between the output point and *GND*. This step in the process is illustrated in Figure 3.3(b), remembering that poly. (red) crosses thinox (green) wherever transistors are required. Do not forget the implants (yellow) for depletion mode transistors and do not forget to write in the length to width (L:W) ratio for each transistor. Ratios are important, particularly in nMOS and nMOS-like circuits.

Signal paths may also be switched by pass transistors, and long signal paths may often require metal buses (blue). Allowing for the fact that the stick diagram may well represent only a small section of circuit which will be replicated many times, a convenient strategy is

to run power rails and bus(es) in parallel in metal (blue) and then propagate control signals at right angles on poly. as shown. At this stage of design, 'leaf-cell' boundaries are conveniently shown on the stick diagram and these are placed so that replicated cells may be directly interconnected by direct abutment on a side-by-side and/or top-to-bottom basis. The aspects just discussed are illustrated in Figure 3.3(c).

From the very beginning a design style should encourage the concepts of 'regularity' (through the use of replication) and generality so that design effort can be minimized and the interconnection of leaf-cells, subsystems and systems is facilitated.

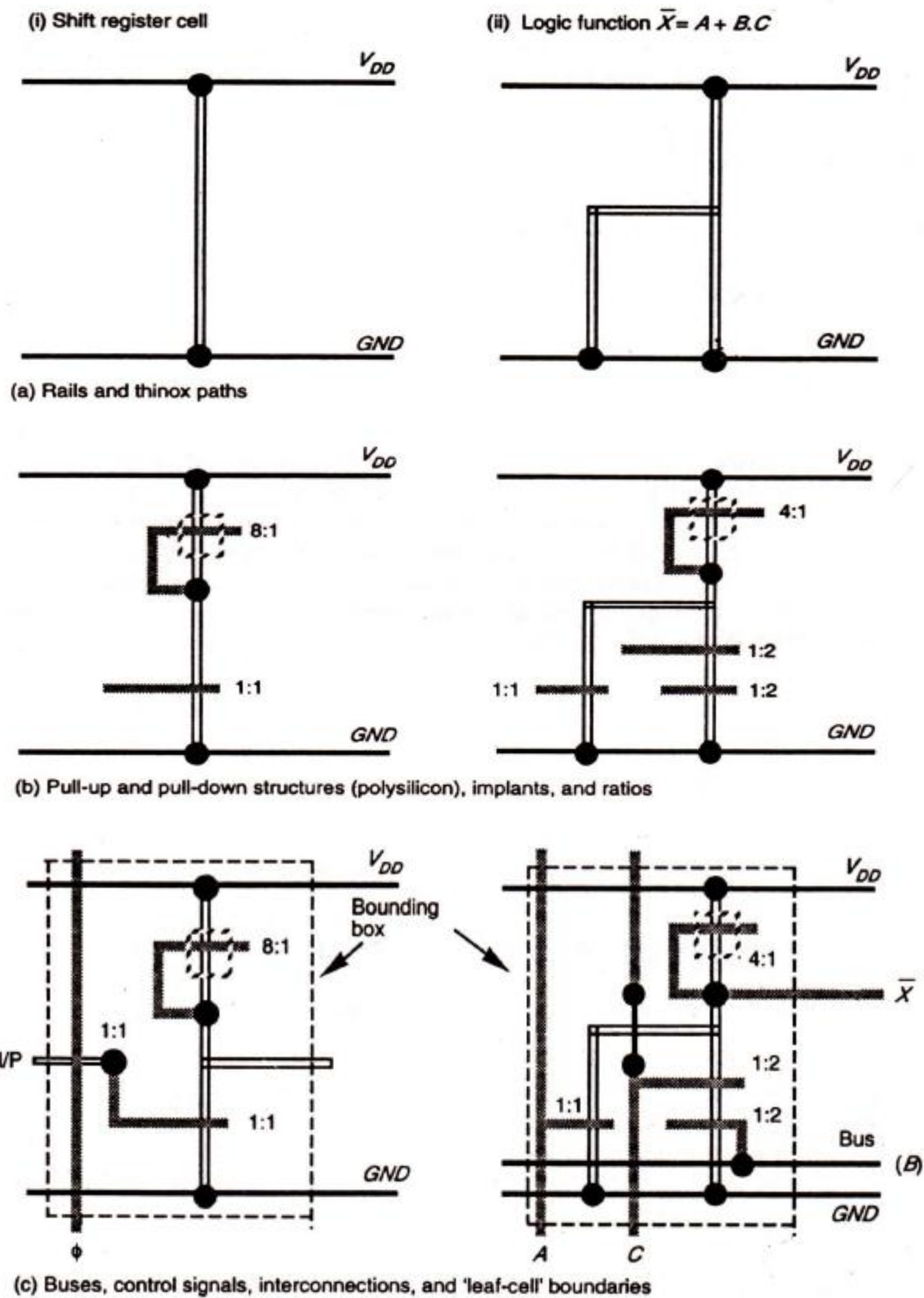


FIGURE 3.3 Examples of nMOS stick layout design style.

CMOS Design Style

The stick and layout representations for CMOS used in this text are a logical extension of the nMOS approach and style already outlined. They are based on the widely accepted work of Mead and Conway.

All features and layers defined in Figure 3.1, with the exception of implant (yellow) and the buried contact (brown), are used in CMOS design. Yellow in CMOS design is now used to identify p-transistors and wires, as depletion mode devices are not utilized. As a result, no confusion results from the allocation of the same color to two different features. The two types of transistor used, 'n' and 'p', are separated in the stick layout by the demarcation line (representing the p-well boundary) above which all p-type devices are placed (transistors and wires (yellow)). The n-devices (green) are consequently placed below the demarcation line and are thus located in the p-well. These factors are emphasized by Figure 3.4.

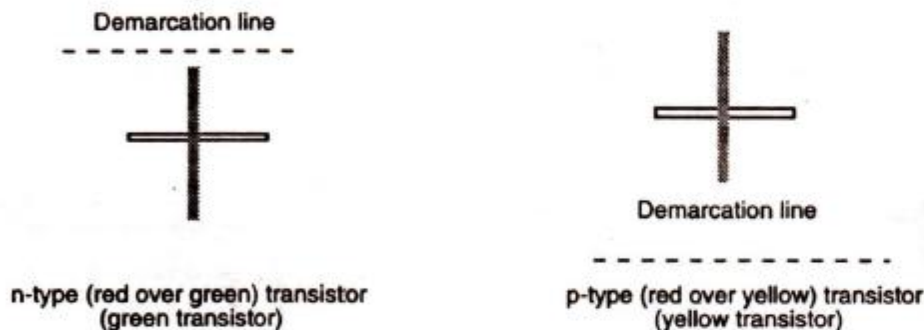
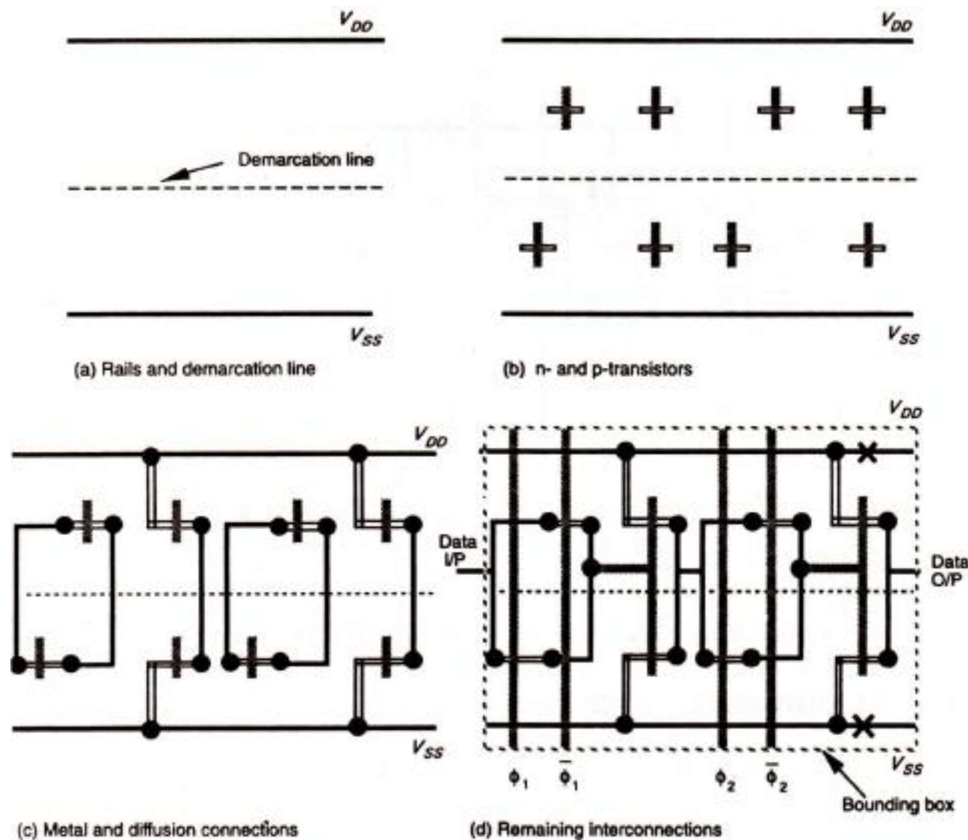


FIGURE 3.4 n-type and p-type transistors in CMOS design.

Diffusion paths must not cross the demarcation line and n-diffusion and p-diffusion wires must not join. The 'n' and 'p' features are normally joined by metal where a connection is needed. Apart from the demarcation line, there is no indication of the actual p-well topology at this (stick diagram) level of abstraction; neither does the p^+ mask appear. Their geometry will appear when the stick diagram is translated to a mask layout. However, we must not forget to place crosses on V_{DD} and V_{SS} rails to represent the substrate and p-well connection respectively. The design style is illustrated simply by taking as an example the design of a single bit of a shift register. The design begins with the drawing of the V_{DD} and V_{SS} rails in parallel and in metal and the creation of an (imaginary) demarcation line in between, as in Figure 3.5(a). The n-transistors are then placed below this line and thus close

to V_{SS}, while p-transistors are placed above the line and below V_{DD}. In both cases, the transistors are conveniently placed with their diffusion paths parallel to the rails (horizontal in the diagram) as shown in Figure 3.5(b). A similar approach can be taken with transistors in symbolic form.

A sound approach is to now interconnect the n- with the p-transistors as required, using metal and connect to the rails as shown in Figure 3.5(c). It must be remembered that only metal and polysilicon can cross the demarcation line but with that restriction, wires can run in diffusion also. Finally, the remaining interconnections are made as appropriate and the control signals and data inputs are added. These steps are illustrated in Figure 3.5(d).



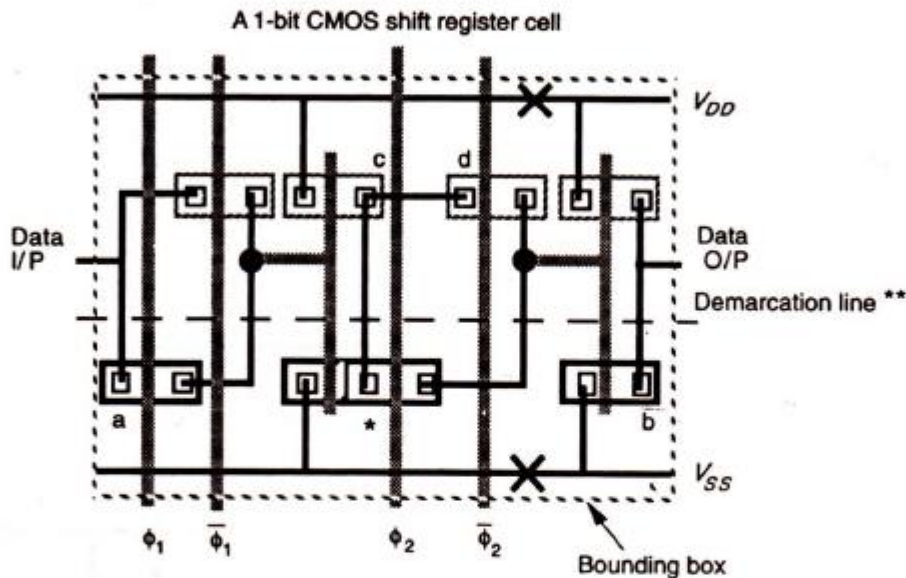
Note: The contact crosses in (d) should represent one V_{DD} contact for every four p-transistors and one V_{SS} contact for every four n-transistors.

FIGURE 3.5 Example of CMOS stick layout design style.

Although the circuit layout is now complete, we must not forget to represent the V_{SS} and V_{DD} contact crosses—one on the V_{DD} line for every four p-transistors and one on the V_{SS} line for every four n-transistors. The bounding box for the entire leaf-cell may also be shown if appropriate.

This design style is straightforward in application but later on we may recognize that sometimes transistors can be merged to advantage. We will also see how stick diagrams are turned into mask layouts, noting for CMOS layouts that the thinox mask includes all green features (n-devices) and all yellow features (p-devices) in the stick diagram.

An even simpler representation, which nevertheless carries much of the information present in a stick diagram, is to draw a symbolic diagram as in Figure 3.5(e). This diagram represents the same circuit as Figure 3.5(d) and the similarities are quite apparent. This form of diagram facilitates transistor merging, as shown, and is also readily translated to mask layouts.



* Note that two transistors (n-type) are merged as shown. When abutting cells, transistors a and b could also be merged. It is also possible to merge p-type transistors c and d etc.

** Demarcation line may be shown but is not essential since transistor symbols are already encoded.

FIGURE 3.5(e) Symbolic form of diagram (CMOS shift register).

DESIGN RULES AND LAYOUT

The object of a set of design rules is to allow a ready translation of circuit design concepts, usually in stick diagram or symbolic form, into actual geometry in silicon. The design rules are the effective interface between the circuit/system designer and the fabrication engineer. Clearly, both sides of the interface have a vested interest in making their own particular tasks as easy as possible and design rules usually attempt to provide a workable and reliable compromise that is friendly to both sides.

Circuit designers in general want tighter, smaller layouts for improved performance and decreased silicon area. On the other hand, the process engineer wants design rules that result in a *controllable and reproducible* process. Generally we find that there has to be a compromise for a competitive circuit to be produced at a reasonable cost.

One of the important factors associated with design rules is the achievable definition of the process line. Definition is determined by process line equipment and process design. For example, it is found that if a 10:1 wafer stepper is used instead of a 1:1 projection mask aligner, the level-to-level registration will be closer. Design rules can be affected by the maturity of the process line. For example, if the process is mature, then one can be assured of the process line capability, allowing tighter designs with fewer constraints on the designer.

The simple 'lambda (λ)-based' design rules set out first in this text are based on the invaluable work of Mead and Conway and have been widely used, particularly in the educational context and in the design of multiproject chips. The design rules are based on a single parameter λ which leads to a simple set of rules for the designer, and wide acceptance of the rules by a large cross-section of the fabrication houses and silicon brokers, and allows for scaling of the designs to a limited extent. This latter feature may help to give designs a longer lifetime. The simplicity of lambda-based rules also provides a simple introduction to design rules and to mask layout design in general and helps to set the scene for the 'micron-based' rule sets which follow.

Lambda-based Design Rules

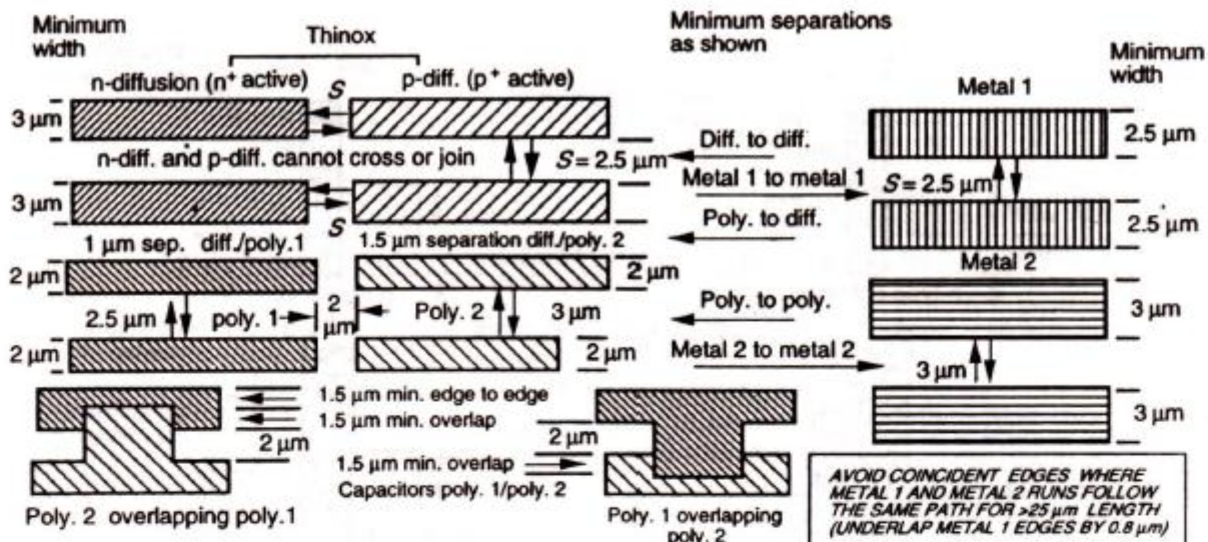
In general, design rules and layout methodology based on the concept of λ provide a process and feature size-independent way of setting out mask dimensions to scale.

All paths in all layers will be dimensioned in λ units and subsequently λ can be allocated an appropriate value compatible with the feature size of the fabrication process. This concept means that the actual mask layout design takes little account of the value subsequently allocated to the feature size, but the design rules are such that, if correctly obeyed, the mask layouts will produce working circuits for a range of values allocated to λ. For example, λ can be allocated a value of 1.0 μm so that minimum feature size on chip will be 2 μm (2λ). Design rules, also due to Mead and Conway, specify line widths, separations, and extensions in terms of λ, and are readily committed to memory.

2 μM DOUBLE METAL, DOUBLE POLY. CMOS/BICMOS RULES*

In order to accommodate the additional features present in this technology, it is necessary to extend the range of color and monochrome encodings previously used for double metal p-well CMOS. The encoding used is compatible with that already described, but as far as color assignments are concerned the following extension/additions are made: n-well—brown (same as p-well); Poly. 1—red; Poly. 2—orange; nDiff. (n-active)—green; pDiff. (p-active) —yellow (a green outline to the yellow may be used to show pDiff. clearly in color stick diagrams). Hatching, which is compatible with monochrome encoding, may also be added to color mask encoding, to distinguish underlying layers and to allow for ready copying of color diagrams on monochrome copying machines.

For BiCMOS the following are added: buried n^+ subcollector—pale green; p-base—pink. These extra features are set out in Figure 3.1(c) and in Color plate l(c). The monochrome encoded rule set for the Orbit™ 2 μm double metal double poly. BiCMOS process is given in Figures 3.13(a)–(f).



Otherwise polysilicon 2 must not be coincident with polysilicon 1

Note: Where no separation is specified, wires may overlap or cross (e.g. metal may cross any layer). For p-well CMOS, n-diff. wires can only exist inside and p-diff. wires outside the p-well. For n-well CMOS, p-diff. wires can only exist inside and n-diff. wires outside the n-well.

FIGURE 3.13(a) Design rules for wires (interconnects) (Orbit 2 μm CMOS).

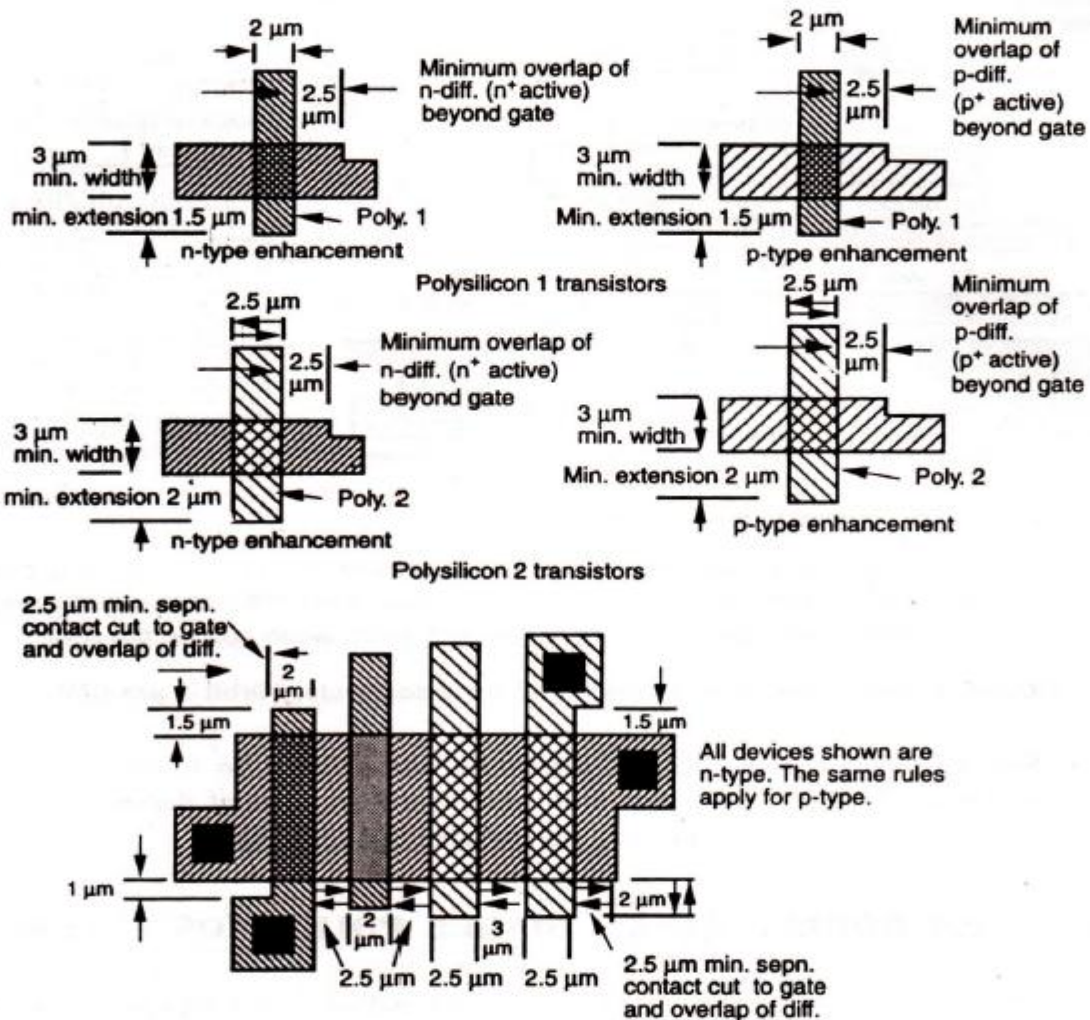
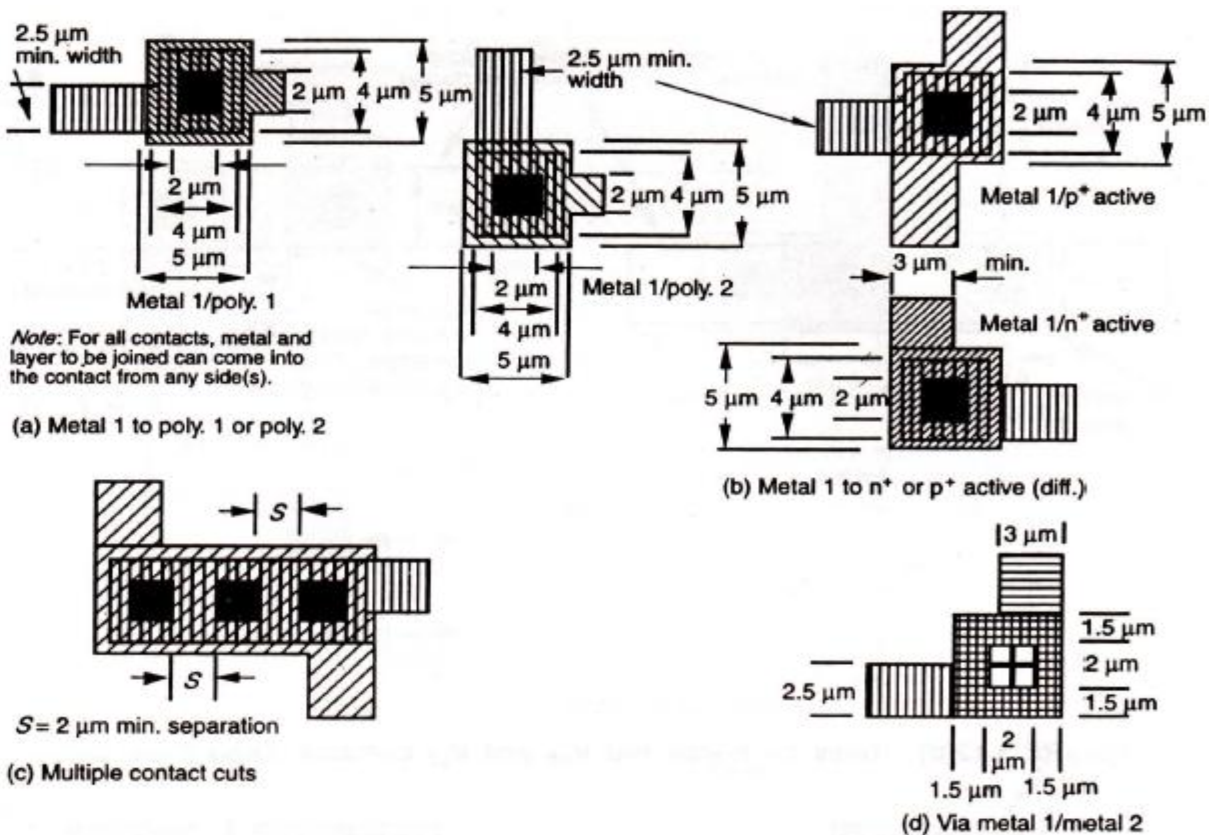
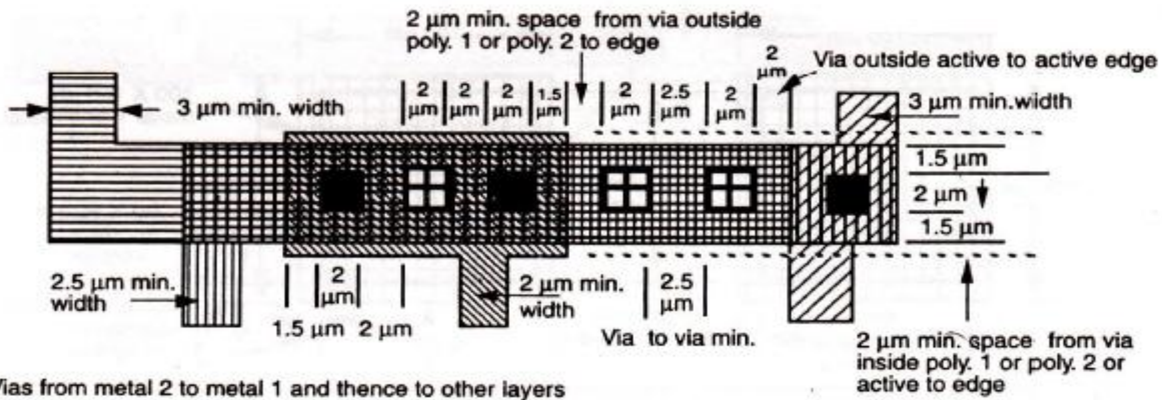


FIGURE 3.13(b) Transistor related design rules (Orbit 2 µm CMOS) minimum sizes and overlaps.





Note: The vias must not be placed over contacts

FIGURE 3.13(c) Rules for contacts and vias (Orbit 2 µm CMOS).

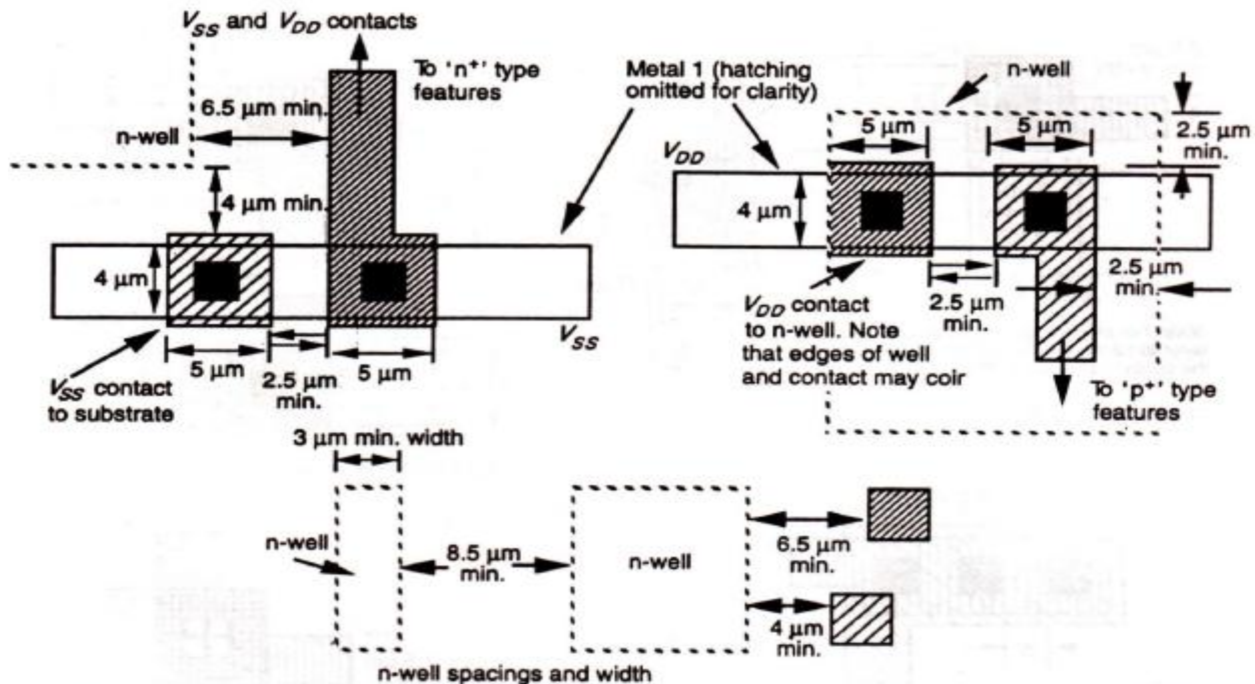
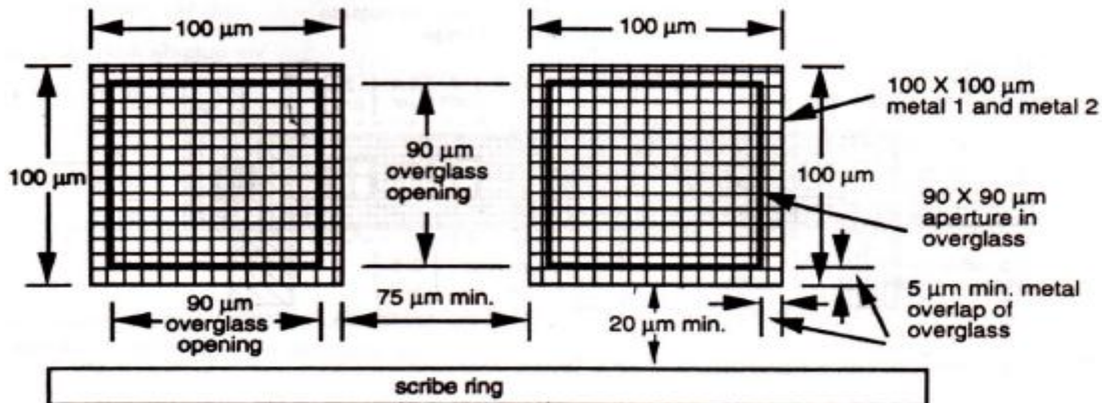
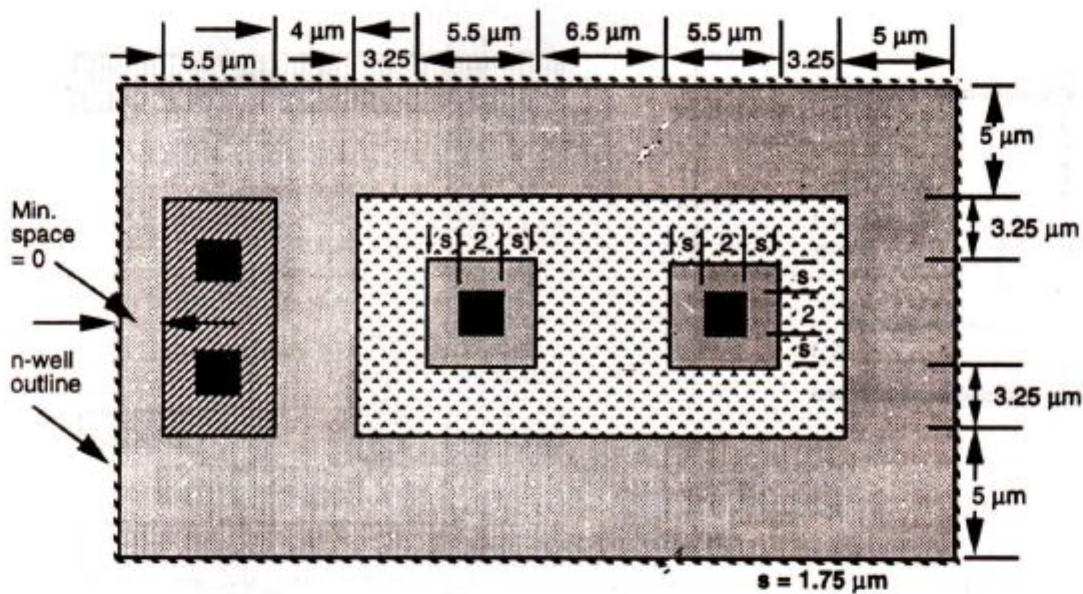


FIGURE 3.13(d) Rules for n-well and V_{DD} and V_{SS} contacts (Orbit 2 µm CMOS).

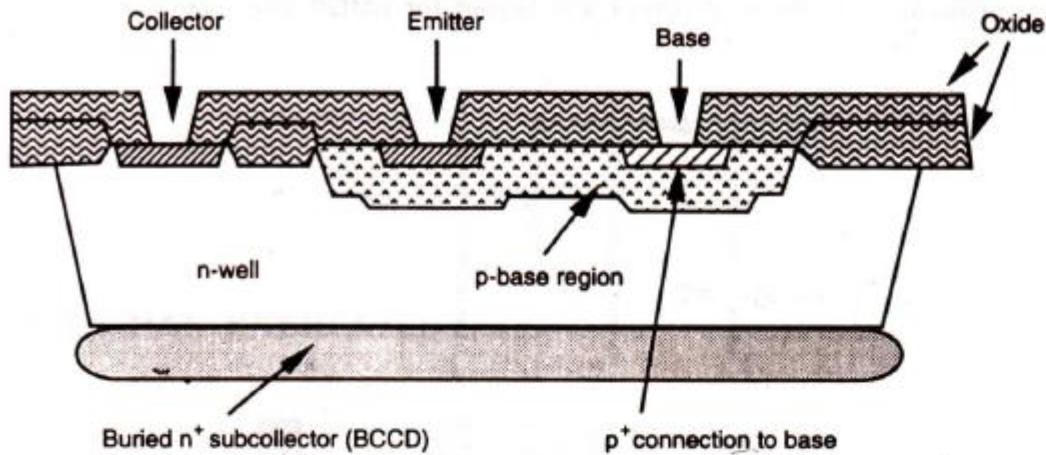


Other rules and encodings:
Via overlap of pad 2 µm.
Pad to active separation 20 µm min.
Color encoding for overglass mask . . . Gray

FIGURE 3.13(e) Rules for pad and overglass geometry (Orbit 2 µm CMOS).



Note: For clarity, the layers have not been drawn transparent but BCCD underlies the entire area and the p-base underlies all within its boundary.



Cross-section through npn transistor (Orbit 2 μm BiCMOS)

FIGURE 3.13(f) Special rules for BiCMOS transistors (Orbit 2 μm CMOS).

LAYOUT DIAGRAMS—A BRIEF INTRODUCTION

Mask layout diagrams may be hand-drawn on, say, 5 mm squared paper. In the case of lambda-based rules, the side of each square is taken to represent λ and, for micron-based rules, it will be taken to represent the least common factor associated with the rules (for example, 0.25 μm per side for the 2 μm process and 0.2 μm per side for the 1.2 μm Orbit™ process layout). Most CAD VLSI tools also offer convenient facilities for mask level design.

The introductory layout diagrams which follow in Figures 3.14 to 3.17 inclusive have been included to illustrate the use of the lambda-based rule set

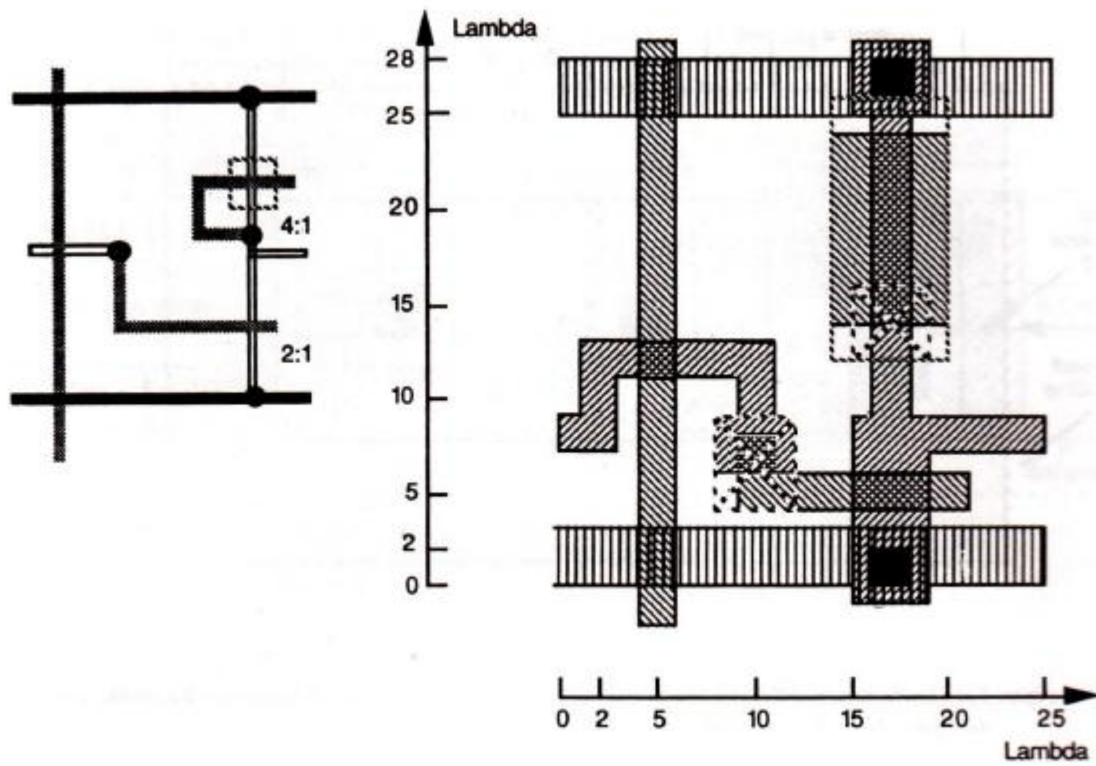


FIGURE 3.14 Stick diagram and layout for nMOS shift register cell.

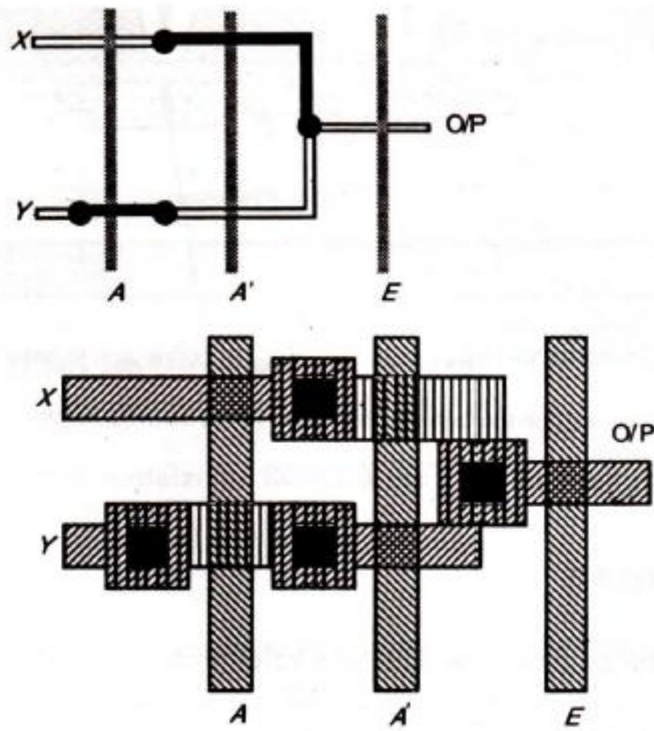


FIGURE 3.15 Two-way selector with enable.

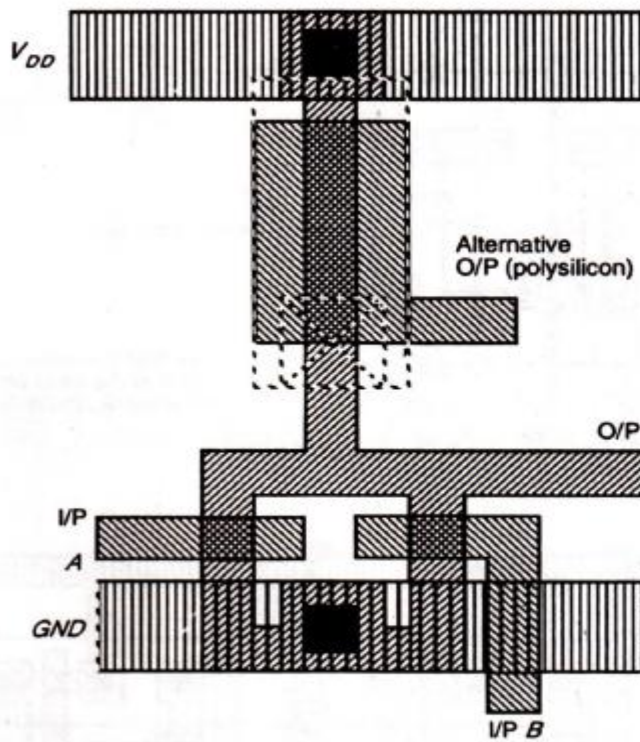
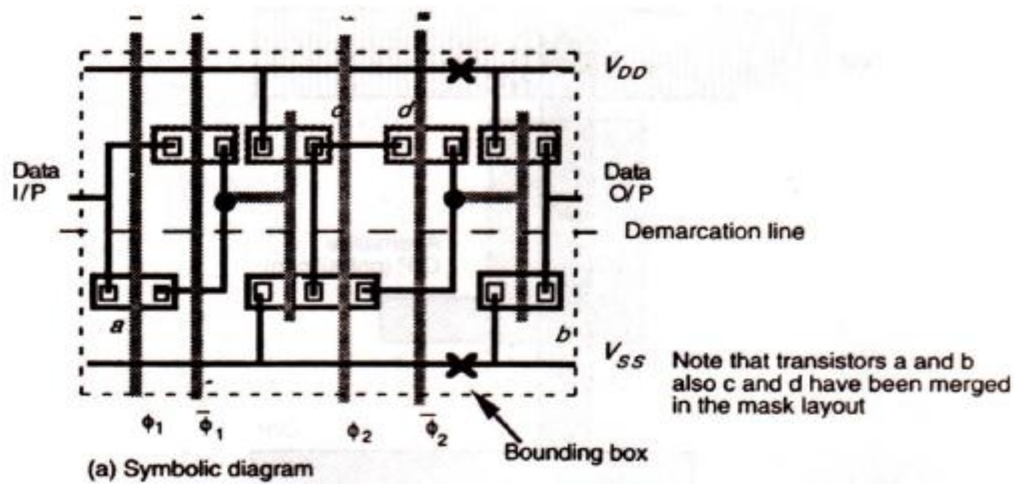
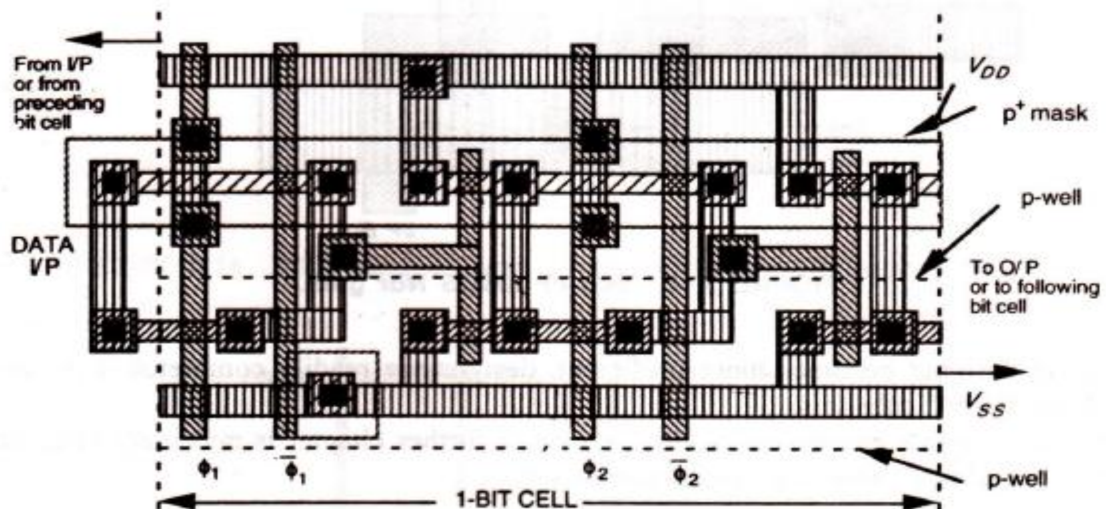


FIGURE 3.16 Two I/P nMOS *Nor* gate.



(a) Symbolic diagram



(b) Derived mask layout

FIGURE 3.17 A 1-bit CMOS shift register cell.

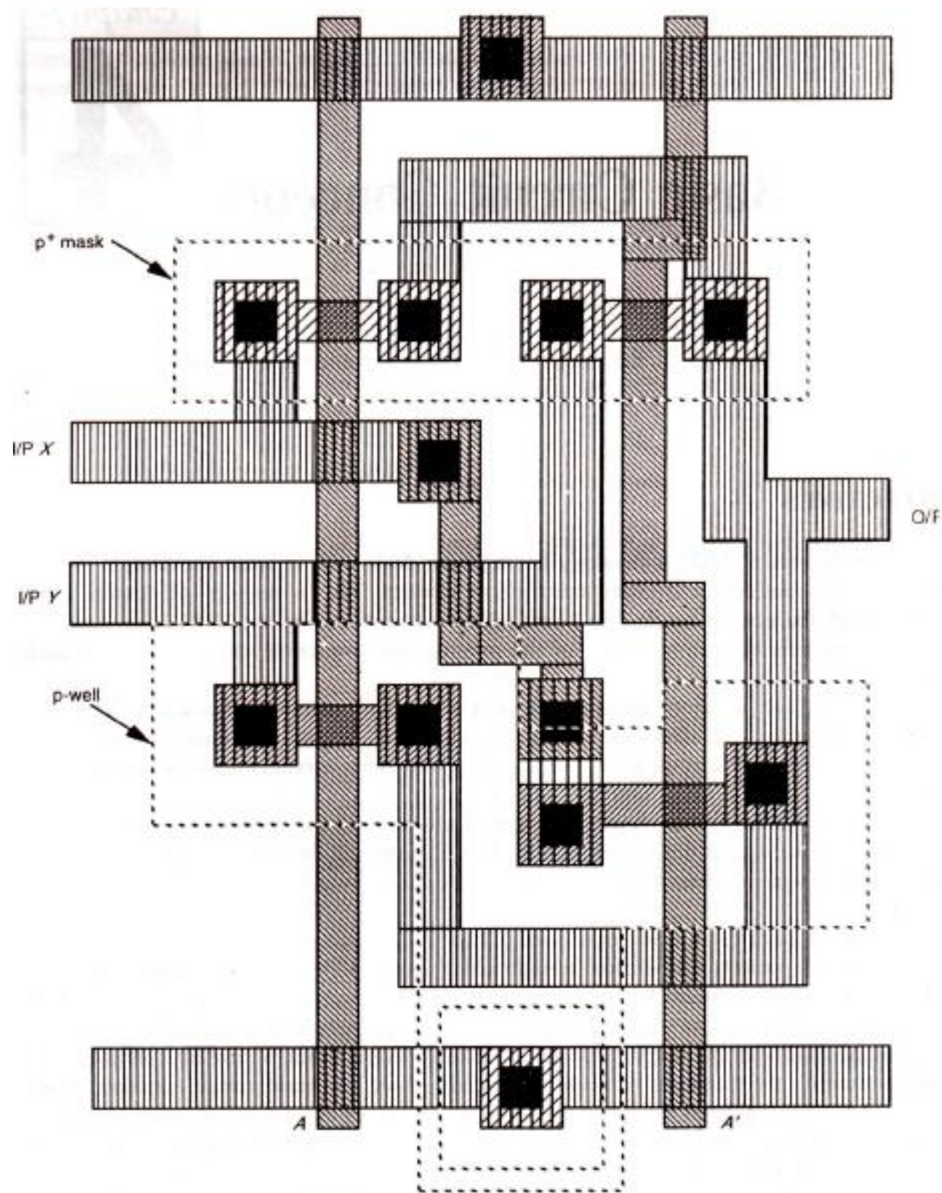


FIGURE 3.18 CMOS layout example.

Scaling of MOS Circuits

VLSI fabrication technology is still in the process of evolution which is leading to smaller line widths and feature size and to higher packing density of circuitry on a chip.

The scaling down of feature size generally leads to improved performance and it is important therefore to understand the effects of scaling. There are also future limits to scaling down which may well be reached in the next decade.

Microelectronic technology may be characterized in terms of several indicators, or figures of merit. Commonly, the following are used:

- Minimum feature size
- Number of gates on one chip
- Power dissipation
- Maximum operational frequency
- Die size
- Production cost.

Many of these figures of merit can be improved by shrinking the dimensions of transistors, interconnections and the separation between features, and by adjusting the doping levels and supply voltages. Accordingly, over the past decade, much effort has been directed toward the upgrading of process technology and the resultant scaling down of devices and feature size.

SCALING MODELS AND SCALING FACTORS

The most commonly used models are the constant electric field scaling model and the constant voltage scaling model. They both present a simplified view, taking only first degree effects into consideration, but are easily understood and well suited to educational needs.

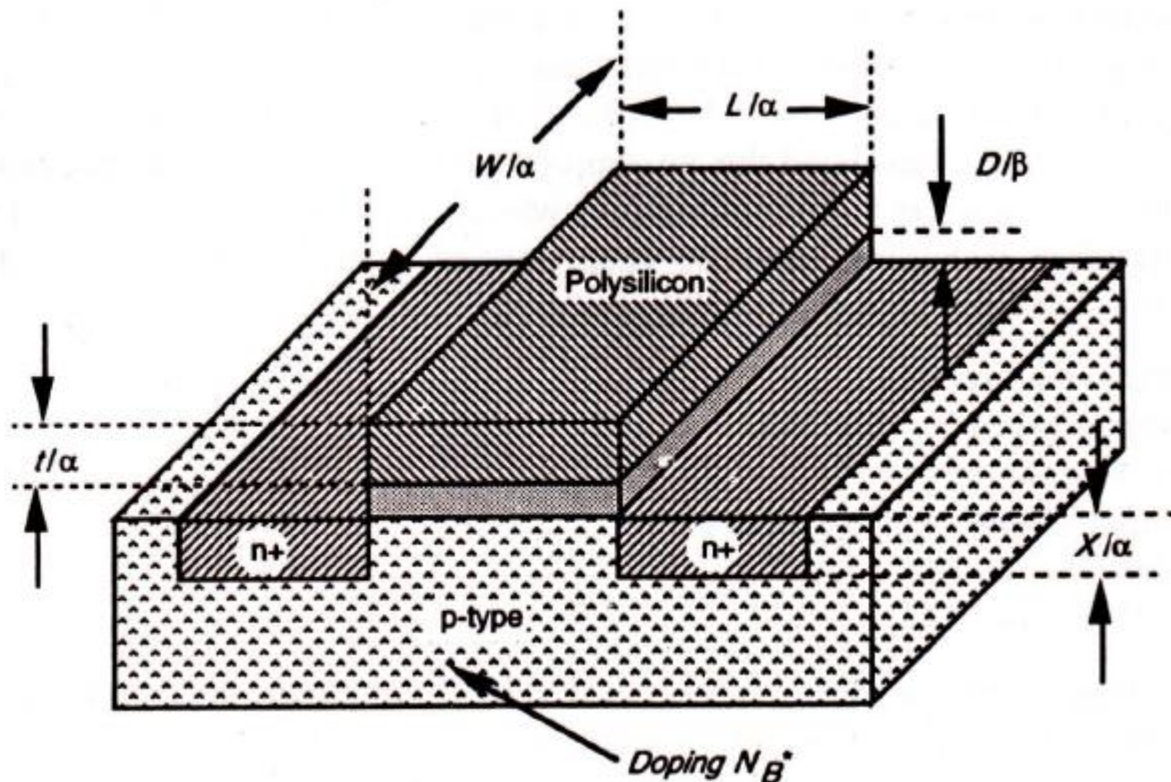


FIGURE 5.1 Scaled nMOS transistor (pMOS similar).

In order to accommodate the three models, two scaling factors—$1/\alpha$ and $1/\beta$—are used. $1/\beta$ is chosen as the scaling factor for supply voltage V_{DD} and gate oxide thickness D, and $1/\alpha$ is used for all other linear dimensions, both vertical and horizontal to the chip surface. For the constant field model and the constant voltage model, $\beta = \alpha$ and $\beta = 1$ respectively are applied.

SCALING FACTORS FOR DEVICE PARAMETERS

Gate Area A_g

$$A_g = L.W.$$

where L and W are the channel length and width respectively. Both are scaled by $1/\alpha$.
Thus A_g is scaled by $1/\alpha^2$

Gate Capacitance Per Unit Area C_0 or C_{ox}

$$C_0 = \frac{\varepsilon_{ox}}{D}$$

where ε_{ox} is the permittivity of the gate oxide (thinox) $[= \varepsilon_{ins.}\varepsilon_0]$ and D is the gate oxide thickness which is scaled by $1/\beta$

Thus C_0 is scaled by $\frac{1}{1/\beta} = \beta$

Gate Capacitance C_g

$$C_g = C_0 L.W.$$

Thus C_g is scaled by $\beta \frac{1}{\alpha^2} = \frac{\beta}{\alpha^2}$

Parasitic Capacitance C_x

C_x is proportional to $\frac{A_x}{d}$

where d is the depletion width around source or drain which is scaled by $1/\alpha$, and A_x is the area of the depletion region around source or drain which is scaled by $1/\alpha^2$.

Thus C_x is scaled by $\frac{1}{\alpha^2} \cdot \frac{1}{1/\alpha} = \frac{1}{\alpha}$

Carrier Density in Channel Q_{on}

$$Q_{on} = C_0 \,.\, V_{gs}$$

where Q_{on} is the average charge per unit area in the channel in the 'on' state. Note that C_0 is scaled by β and V_{gs} is scaled by $1/\beta$.

Thus Q_{on} is scaled by 1

Channel Resistance R_{on}

$$R_{on} = \frac{L}{W} \frac{1}{Q_{on}\mu}$$

where μ is the carrier mobility in the channel and is assumed constant.

Thus R_{on} is scaled by $\frac{1}{\alpha} \frac{1}{1/\alpha} 1 = 1$

Gate Delay T_d

T_d is proportional to $R_{on} \,.\, C_g$

Thus T_d is scaled by $\frac{1.\beta}{\alpha^2} \frac{\beta}{\alpha^2}$

Maximum Operating Frequency f_0

$$f_0 = \frac{W}{L} \frac{\mu C_0 V_{DD}}{C_g}$$

or, f_0 is inversely proportional to delay T_d.

Thus f_0 is scaled by $\frac{1}{\beta/\alpha^2} = \frac{\alpha^2}{\beta}$

Saturation Current I_{dss}

$$I_{dss} = \frac{C_0 \mu}{2} \frac{W}{L} (V_{gs} - V_t)^2$$

noting that both V_{gs} and V_t are scaled by $1/\beta$, we have

$$I_{dss} \text{ is scaled by } \beta(1/\beta)^2 = 1/\beta$$

Current Density J

$$J = \frac{I_{dss}}{A}$$

where A is the cross-sectional area of the channel in the 'on' state which is scaled by $1/\alpha^2$

So, J is scaled by $\dfrac{1/\beta}{1/\alpha^2} = \dfrac{\alpha^2}{\beta}$

Switching Energy Per Gate E_g

$$E_g = \frac{1C_g}{2} (V_{DD})^2$$

So, E_g is scaled by $\dfrac{\beta}{\alpha^2} \cdot \dfrac{1}{\beta^2} = \dfrac{1}{\alpha^2 \beta}$

Power Dissipation Per Gate P_g

P_g comprises two components such that

$$P_g = P_{gs} + P_{gd}$$

where the static component

$$P_{gs} = \frac{(V_{DD})^2}{R_{on}}$$

and the dynamic component

$$P_{gd} = E_g f_0$$

It will be seen that both P_{gs} and P_{gd} are scaled by $1/\beta^2$

So, P_g is scaled by $1/\beta^2$

Power Dissipation Per Unit Area P_a

$$P_a = \frac{P_g}{A_g}$$

So, P_a is scaled by $\frac{1/\beta^2}{1/\alpha^2} = \alpha^2/\beta^2$

Power-speed Product P_T

$$P_T = P_g \, . \, T_d$$

So, P_T is scaled by $\frac{1}{\beta^2} \cdot \frac{\beta}{\alpha^2} = \frac{1}{\alpha^2\beta}$

Summary of Scaling Effects

Parameters		*Combined V and D*	*Constant E*	*Constant V*
V_{DD}	Supply voltage	$1/\beta$	$1/\alpha$	1
L	Channel length	$1/\alpha$	$1/\alpha$	$1/\alpha$
W	Channel width	$1/\alpha$	$1/\alpha$	$1/\alpha$
D	Gate oxide thickness	$1/\beta$	$1/\alpha$	1
A_g	Gate area	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha^2$
C_0(or C_{ox})	Gate C per unit area	β	α	1
C_g	Gate capacitance	β/α^2	$1/\alpha$	$1/\alpha^2$
C_x	Parasitic capacitance	$1/\alpha$	$1/\alpha$	$1/\alpha$
Q_{on}	Carrier density	1	1	1
R_{on}	Channel resistance	1	1	1
I_{dss}	Saturation current	$1/\beta$	$1/\alpha$	1
A_c	Conductor X-section area	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha^2$
I	Current density	α^2/β	α	α^2
V_g	Logic 1 level	$1/\beta$	$1/\alpha$	1
E_g	Switching energy	$1/\alpha^2.\beta$	$1/\alpha^3$	$1/\alpha^2$
P_g	Power dispn per gate	$1/\beta^2$	$1/\alpha^2$	1
N	Gates per unit area	α^2	α^2	α^2
P_a	Power dispn per unit area	α^2/β^2	1	α^2
T_d	Gate delay	β/α^2	$1/\alpha$	$1/\alpha^2$
f_0	Max. operating frequency	α^2/β	α	α^2
P_T	Power-speed product	$1/\alpha^2.\beta$	$1/\alpha^3$	$1/\alpha^2$

Constant E: $\beta = \alpha$; Constant V: $\beta = 1$