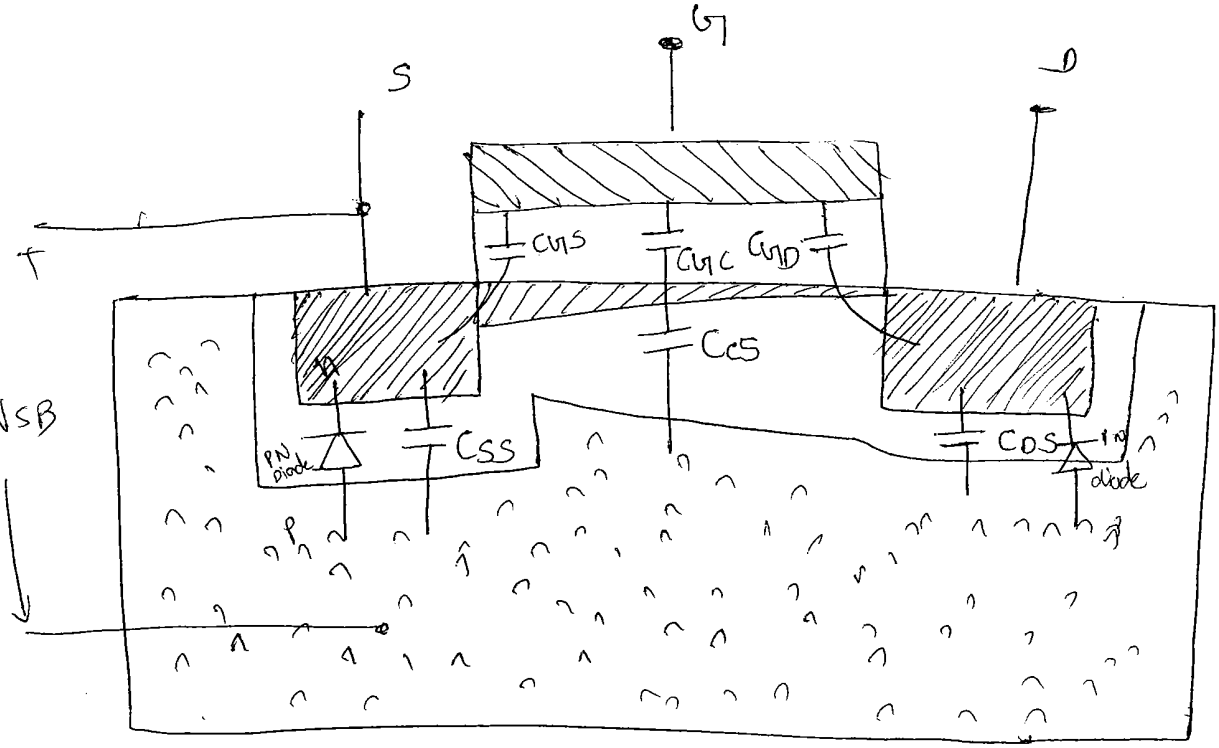
MOS Tr circuit model :-

→ The MOS Tr can be modeled with varying degrees of complexity. (X) consideration of actual physical construction of the device leads to some understanding of various components of the model.



nmos Tr model

C_{GC} → gate to channel capacitance
C_{GS} → gate to source
C_{GD} → gate to drain

} small for self-aligned process.

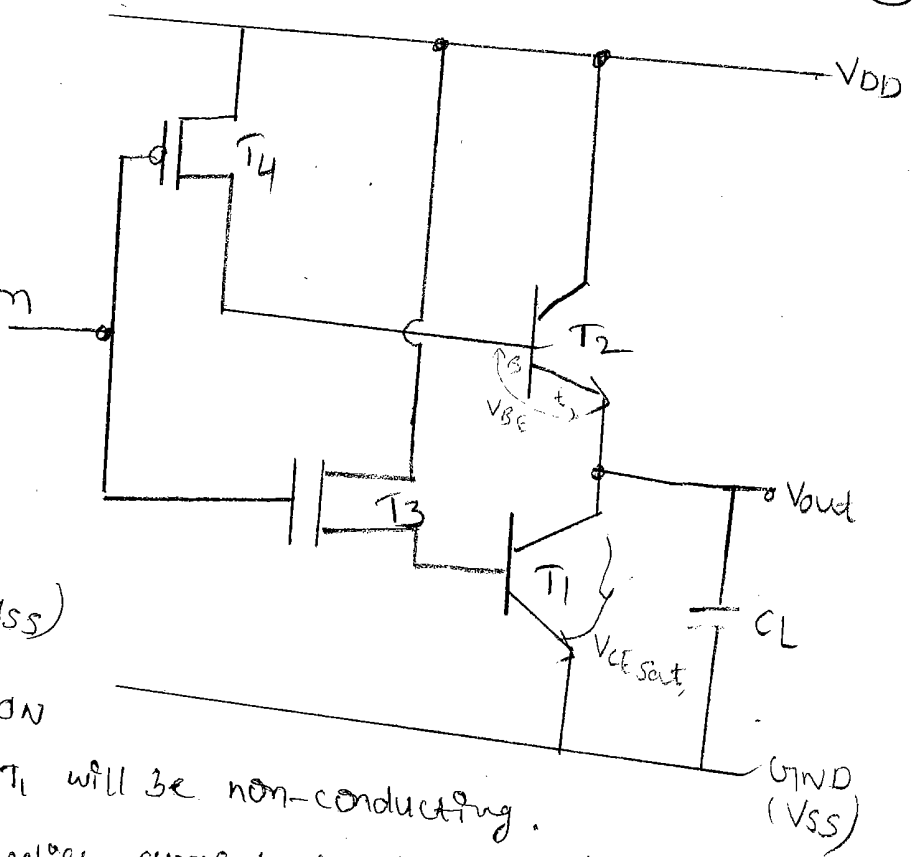
Remaining capacitances are associated with depletion layer & voltage dependent.

C_{SS} → source to substrate capacitance
C_{DS} → drain to substrate
C_{CS} → channel to substrate

Bi-cmos inverter:-

→ It consists of 2 Bi-Polar Transistors T_1, T_2.

→ And 1 nmos T_3, 1 pmos T_4. Both are enhancement mode T_s.



Case 1:- Logic 0 i/p.

With Vin = 0 (VSS)

T_3 → off & T_4 − ON

So, As T_3 is off T_1 will be non-conducting.

→ T_4 is on and supplies current to the base of T_2 which will conduct & act as a current source to charge the load C_L toward +5V (VDD). [a current source to charge the load C_L to(wa&d)]

The o/p of inverter will rise to +5V. less the Base-to-emitter voltage V_{BE} of T_2. ie. $V_{DD} - V_{BE}$ = Logic 1

Case 2; With Vin = +5V (VDD)

T_4 → off so that T_2 is non-conducting.

T_3 is on & will supply current to the base of T_1 which will conduct & act as a current sink to the load C_L discharging it toward 0V.

The o/p of inverter will fall to 0V plus the saturation voltage V_{CEsat} from the collector to the emitter of T_1.

(2) i.e., $0V + V_{CEsat}$ = Logic 0.

→ T_1 & T_2 will present low impedance when turned on into saturation and the load CL will be charged & discharged rapidly.

→ The o/p logic levels will be good and will be close to the rail voltages (VDD, VSS) since V_{CEsat} is quite small & $V_{BE} \cong +0.7V$.

$(V_{SS})\ 0 \cong V_{CEsat}$ $\quad 5 - 0.7 \cong V_{DD}$.

→ The inverter has high i/p impedance.

→ The inverter has low o/p impedance.

→ The inverter has high noise margins.

→ Due to the presence of a DC path from VDD to GND through T_3 & T_1, this is not a good arrangement to implement since there will be significant static current flow whenever Vin = logic 1.

→ Problem: There is no discharge path for current from the base of either BJT when it is being turned off. This will slow down the action of this circuit.

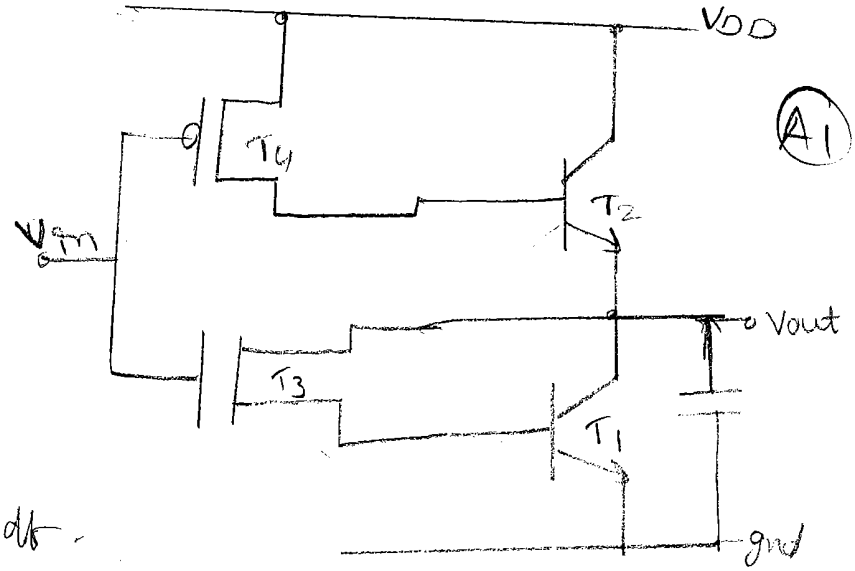
TO avoid this, improved version of the circuit used:

⇒ DC path through T_3 & T_1 is eliminated.

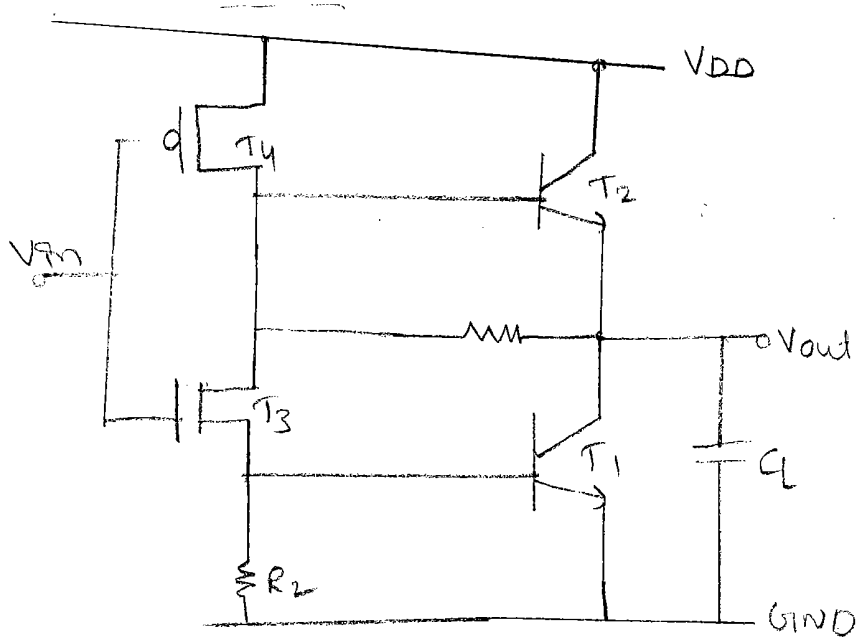
⇒ But, o/p voltage swing is now reduced, since the o/p

cannot fall below the V_{BE} of T_1. (B)

→ An improved inverter arrangement with resistor provide the improved swing of o/p voltage when each bipolar Tr is off & also provide discharge path for base current during turn-off.

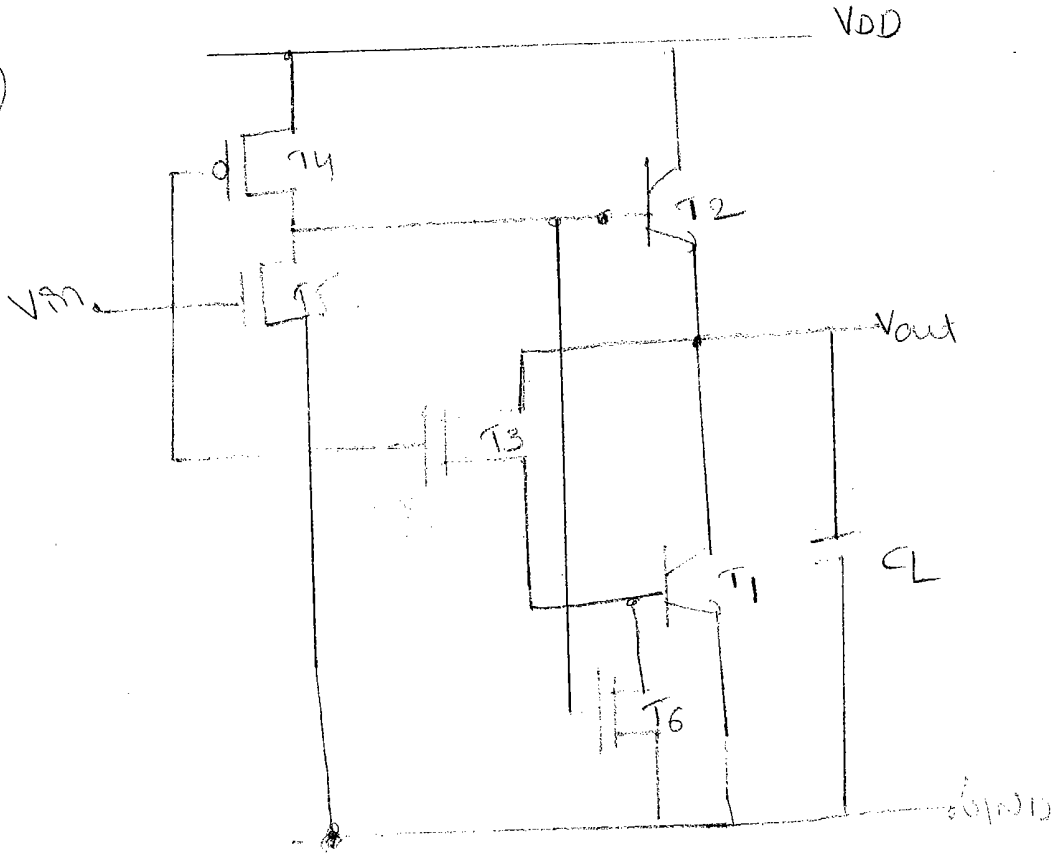


(A1)

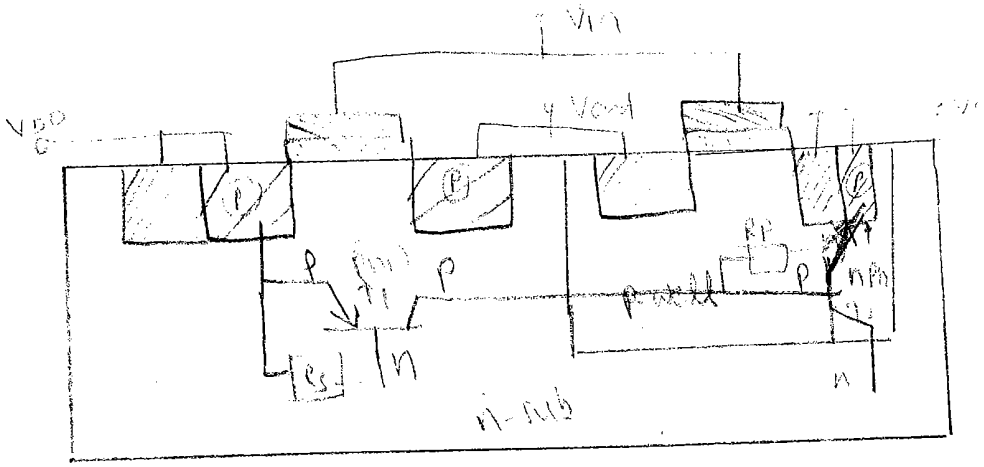


→ The provision of on-chip resistor of suitable value is not always convenient and may be space-consuming. To avoid this, another arrangement in that, T_5 & T_6 are arranged to turn on when T_2 & T_1 respectively are being turned off.

A2



Latch up in cmos circuits :-



→ A problem which is inherent in p-well & n-well process due to the large no. of junctions which are formed in these structures. The consequent presence of parasitic T's & diodes.

Latch up : is a condition in which the parasitic component give rise to the establishment of low-resistance conducting path between Vdd & Vss.

Problems :-

① Find g_m and r_{ds} for an n-channel transistor with $V_{gs} = 1.2V$, $V_{tn} = 0.8V$, $\frac{W}{L} = 10$, $\mu_n C_{ox} = 92 \mu A/V^2$ & $V_{ds} = V_{eff} + 0.5V$. The output impedance constant $= 95.3 \times 10^{-3}/V$.

Sol:

$$\lambda = 95.3 \times 10^{-3}/V$$

$$V_{ds} = V_{eff} + 0.5V$$

where

$$V_{eff} = V_{gs} - V_{tn}$$

$$= 1.2 - 0.8$$

$$= 0.4V$$

$\therefore V_{ds} = 0.4 + 0.5 = 0.9V$

$0.9 > 0.4$

$V_{ds} > V_{gs} - V_{th}$

So, T_r is in saturation region,

$$I_d = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{gs} - V_{tn})^2$$

Transconductance, $g_m = \frac{C_g \mu}{L^2} V_{ds}$

$C_g = C_{ox} WL$ (C_{ox} = unit capacitance)

$\therefore g_m = \frac{\mu_n C_{ox} WL}{V_{ds}}$

$= \mu_n C_{ox} \frac{W}{L} V_{ds}$

$= 92 \times 10^{-6} \times 0.9 \times 10$

$\boxed{g_m = 8.28 \times 10^{-4} \mho}$

Drain to Source resistance, $r_{ds} = \frac{1}{\partial I_{ds}}$

$I_{ds} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{gs} - V_{th})^2$

$= \frac{92 \times 10^{-6}}{2} \times 10 (0.4)^2$

$= 7.36 \times 10^{-5} A$

$\therefore r_{ds} = \frac{1}{95.3 \times 10^{-3} \times 7.36 \times 10^{-5}}$

$= 142.57 k\Omega$

11
2, 3, 4, 5, 6, 7, 8, 9 (1)

If $\beta_n = \beta_p$ & $V_{tn} = -V_{tp}$

then

$$V_{in} = \frac{V_{DD} + V_{tp} - V_{tp}\left(\sqrt{\frac{\beta_n}{\beta_n}}\right)}{1 + \left(\sqrt{\frac{\beta_n}{\beta_p}}\right)}$$

$$V_{in} = \frac{V_{DD}}{1+1} = \frac{V_{DD}}{2} = 0.5 V_{DD}.$$

→ change over b/w logic levels is symmetrically disposed about the point at which

$$\boxed{V_{in} = V_{out} = 0.5 V_{DD}}$$

since only at this At will the 2 'β' factors be equal.

But for $\beta_n = \beta_p$, the device geometries must be such that

$$\beta_n = \beta_p$$

$$\frac{\epsilon_0 \epsilon_r l_n w_n}{D\, L_n} = \frac{\epsilon_0 \epsilon_r l_p w_p}{L_p}$$

$$\frac{l_n w_n}{L_n} = \frac{l_p w_p}{L_p}.$$

we know, $l_n = 2.5 l_p$.

$$\frac{2.5 \cancel{l_p} w_n}{L_n} = \frac{\cancel{l_p} w_p}{L_p}$$

$$\boxed{\frac{w_p}{L_p} \simeq 2.5 \frac{w_n}{L_n}}$$

width to Length ratio of P-device is to be 2 to 3 time that of n-device.

→ mobility (μ) affected by transverse electric field [illegible]

dependent on V_{gs}.

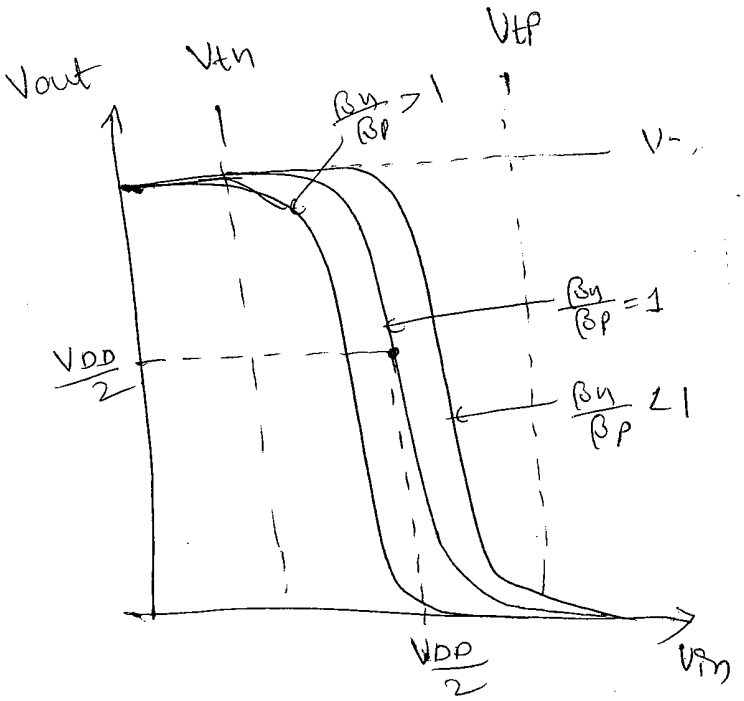
actual mobility is, $\mu = \mu_z (1 - \phi (V_{gs} - V_t))^{-1}$

(a) $\phi \rightarrow$ constant $\cong 0.05$.

$\mu_z \rightarrow$ mobility with zero transverse field.

β ratio of $\left(\frac{\beta_n}{\beta_p} = 1\right)$ will only hold good around the pt of symmetry when $V_{out} = V_{in} = 0.5 V_{DD}$.

→



Trends in transfer c/s with β ratio

Region 4 :— the input voltage of P-Tr must exceed threshold voltage. The P-Tr conducts but large voltage b/w source and drain.

So P-Tr saturation,

→ The n-Tr conducting with a small voltage across it, it operates in resistive region.

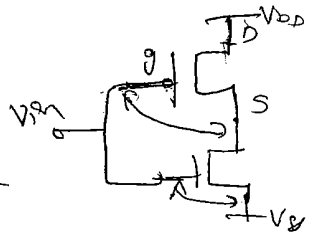
→ Currents in region 2 & 4 are small. Most of energy consumed in switching from one state to another.

In region 3 both Trs are in saturation. The currents in each device must be same since Trs are in series,

$$I_{dsp} = -I_{dsn}$$

$$I_{ds} = \frac{\beta}{2}(V_{gs}-V_t)^2$$

$$I_{dsp} = \frac{\beta_p}{2}(V_{in}-V_{DD}-V_{tp})^2$$



& $I_{dsn} = \frac{\beta_n}{2}(V_{in}-V_{SS}-V_{tn})^2$

$$\frac{\beta_p}{2}(V_{in}-V_{DD}-V_{tp})^2 = -\frac{\beta_n}{2}(V_{in}-V_{tn})^2$$

$$(V_{in}-V_{DD}-V_{tp})^2 = \frac{\beta_n}{\beta_p}(V_{in}-V_{tn})^2$$

$$V_{in}-V_{DD}-V_{tp} = -\sqrt{\frac{\beta_n}{\beta_p}}(V_{in}-V_{tn})$$

$$V_{in}+\sqrt{\frac{\beta_n}{\beta_p}}V_{in} = V_{DD}+V_{tp}+\sqrt{\frac{\beta_n}{\beta_p}}V_{tn}$$

$$V_{in} = \frac{V_{DD}+V_{tp}+V_{tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1+\sqrt{\frac{\beta_n}{\beta_p}}}$$

CMOS inverter :—

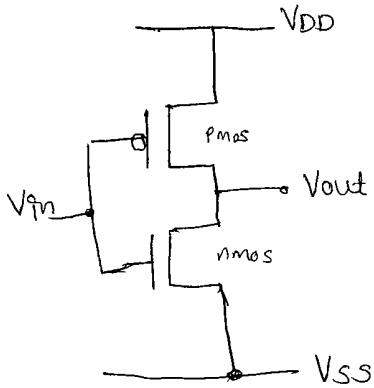
we have seen, current - voltage relationships for MOS Tr's,

$$Ids = \frac{kw}{L}\left((Vgs - Vt)Vds - \frac{Vds^2}{2}\right)$$

In resistive region or non-saturation region,

$$Ids = \frac{kw}{L}\frac{(Vgs - Vt)^2}{2}$$

in saturation region.



(5)

circuit

→ In both cases, the factor K is a Technology - dependent parameter such that,

$$K = \frac{\epsilon_0 \epsilon_{rel}}{D}$$

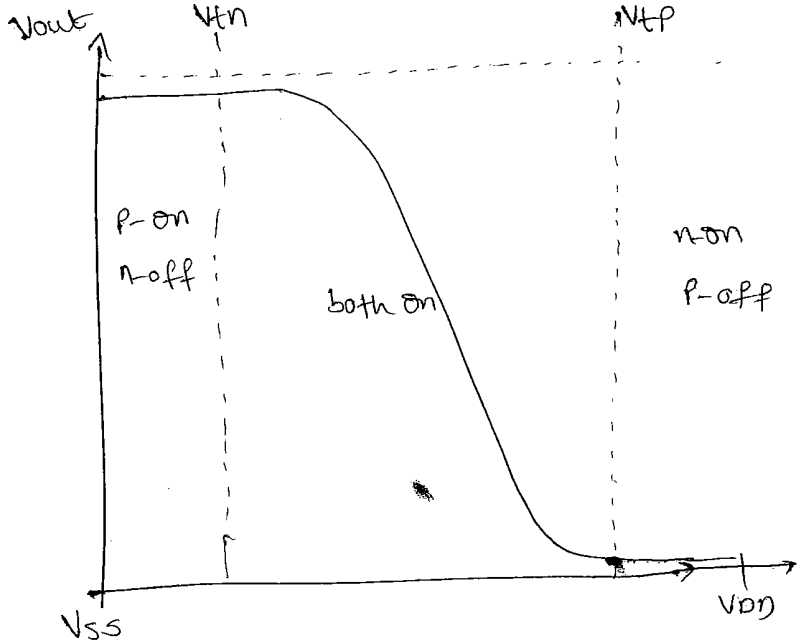
& $\beta = \frac{kw}{L}$

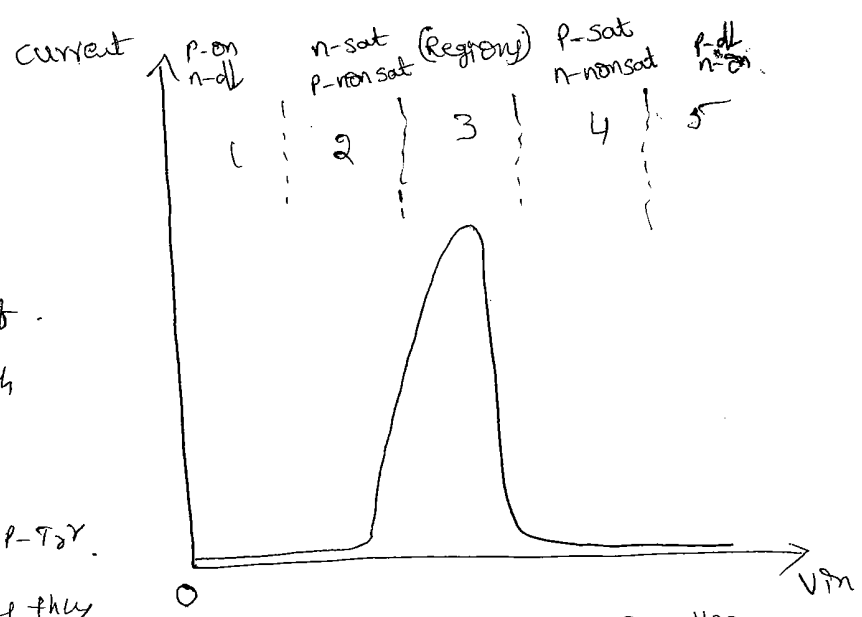
β may be applied to both nmos & pmos Tr's as follows,

$$\beta_n = \frac{\epsilon_0 \epsilon_{reln}}{D}\frac{w_n}{L_n}$$

$$\beta_p = \frac{\epsilon_0 \epsilon_{relp}}{D}\cdot\frac{w_p}{L_p}$$

where ~~βn + βp~~ w_n, L_n & w_p L_p are n-Tr & p-Tr dimensions





In region 1 :-

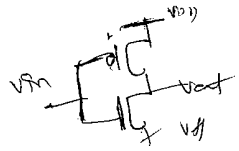
For which Vin = Logic 0.

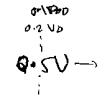
We have P-Tr fully turned on while n-Tr fully turned off.

Thus no current flows through inverter & o/p is directly connected to VDD through P-Tr.

A good logic 1 o/p voltage is thus present at the o/p.

Vin	P	n
Logic 0	on	off
$< V_{tp}$	non-sat	sat





In region 5 :-

Vin = Logic 1, the n-Tr is fully on while P-Tr is fully off. Again, no current flows & good logic 0 appears at o/p.

In region 2 :- i/p voltage has increased to a level which just exceeds the threshold voltage of n-Tr. ($V_{in} > V_{tn}$), & it is in saturation region. ($V_{ds} \geq V_{gs} - V_t$)

The n-Tr conducts & a large voltage b/w source & drain (V_{ds}).

→ The P-Tr also conducts but a small voltage across it, ($V_{ds} < V_{gs} - V_t$)

it is in non-saturated or resistive region.

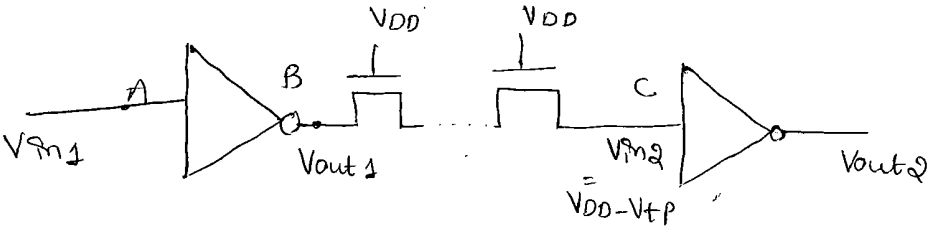
→ A small current flows through the inverter from VDD to Vss.

→ If we wish to analyze behaviour in this region,

P-device non-saturation current = n device saturation current.

In region 3 :- is the region in which inverter exhibits gain & both Tr's are in saturation region.

Pull-up to Pull-down ratio for an nmos inverter driven through one or more pass transistors :-



Input 2 to inverter 2 comes from the o/p of inverter 1 but passes through one or more nmos transistors used as switches in series (Pass Tr)

By the connection of Pass Transistors in series will degrade the logic 1 level into inverter 2 so that o/p will not be a proper Logic 0 level..

When Vin1 = 0V (point A), the o/p of 1st inverter is VDD (Pt B). The voltage into inverter 2 at point C is reduced from VDD by voltage of series pass Transistor.

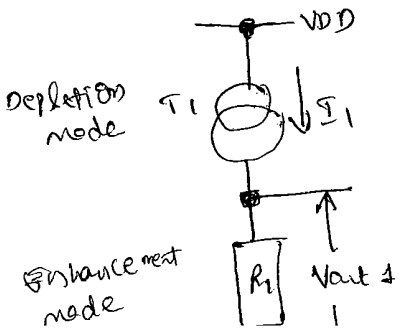
The i/p voltage to inverter 2 $V_{in2} = V_{DD} - V_{tp}$.

V_{tl} → Threshold voltage of a pass Tr.

Consider inverter 1 with i/p VDD. If i/p is at VDD, then p.d Tr is conducting but with a slow voltage across it.

∴ It is in its resistive region (non-saturation) represented by R_1.

meanwhile the p-d Tr is in saturation & is represented by current source.



$I_{ds} = \frac{k w}{L}\left((V_{gs}-V_t)V_{ds} - \frac{V_{ds}^2}{2}\right)$

For P.d Tr$_1$ $(V_{ds} < V_{gs}-V_t)$

$$I_{ds} = \frac{k W_{pd1}}{L_{pd_1}}\left((V_{DD}-V_t)V_{ds1} - \frac{V_{ds1}^2}{2}\right) \quad (V_{in} = V_{DD})$$

(P)

$$\frac{I_{ds}}{V_{ds1}} = \frac{k w_{pd1}}{L_{pd1}}\left((V_{DD}-V_t) - \frac{V_{ds1}}{2}\right)$$

$$R_1 = \frac{V_{ds1}}{I_{ds}} = \frac{L_{pd1}}{k w_{pd1}}\left[\frac{1}{V_{DD}-V_t-\frac{V_{ds1}}{2}}\right] \quad \left(V_{ds} < V_{gs}-V_t \text{ (small)}\right)$$

V_{ds1} is small & $\frac{V_{ds1}}{2}$ we can ignore.

$$R_1 = \frac{1}{k}\cdot Z_{pd1}\left[\frac{1}{V_{DD}-V_t}\right] \quad \left(\because \frac{L_{pd1}}{w_{pd1}} = Z_{pd1}\right) \quad \left(\frac{V_{ds1}}{2} \to \text{ignored.}\right)$$

——— (1)

For depletion mode P.U in saturation with $V_{gs}=0$,

$$I_1 = I_{ds} = k\frac{w_{pu1}}{2L_{pu1}}\left[V_{gs}-V_{td}\right]^2 \qquad \left[I_{ds} = \frac{kw}{L}\frac{(V_{gs}-V_t)^2}{2}\right]$$

But $V_{gs}=0$.

$$I_1 = k\frac{w_{pu1}}{L_{pu1}}\frac{(-V_{td})^2}{2}$$

$$I_1 = k\cdot\frac{1}{Z_{pu1}}\frac{(-V_{td})^2}{2} \quad \text{——— (2)}$$

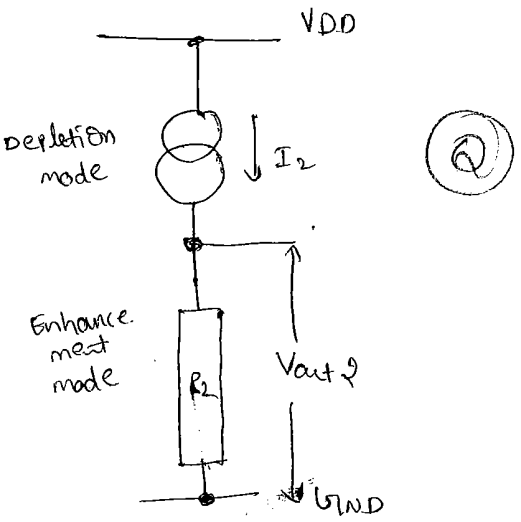
sub (1) & (2) in below eqn

$$V_{out1} = I_1 R_1$$

$$V_{out1} = \frac{k}{Z_{pu1}}\frac{(-V_{td})^2}{2} * \frac{1}{k} Z_{pd1}\left[\frac{1}{V_{DD}-V_t}\right]$$

$$V_{out1} = \frac{Z_{pd1}}{Z_{pu1}}\left(\frac{1}{V_{DD}-V_t}\right)\left(\frac{-V_{td}}{2}\right)^2 \quad \text{——— (3)}$$

Consider inverter 2 :—



Inverter 2 with i/p = $V_{DD} - V_{tp}$

Input $V_{DD} - V_{tp}$.

For p.d Tr, $I_{dy} = \frac{k w_{pd}}{L_{pd}} \left(((V_{DD} - V_{tp}) - V_t) V_{ds2} - \frac{V_{ds}^2}{2} \right)$

$$R_2 = \frac{1}{k} \cdot Z_{pd2} \cdot \frac{1}{((V_{DD} - V_{tp}) - V_t)} \quad \text{—(4)}$$

$$I_2 = k \cdot \frac{1}{Z_{pu2}} \cdot \frac{(-V_{td})^2}{2} \quad \text{—(5)}$$

$$V_{out2} = I_2 R_2$$

$$= k \frac{1}{Z_{pu2}} \frac{(-V_{td})^2}{2} \cdot \frac{1}{k} Z_{pd2} \cdot \frac{1}{V_{DD} - V_{tp} - V_t}$$

$$V_{out2} = \frac{Z_{pd2}}{2 Z_{pu2}} \cdot \frac{(-V_{td})^2}{V_{DD} - V_{tp} - V_t} \quad \text{—(6)}$$

If inverter 2 is to have same o/p voltage under these conditions then $V_{out1} = V_{out2}$.

$$I_1 R_1 = I_2 R_2$$

(3) = (6)

$$\frac{Z_{pd1}}{Z_{pu1}} \frac{(-V_{td})^2}{2} \frac{1}{V_{DD} - V_t} = \frac{Z_{pd2}}{Z_{pu2}} \frac{(-V_{td})^2}{2 (V_{DD} - V_{tp} - V_t)}$$

$$\frac{Z_{pu1}}{Z_{pd1}} (V_{DD} - V_t) = \frac{Z_{pd2}}{Z_{pd2}} (V_{DD} - V_{tp} - V_t)$$

Typical values,

$V_t = 0.2 V_{DD}$

$V_{tp} = 0.3 V_{DD}$

(R)

$$\frac{Z_{PU2}}{Z_{Pd2}} = \frac{Z_{PU1}}{Z_{Pd1}} \cdot \frac{(V_{DD} - V_t)}{(V_{DD} - V_{tp} - V_t)}$$

$$\frac{Z_{PU2}}{Z_{Pd2}} = \frac{Z_{PU1}}{Z_{Pd1}} \cdot \frac{V_{DD} - 0.2V_{DD}}{V_{DD} - 0.3V_{DD} - 0.2V_{DD}}$$

$$= \frac{Z_{PU1}}{Z_{Pd1}} \cdot \frac{0.8V_{DD}}{0.5V_{DD}}$$

$$= \frac{Z_{PU1}}{Z_{Pd1}} \times (1.6)$$

$$\simeq \frac{4}{1} \times 2 \qquad (1.6 \simeq 2).$$

$$\frac{Z_{PU2}}{Z_{Pd2}} \simeq \frac{8}{1}$$

$$\frac{Z_{PU1}}{Z_{Pd1}} = \frac{4}{1}$$

Summarizing for nmos inverter

1) An inverter driven directly from o/p of another should have a Z_{PU}/Z_{Pd} ratio of $\geq \frac{4}{1}$

2) An inverter driven through one or more pass transistors should have $\frac{Z_{PU}}{Z_{Pd}}$ ratio of $\geq \frac{8}{1}$.

Aspects of MOS Tr^s threshold Voltage (V_t):-

(G)

The threshold voltage V_t may be expressed as,

$$V_t = \phi_{ms} \frac{Q_B - Q_{ss}}{C_o} + 2\phi_{fN}$$

Q_B = charge per unit area in depletion layer beneath the oxide.

Q_{ss} = charge density at $Si : SiO_2$ interface.

C_o = capacitance per unit gate area.

ϕ_{ms} = work fn difference b/w gate and Si.

ϕ_{fN} = fermi level potential b/w inverted surface & bulk Si.

FR Polysi gate & Si substrate,
ϕ_{ms} is -ve. but negligible.

the magnitude, sign of V_t determined by negative term $-\frac{Q_{ss}}{C_o}$ & remaining +ve terms.

To evaluate V_t, each term is determined as follows:

$$Q_B = \sqrt{2\epsilon_0 \epsilon_{si} q N (2\phi_{fN} + V_{SB})} \text{ Coulomb/m}^2.$$

$$\phi_{fN} = \frac{KT}{q} \ln \frac{N}{n_i} \text{ volts.}$$

$$Q_{ss} = (1.5 \text{ to } 8) \times 10^{-8} \text{ Coulomb/m}^2.$$

where V_{SB} = substrate bias voltage
(-ve w.r.t.u source fr nmos
+ve " " pmos)

$q = 1.6 \times 10^{-19}$ Coulomb.

$\epsilon_{ins} = 6\gamma = 4$ fr SiO_2

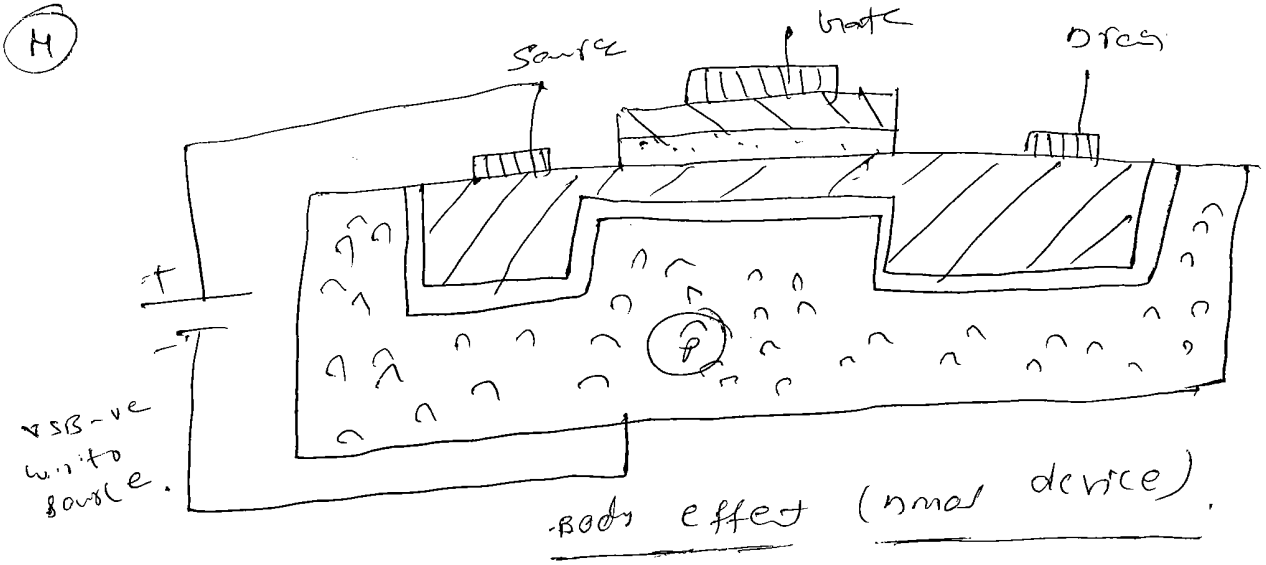
N = impurity concentration in substrate (N_A & N_D)

ϵ_{si} = relative permittivity of Si

n_i = intrinsic concentration ($1.6 \times 10^{10}/cm^3$ at 300°K)

k = Boltzmann's constant = 1.4×10^{-23} joule/°K.

(H)



Body effect (nmos device).

Body effect may also be taken into account since substrate may be biased w.r.t to source.

change in V_t : $\Delta V_t \cong \gamma(\sqrt{V_{SB}})$

γ is constant depends on substrate doping.

So, that more lightly doped the substrate, smaller will be body effect

we may write,

$$V_t = V_t(0) + \left[\frac{D}{\epsilon_{ins} t_o}\right)\sqrt{2\epsilon_o \epsilon_{Si} Q_N} \cdot \sqrt{V_{SB}}$$

$V_t(0)$ → Threshold voltage for $V_{SB} = 0$

For nmos enhancement mode type

$V_{SB} = 0V$, $V_t = 0.2\, V_{DD}$ (1V for $V_{DD} = 5V$)

$5 \times 0.2 = 5 \times \frac{2}{10} = 1V$

$V_{SB} = 5V$, $V_t = 0.3\, V_{DD}$ [1.5V for $V_{DD} = 5V$)

For PMOS negative values.

nmos depletion mode :-

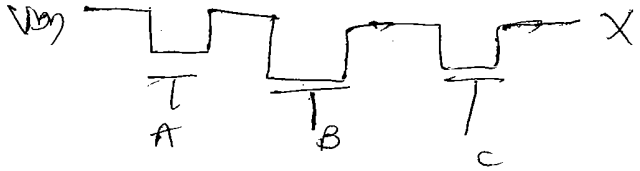
$V_{SB} = 0V$, $V_t = -0.3 V_{DD}$ (-3.5 V for $V_{DD} = 5V$)

Pass Tr :-

Unlike bipolar Tr's, the isolated nature of the gate allows MOS Tr's to be used as switches in series with lines carrying logic levels. (1)

This application of MOS device is called as Pass Tr and switching logic arrays can be formed.

EX: AND array



$X = A.B.C$ (Logic 1 = $V_{DD} - V_t$).

$\overline{X} = ?$ $\qquad \overline{X} = \overline{ABC}$

$= \overline{A} + \overline{B} + \overline{C}$

$=$

Assumes gnd potential when $A+B+C=0$.

fig:- Pass Tr AND gate

Mos ↑r figure of merit (ω_0):—

An indication of freq response may be obtained from the parameter ω_0.

$$\frac{1}{\text{Time}} \propto g_m = \omega_0 = \frac{g_m}{C_g} = \frac{\mu}{L^2}(V_{gs} - V_t) = \frac{1}{\tau_{sd}}.$$

$\frac{1}{\text{Time}} \propto g_m$

less time → high speed.

$$\begin{cases} \tau_{sd} = \dfrac{L^2}{\mu V_d} \\ \tau_{sd} = \dfrac{L^2}{\mu(V_{gs}-V_t)} \\ \dfrac{1}{\tau_{sd}} = \dfrac{\mu(V_{gs}-V_t)}{L^2}. \end{cases}$$

(J) switching speed depends on gate voltage (V_{gs}) above threshold and on carrier mobility (μ) & inverse of square of channel length ($\frac{1}{L^2}$)

For ckt required that g_m be as high as possible.

→ e mobility ratio $\simeq$ 3:1p.

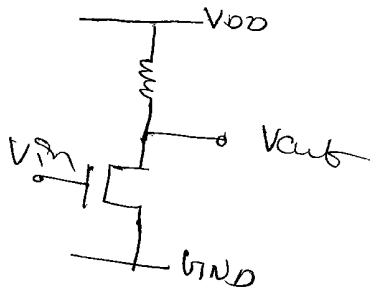
Surface mobility is also dependent on effective gate voltage $V_{gs} - V_t$.

The Basic Inverter ckt

The Basic Inverter ckt requires a Tr with source connected to gnd and a load resistor of some sort connected from drain to the positive supply VDD. The o/p is taken from drain and the i/p is applied b/w gate and gnd.

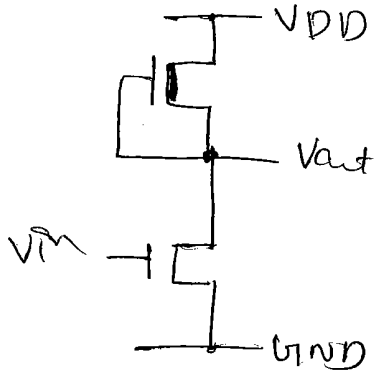
(K)

Resistors are not conveniently produced on Si substrate. Even modest values occupy excessively large areas so that some other form of load resistance is required.



Basic inverter.

Convenient way to solve this problem is to use a a depletion mode Tr as load.



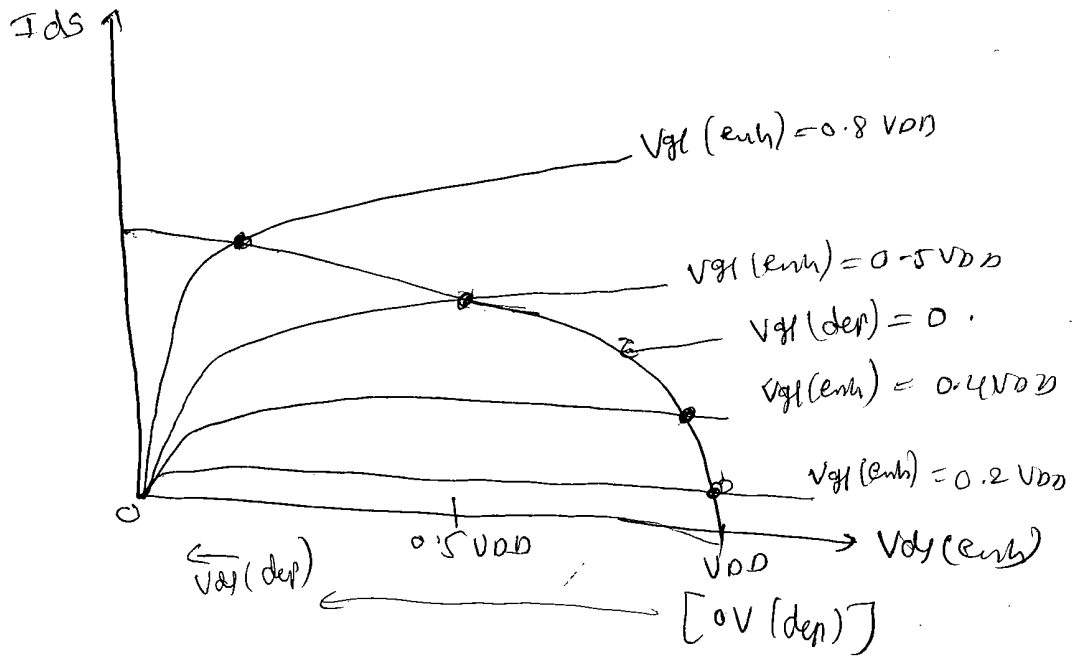
(1) With no current drawn from o/p, the current Id for both Trs must be equal.

(2) For depletion mode Tr, the gate is connected to source so it is always on.

(3) depletion mode Tr is called pull up (PU) & enhancement mode Tr ↳ pull down (PD)

(4) To obtain inverse transfer ch's we superimpose the Vgs = 0, depletion mode ch curve on the family of curves for enhancement mode device, noting that max. voltage

across the ...



(L)

$V_{ds(enh)} = V_{DD} - V_{ds(dep)}$

$= V_{out}$.

$V_{gs(enh)} = V_{in}$

→ V_{in} ($= V_{gs}$ P.d Tr) exceeds the P.d threshold voltage current begins to flow. $(V_{gs} \geq V_t)$

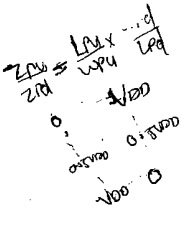
The o/p voltage ↓ decrease (thy) and subsequent increase in V_{in} will cause P.d Tr to come out of saturation and become resistive. $(V_{ds} < V_{gs} - V_t)$

i/p volt ↑ → o/p V ↓

Slope of Transfer ch's determines gain.

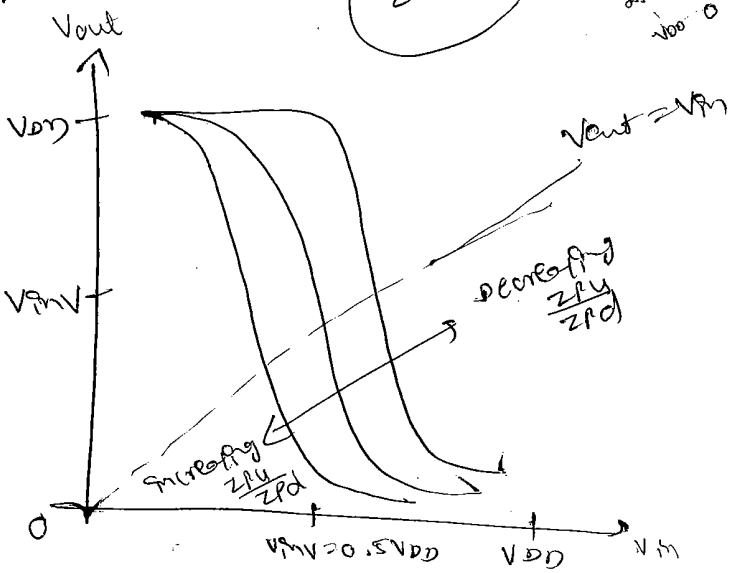
$$\text{Gain} = \frac{\delta V_{out}}{\delta V_{in}}.$$

$Z = \frac{L}{W}$



→ The point at which $V_{out} = V_{in}$ is denoted as V_{inv} and it will noted that Transfer ch's and V_{inv} can be shifted by variation of ratio of Pull-up to pull down resistance. $\left(\frac{Z_{pu}}{Z_{pd}}\right)$

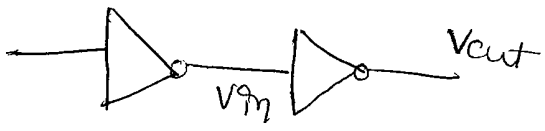
Z — ⊕ L ratio.



Determination of Pull up to Pull down ratio (Z_{pu}/Z_{pd}) For an nmos inverter driven by another nmos inverter?

(M)

→ an inverter is driven from the o/p of another similar inverter.



→ Consider the depletion mode TrT for which $V_{gs} = 0$ under all conditions,

→ Assume that in order to cascade inverters without degradation of levels we are aiming to meet the requirement

$$V_{in} = V_{out} = V_{inv}$$

⇒ we set $V_{inv} = 0.5 V_{DD}$. At this pt both TrTs are in saturation. $(V_{ds} > V_{gs} - V_t)$

$$I_{ds} = \frac{k_w}{L} \frac{(V_{gs} - V_t)^2}{2} \qquad \left[\left(I_{ds} = \frac{\beta}{2} V_{ds}^2 \right) \right]$$

In depletion mode $V_{gs} = 0$.

$$I_{ds} = k \cdot \frac{W_{pu}}{L_{pu}} \frac{(-V_{td})^2}{2} \quad - (1)$$

For Enhancement mode (Pull down TrT)

$$I_{ds} = k \cdot \frac{W_{pd}}{L_{pd}} \frac{(V_{inv} - V_t)^2}{2} \quad - (2) \quad (V_{gs} = V_{inv})$$

Both currents are same.

$$\therefore \quad (1) = (2)$$

$$\frac{k W_{pu}}{L_{pu}} (-V_{td})^2 = k \cdot \frac{W_{pd}}{L_{pd}} \frac{(V_{inv} - V_t)^2}{2}$$