VLSI DESIGN

UNIT-I

Introduction to IC Technology:

Electronics as we know it today is characterized by reliability, low power dissipation, extremely low weight and volume & low cost, coupled with an ability to cope easily with a high degree of sophistication and complexity. Electronics & in particular the Integrated circuit, has made possible the design of powerful and flexible processors which provide highly intelligent and adaptable devices for the user. IC memories have provided the essential element to complement these processors & together with a wide range of logic & analog Integrated circuitry, they have provided the system designer with components of considerable capability & extensive application.

The invention of Transistor by William B. Shockley, Walter H. Brattain & John Bardeen of Bell Telephone Laboratories was followed by the development of the IC.

The very first IC emerged at the beginning of 1960 and since that time there have already been 4 generations of IC's:

1) SSI (small scale Integration) (10-100)
2) MSI (mediam scale Integration) (100-1000)
3) LSI (Large scale Integration) (1K - 20K)
4) VLSI (Very

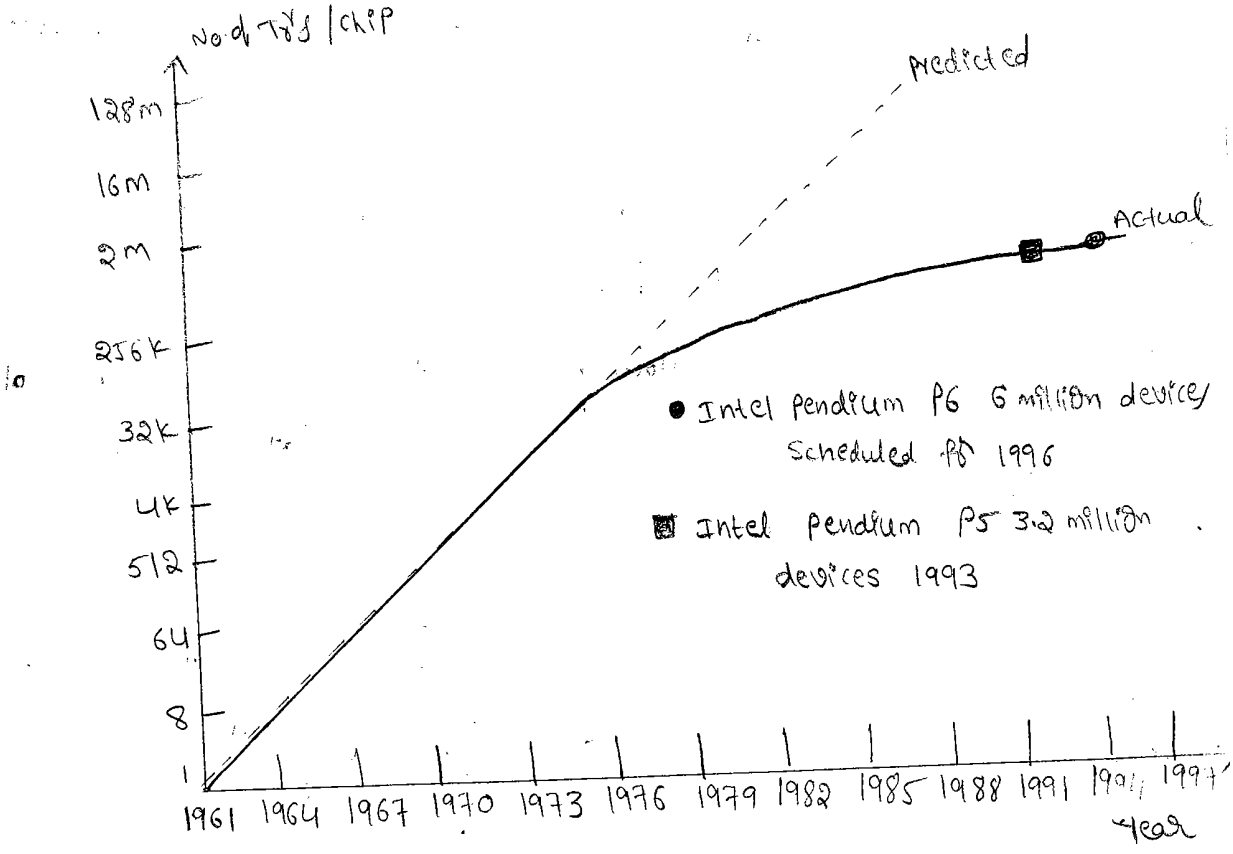
⇒ Upcoming 5th generation, ULSI (Ultra Large scale Integrati which is characterized by complexities in excess of 3 million devices on a single IC chip.

The IC Era :—

Such has been the Potential of silicon Integrated circuit that has been an extremely rapid growth in the number of transistors being Integrated into circuits on a single silicon chip.

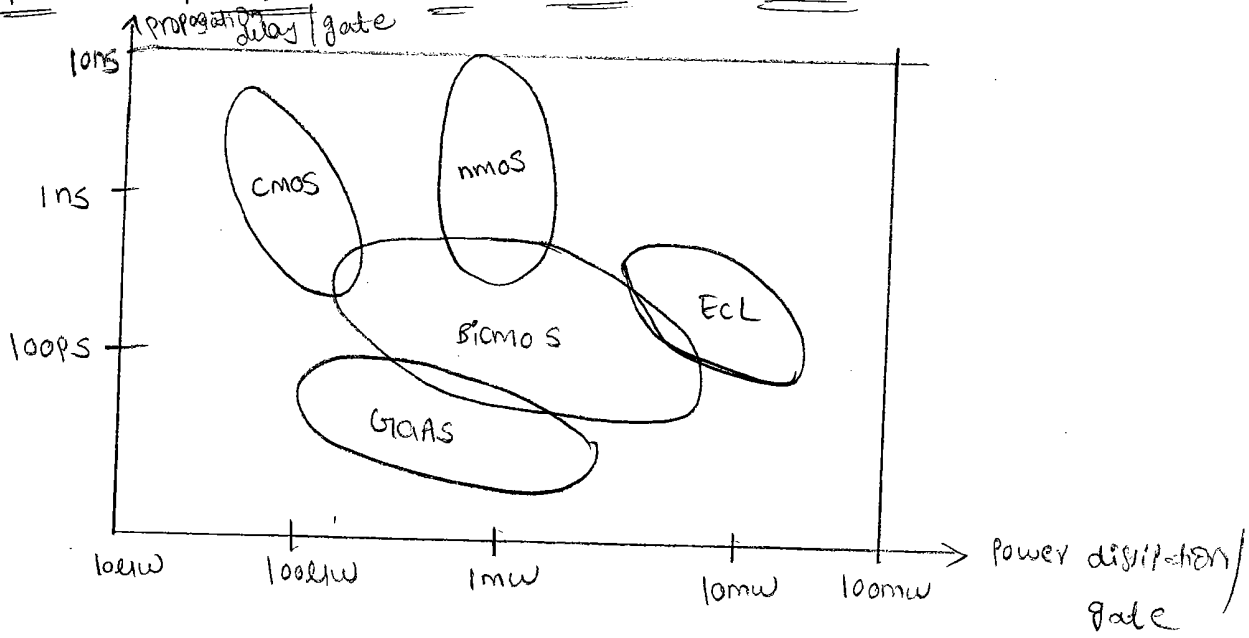
In lessthan 3 decades, this number has risen from tens to millions.

This increase in number of Transistors per chip getting double for every 2 years is known as "moore's first Law". made by Gordon moore (of Intel) in the 1960's.



... predictions and actual over the last few years due to problems associated with the complexities involved in designing and testing such very Large circuits.

Speed / Power performance of available Technologies :-



over the past several years, silicon cmos technology has become the dominant fabrication process for relatively high performance & cost effective VLSI circuits.

→ The increase in no. of Trs/chip is highlighted by recent products such as RISC chips in which it is possible to process some 35 million instructions per second.

→ In order to improve on this throughput rate it will be necessary to improve the technology, both in terms of scaling and processing, & through the incorporation of other enhancements such as BiCMOS.

→ In particular. The emerging Gallium Arsenide (GaAs) based technology will be most significant for ultra high speed logic / fast digital processors.

→ GaAs also has further potential as a result of its photo-electronic properties both as a Rx'er and as a Tx'er of light.

micro electronics evolution:

Year	1947	1950	1961	1966	1971	1980	1990	2000
Technology	Invention of Transistor	discrete components	SSI	MSI	LSI	VLSI	ULSI*	GISI
Approximate number of Transistors per chip in Commercial Products	1	1	10	100 – 1000	1000 – 20,000	20,000 – 1,000,000 (10 Lakh)	1,000,000 (1c lakh) – 10,000,000 (1 crore)	> 1 crore 10,000,000
Typical Products	–	Junction Transistor & diode	Planar devices, logic gate FF	counters, mux, Adders	8-bit µP, Rom, RAM	16 & 32 bit µP, Sophisticated peripherals 64bit dram	special processors, Virtual reality machines, smart sensors	

GSI - Giant-scale Integration

Metal-oxide-semiconductor (MOS) and related VLSI Technology:-

Within the bounds of MOS Technology, the possible circuit realizations may be based on PMOS, NMOS, CMOS & BiCMOS devices. GaAs Technology is also one of the leading IC Technology.

Although CMOS is the dominant technology, some of the examples used to illustrate the design processes will be presented in NMOS form. The reasons for this are

(1) For NMOS Technology, the design methodology and the design rules are easily learned, thus providing a simple but excellent introduction to structured design for VLSI.

(2) NMOS technology and design processes provide an excellent background for other technologies. In particular some familiarity with NMOS allows a relatively easy transition to CMOS Technology and design.

(3) For GaAs Technology some arrangements in relation to logic design are similar to those employed in NMOS Technology.

Not only in VLSI Technology, providing the user with a new and more complex range of "off the shelf" circuits, but VLSI processes are such that system designers can readily design their own special circuits of considerable

→ This provides a new degree of freedom for designers and it is probable that some very significant advances will result.

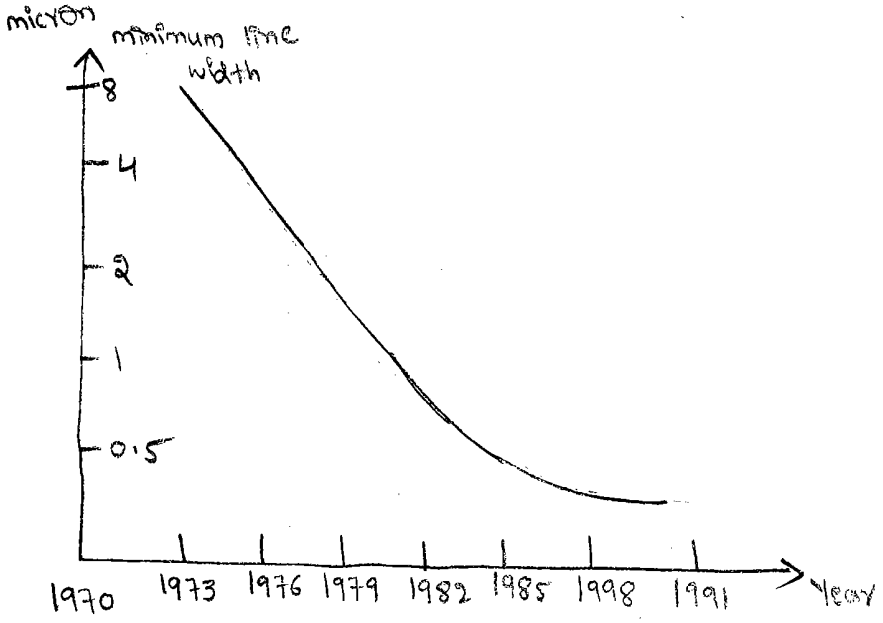


Fig. approximate minimum line width of commercial products Vs year

→ Couple this with the fact that integration density is increasing rapidly, as advances in technology shrink the feature size for circuits integrated in silicon.

The effectiveness of the circuits produced has increased with scaling down as shown in fig.

→ A common measure of effectiveness is the speed power product of the basic logic gate circuit of the technology (for nmos, the nor gate; with nand and nor gates for cmos).

→ speed power product is measured in picojouley (PJ) and

is the product of the gate switching delay in nanoseconds and the gate power dissipation in milliwatts.

Basic Mos transistors:-

nmos enhancement and depletion mode transistors:-

→ nmos devices are formed in a P-type substrate of moderate doping level.

→ The source and drain regions are formed by diffusing n-type impurities through suitable masks into these areas to give the desired n- impurity concentration and give rise to depletion regions which extend mainly in the more lightly doped p- region.

→ Thus source and drain are isolated from one another by 2 diodes.

→ connections to the source and drain are made by a deposited metal layer.

→ In order to make a useful device, there must be the capability to establishing and controlling a current b/w source and drain.

→ This is achieved in one of 2 ways, giving rise to the enhancement mode and depletion mode Transistors.

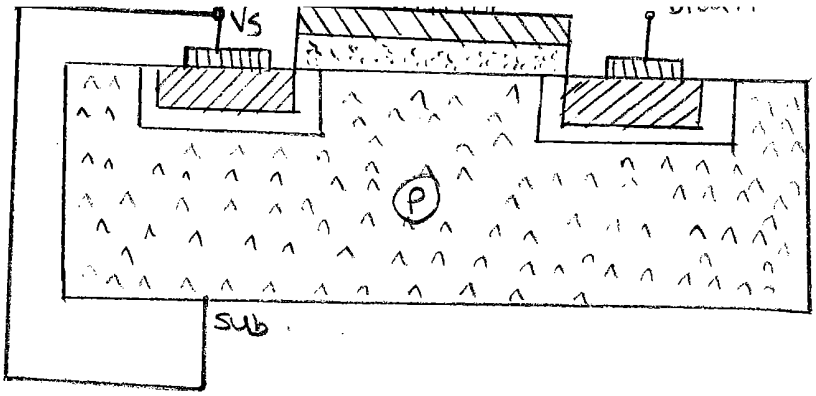


fig : nmos enhancement mode transistor.

In the enhancement mode, A polysilicon gate is deposited on a layer of insulation over the region b/w source and drain.

→ In enhancement mode device the channel is not established and the device is in a non-conducting condition, $V_D = V_S = V_{GS} = 0$.

→ If the gate is connected to a suitable positive voltage with respect to source, then the electric field established b/w the gate and substrate give rise to a charge inversion region in the substrate under the gate insulation and a conducting path of channel is formed b/w source and drain.

→

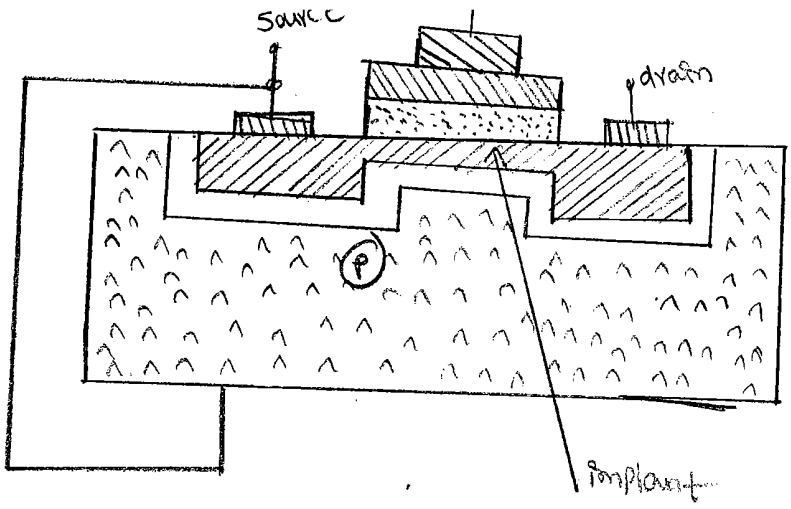
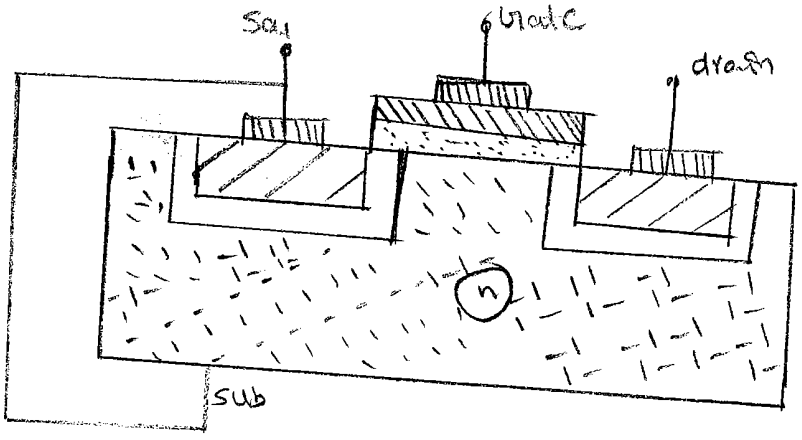


fig : nmos depletion mode transistor

In depletion mode, the channel may also be established so that it is present under the condition $V_{GS} = 0$ by implanting suitable impurities in the region b/w source and drain during manufacture and prior to depositing the insulation and the gate. Under these circumstances, source and drain are connected by a conducting channel, but the channel may now be closed by applying a suitable negative voltage to the gate.

In both cases, variations of the gate voltage allow control of any current flow b/w source and drain.



In Pmos enhancement mode Transistor, the substrate is of n-type material and the source and drain diffusions are p-type. By the application of a negative voltage of suitable magnitude ($>|V_t|$) b/w gate and source will rise to the formation of a channel (p-type) b/w source and drain and current may then flow if the drain is made negative with respect to the source.

→ In this case, the current is carried by holes as opposed to es.

→ The Pmos transistors are inherently slower than nmos, since $\mu_n = 2.5\mu_p$.

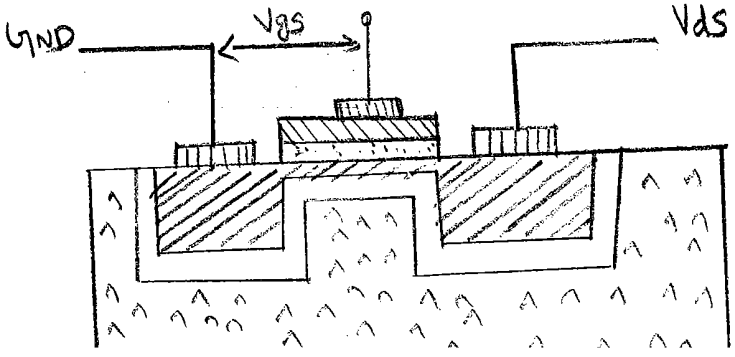
$\mu_n = 650\ cm^2/Vsec$

$\mu_p = 240\ cm^2/Vsec$.

Enhancement mode Transistor Action:

To understand the mechanism of Enhancement mode we have to consider 3 conditions.

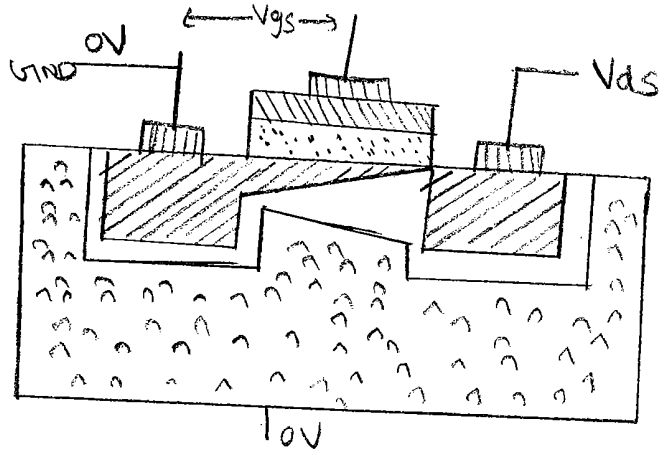
Threshold voltage (V_t):- The minimum voltage applied b/w gate and source to establish channel.



$V_{gs} > V_t$

$V_{ds} = 0V$

Fig. indicates the conditions prevailing with the channel established but no current flowing b/w source and drain ($V_{ds} = 0$).



$V_{gs} > V_t$

$V_{ds} < V_{gs} - V_t$

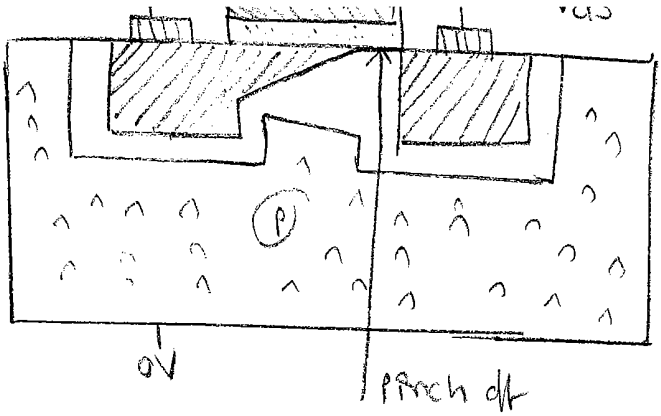
→ Now consider the conditions prevailing when current flows in the channel by applying a voltage V_{ds} b/w drain and source.

→ Along the channel, a corresponding IR drop = V_{ds} will be there.

→ This results in the voltage b/w gate and channel varying with distance along the channel with the voltage being a maximum of V_{gs} at the source end.

→ Since the effective gate voltage is $V_g = V_{gs} - V_t$ (no current flows when $V_{gs} < V_t$), there will be voltage avaiable to invert the channel at the drain end so long as $V_{gs} - V_t \geq V_{ds}$.

→ The limiting condition comes when $V_{ds} = V_{gs} - V_t$. For all voltages $V_{ds} < V_{gs} - V_t$, the device is in the non-saturation region of operation which is $\boxed{V_{ds} < V_{gs} - V_t}$.



$V_{gs} \geq V_t$

$V_{ds} \geq V_{gs} - V_t$

If V_{ds} is increased to a level greater than $V_{gs} - V_t$. In this case, an IR drop = $V_{gs} - V_t$ takes place over less than the whole length of the channel so that over part of the channel, near the drain, there is insufficient electric field available to give rise to an inversion layer to create the channel. The channel is therefore "pinch-off".

→ Diffusion current completes the path from source to drain in this case, causing the channel to exhibit a high resistance and behave as a constant current source.

→ This region is known as saturation, is characterized by almost constant current for increase of V_{ds} above $V_{ds} = V_{gs} - V_t$.

→ In all the cases the channel will cease to exist and no current will flow when $V_{gs} < V_t$.

→ The typical values for enhancement mode devices

$V_t = 1V$ for $V_{DD} = 5V$

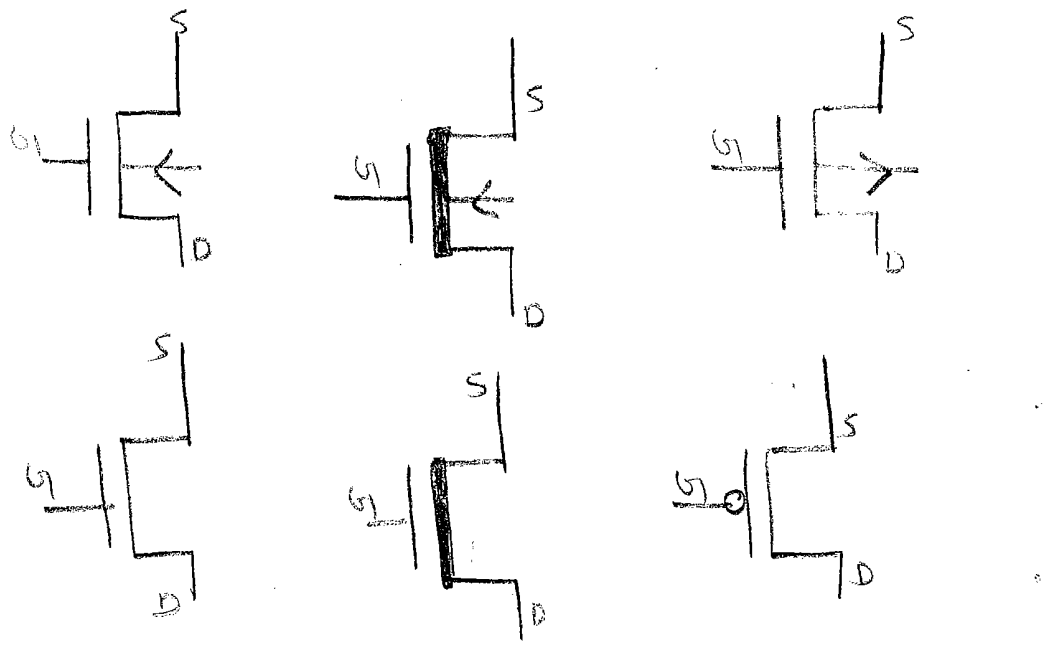
& In general $V_t = 0.2 V_{DD}$.

Depletion mode transistor Action:-

For depletion mode device the channel is established because of the implant, even when $V_{GS} = 0$ and to cause the channel to cease to exist a negative voltage V_{td} must be applied b/w gate and source.

V_{td} is typically $< -0.8 V_{DD}$, depending on implant and substrate bias, but threshold voltage difference aside the action is similar to that of enhancement mode T&R.

Symbols for nmos & pmos transistors:



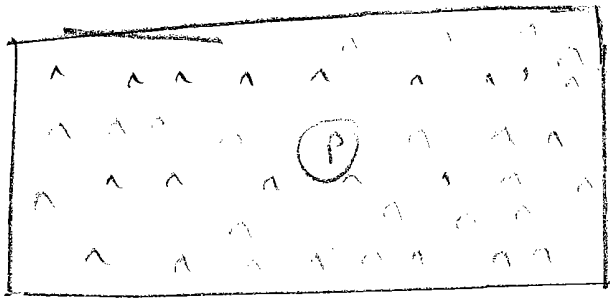
nmos enhancement

nmos depletion

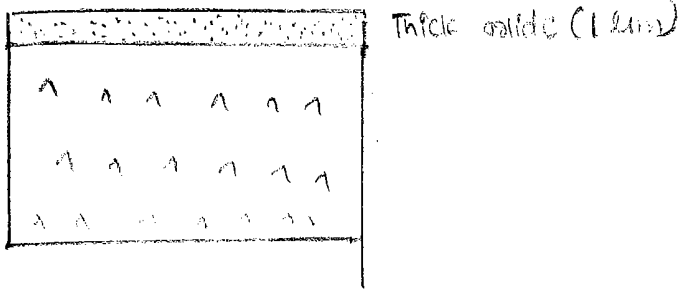
pmos enhancement

nmos fabrication:—

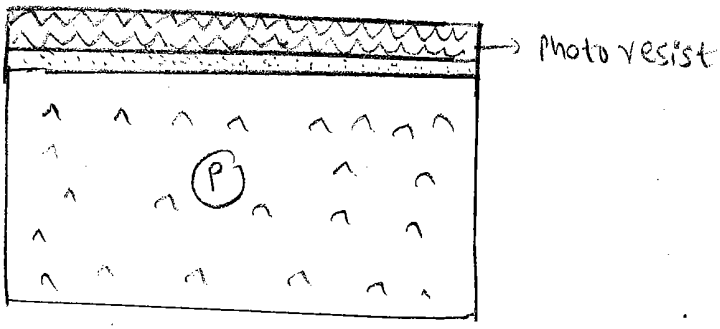
① Processing is carried out on a thin wafer cut from a single crystal of silicon of high purity into which the required P-impurities are introduced as the crystal is grown. Such wafers are typically 75 to 150mm in diameter and 0.4mm thick and are doped with, say boron to impurity concentration of $10^{15}/cm^3$ to $10^{16}/cm^3$, giving resistivity in the approximate range 25 ohm cm to 2 ohm cm.



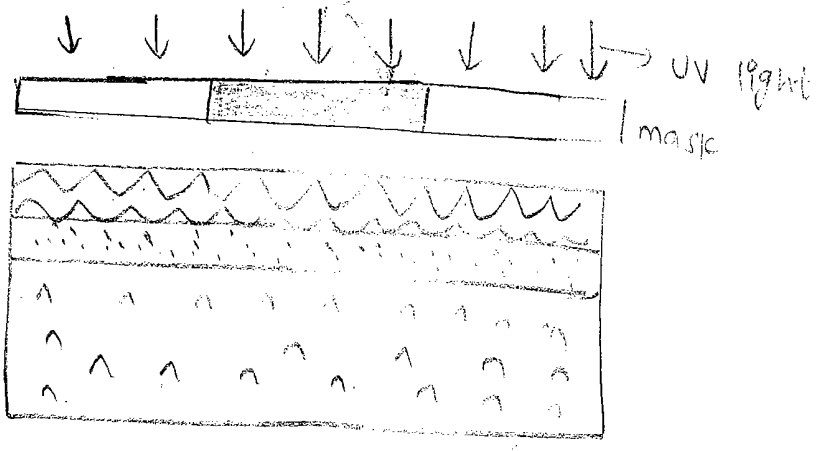
② A layer of silicon dioxide (SiO_2), typically 1 µm thick is grown all over the surface of the wafer to protect the surface, act as a barrier to dopants during processing and provide a generally insulating substrate onto which other layers may be deposited and patterned.



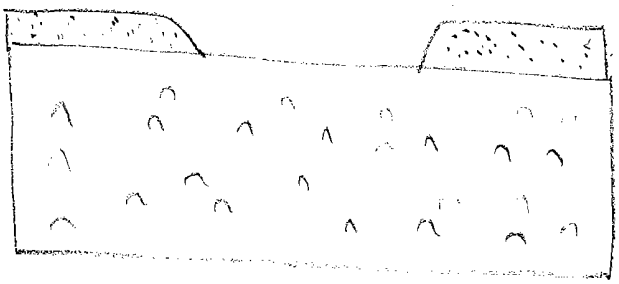
③ The surface is now covered with a photoresist which is deposited onto the wafer and spun to achieve an even



(4) The photoresist layer is then exposed to ultraviolet light through a mask which defines those regions into which diffusion is to take place together with transistor channels. For Example, that those areas exposed to ultraviolet radiation are polymerized (hardened), but that the areas required for diffusion are shielded by the mask and remain unaffected.

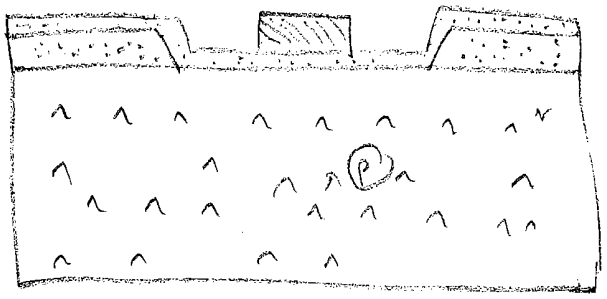


(5) These areas are subsequently readily etched away together with the underlying silicon dioxide so that the wafer surface is exposed in the window defined by the mask.



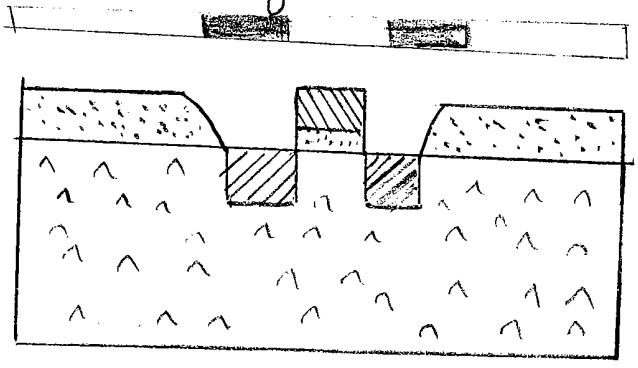
(6) The remaining photoresist is removed and a thin layer of SiO_2

is grown over the entire chip surface and then Polysi is deposited on top of this to form the gate structure. The polysi layer consists of heavily doped polysi, deposited by "Chemical Vapor Deposition (CVD)". In the fabrication of fine pattern devices, precise control of thickness, impurity concentration & resistivity is necessary.

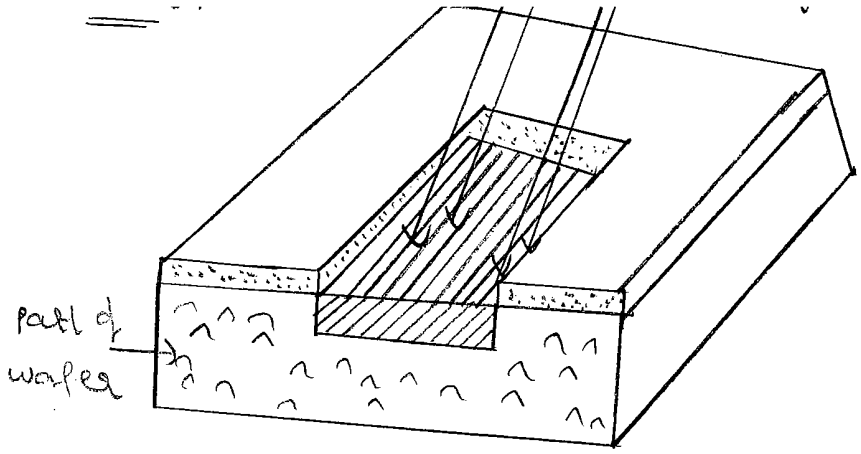


Patterned poly (1-2 μm) on thin oxide (800-1000 Å)

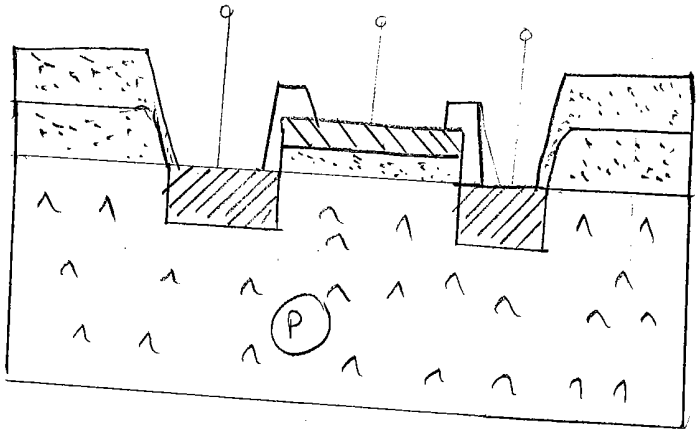
(7) Further photoresist coating and masking allows the polysilicon to be patterned, and then the thin oxide is removed to expose areas into which n-type impurities are to be diffused to form the source and drain. Diffusion is achieved by heating the wafer to a high temperature and passing a gas containing the desired n-type impurity (for example, phosphorus) over the surface. Note that the polysilicon with underlying thin oxide and the thick oxide act as masks during diffusion— the process is self-aligning.



n^+ diffusion (1 μm deep)

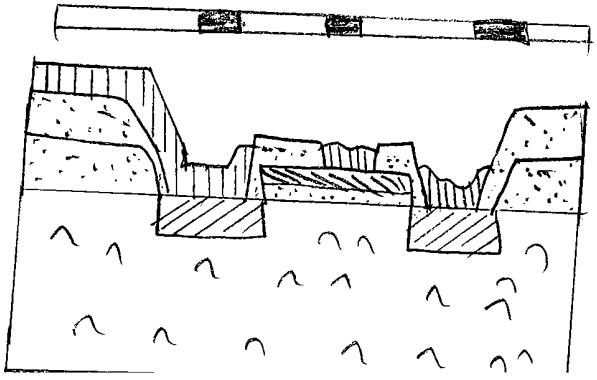


(8) Thick oxide (SiO_2) is grown over all again and is then masked with photoresist and etched to expose selected areas of the polysilicon gate and the drain and source area where connections (ie contact cuts) are to be made.

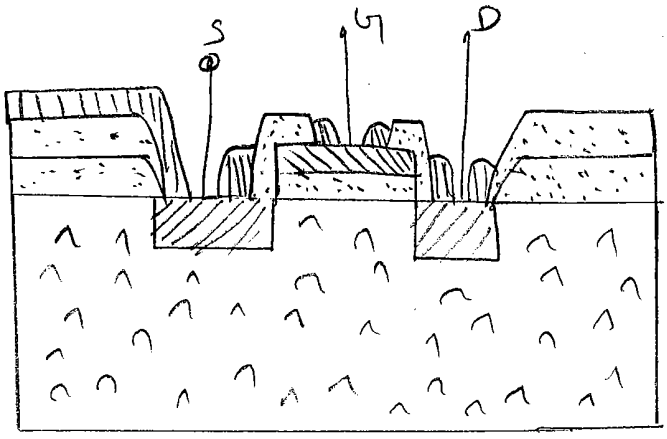


contact holes (cuts)

(9) The whole chip then has metal (aluminum) deposited over its surface to a thickness typically of 1 μm. This metal layer is then masked and etched to form the required interconnection pattern.



Patterned metallization (aluminum 1 μm)



The process revolves around the formation & deposition and patterning of 3 layers, seperated by silicon dioxide insulation. The layers are diffusion within the substrate, Polysilicon on oxide on the substrate & metal insulated again by oxide.

→ To form depletion mode devices it is only necessary to introduce a masked ion implantation step after forming window in oxide (b/w steps and 6). Again the thick oxide acts as a mask and this process stage is also "self-aligning".

→ Some extra process steps are necessary, including the overglassing of the whole wafer, except where contacts to the outside world are required.

Fabrication:-

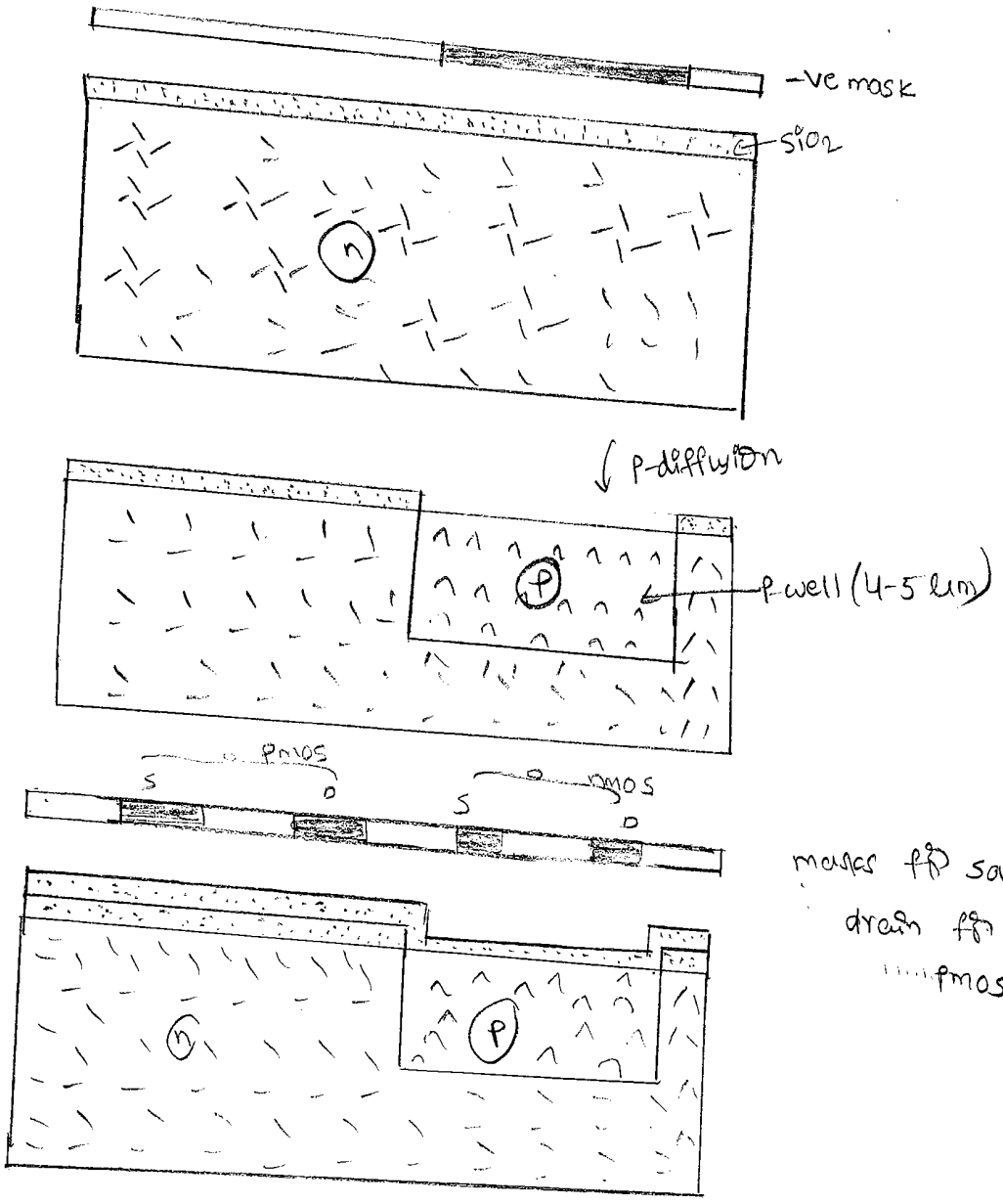
There are number of approaches to cmos fabrication. They are

1. P-well process
2. n-well process
3. Twin tub process
4. Silicon-On-Insulator (SOI) process.

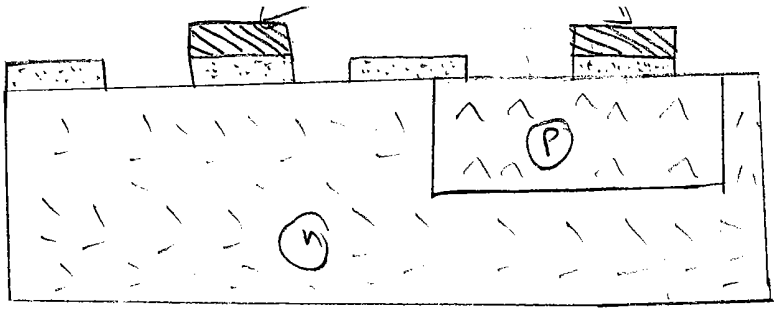
→ we will concentrate on well-bayed circuits. The P-well process is widely used in practice and the n-well process is also popular, particularly as it was an easy retrofit to existing nmos lines.

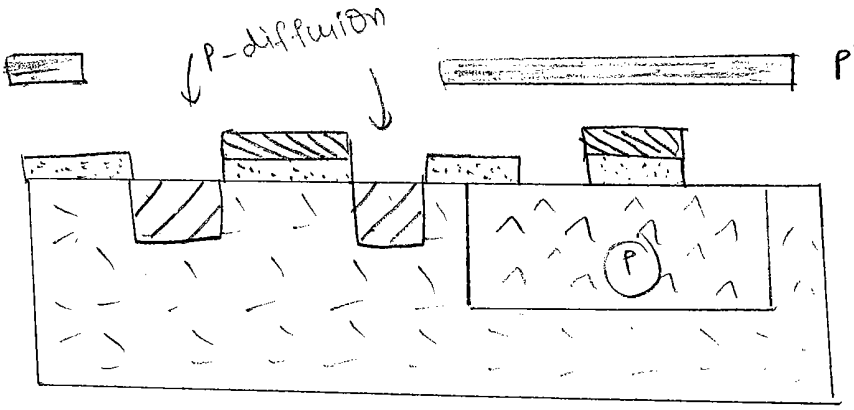
P-well Process:

(1)



masks for source and drain for both nmos & pmos





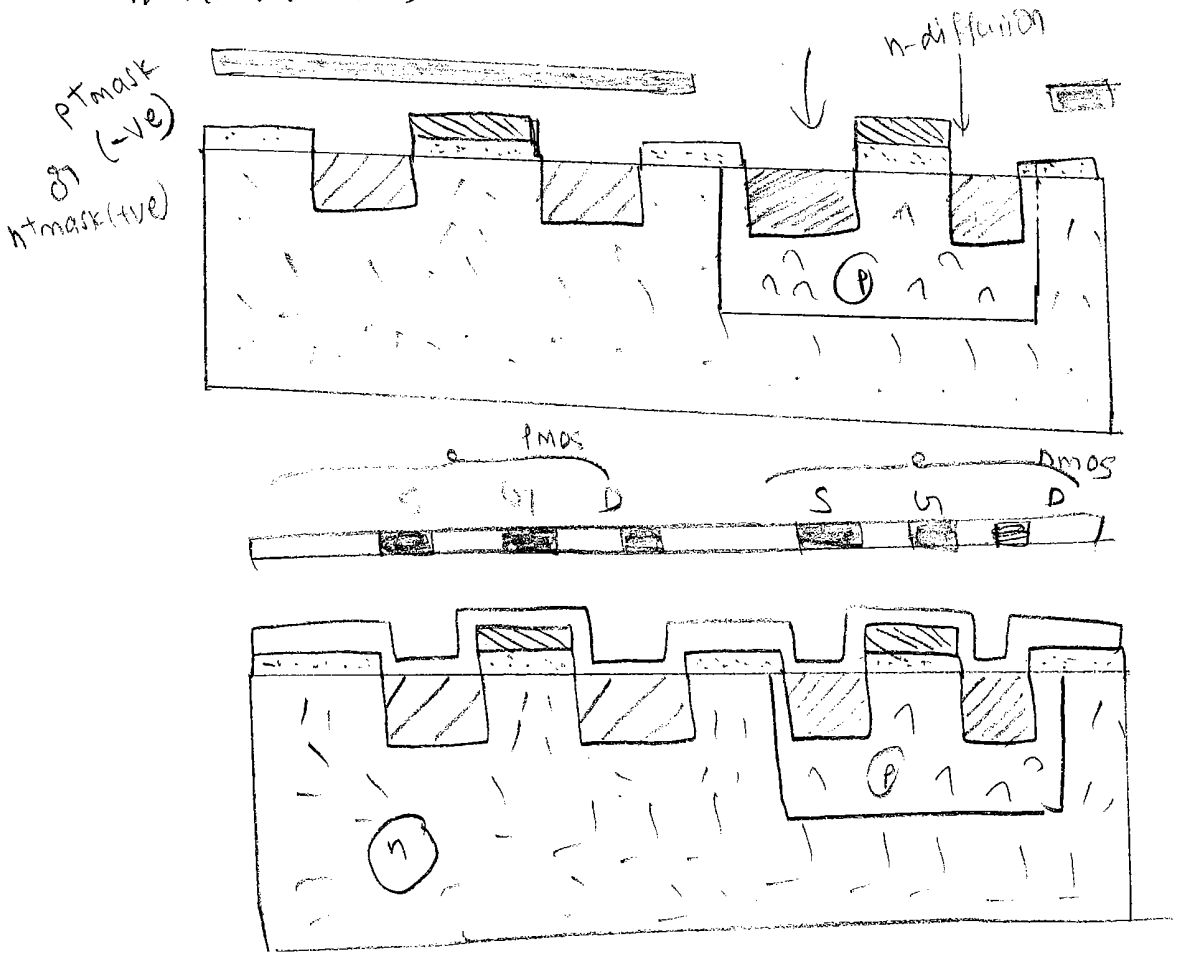
p⁺mask (+ve)
(or) n⁺mask (-ve)

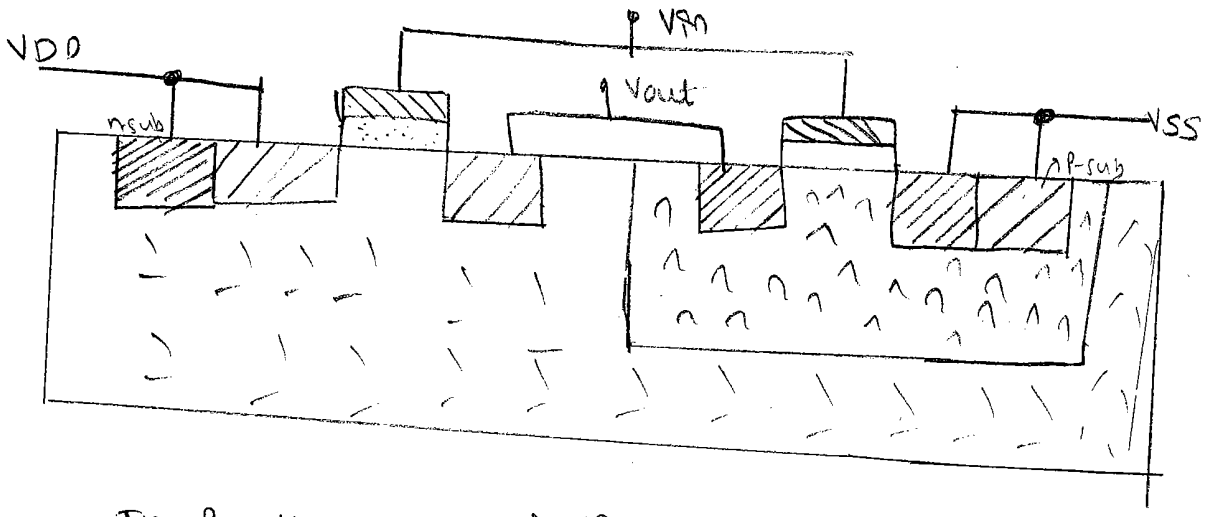
p⁺mask (+ve) ⇒ masked area not effected for p-diffusion.

p⁺mask (-ve) ⇒ masked area not effected for n-diffusion.

n⁺mask (+ve) ⇒ masked area not effected for n-diffusion.

n⁺mask (-ve) ⇒ " " not effected for p-diffusion.





In P-well cmos fabrication, structure consists of an n-type substrate in which P-device may be formed by suitable masking and diffusion and in order to accommodate n-type device a deep P-well is diffused into the n-type substrate.

→ The diffusion must be carried out with special care since the P-well doping concentration & depth will affect the threshold voltages as well as the breakdown voltage of n-Transistors.

→ To achieve low threshold voltage (0.6 to 1V), we need either deep well diffusion or high well resistivity.

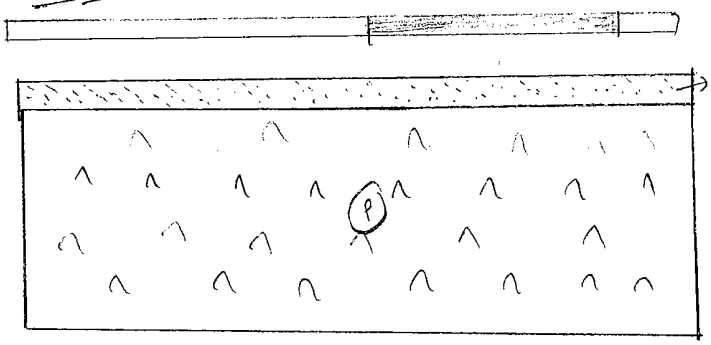
→ However deep wells require larger spacing b/w n- and P-type transistors and wires because of lateral diffusion & therefore a larger chip area.

CMOS n-well Process :-

n-well CMOS circuits are also superior to P-well because of the lower substrate bias effects on transistor threshold voltage and inherently lower parasitic capacitances associated with source and drain regions.

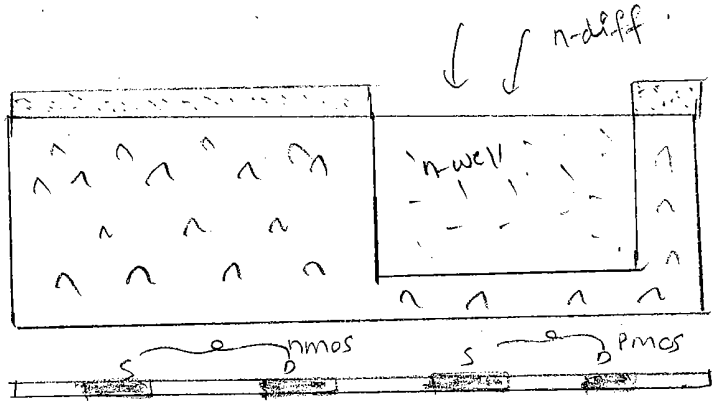
Fabrication steps in Typical n-well process :-

(1)



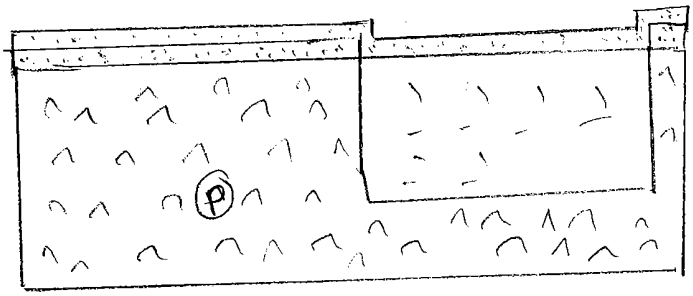
→ Wafer
→ doping with P-sub,
→ deposite oxide layer.

(2)



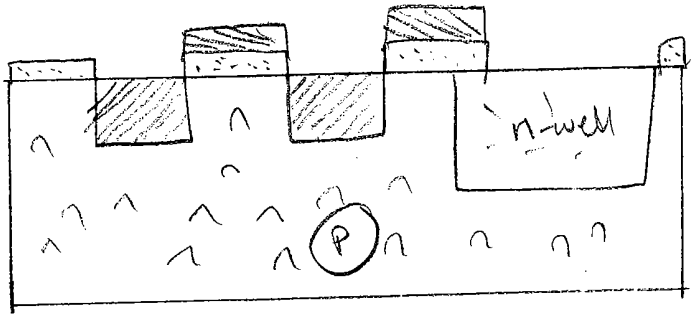
→ etching.
→ n-diffusion for well.

(3)

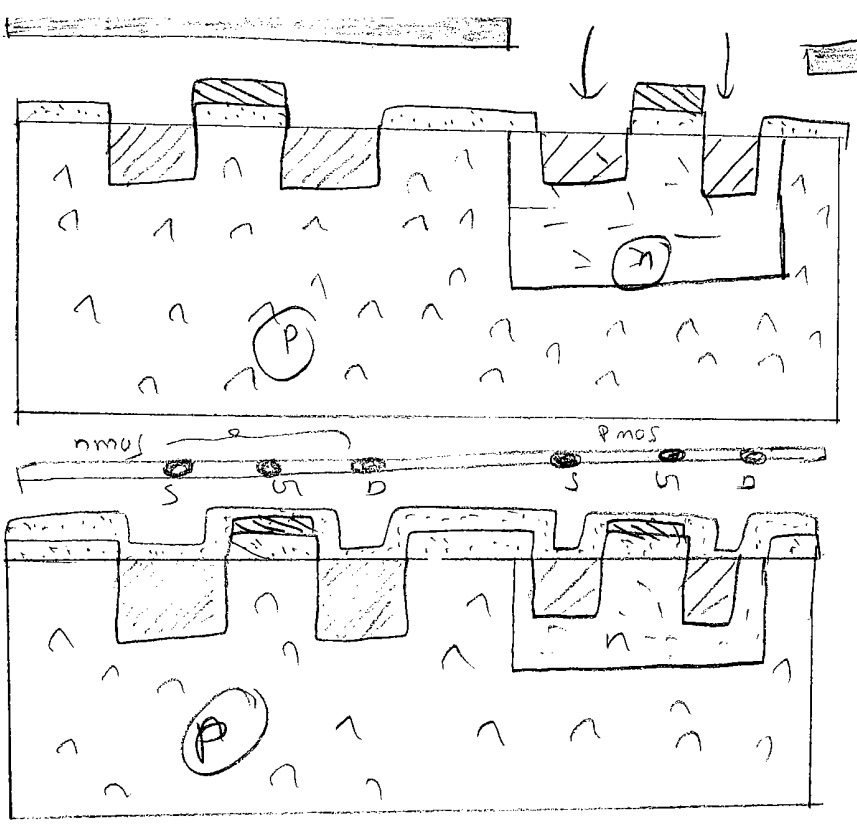


→ again deposit oxide
→ mask area for source & drain for both TYs.

(4)



→ etching area for S & D for both TYs.
→ form gate by depositing polysilicon
→ For S & D of nmos by using



→ form S & D for P-mos.

→ deposit SiO_2

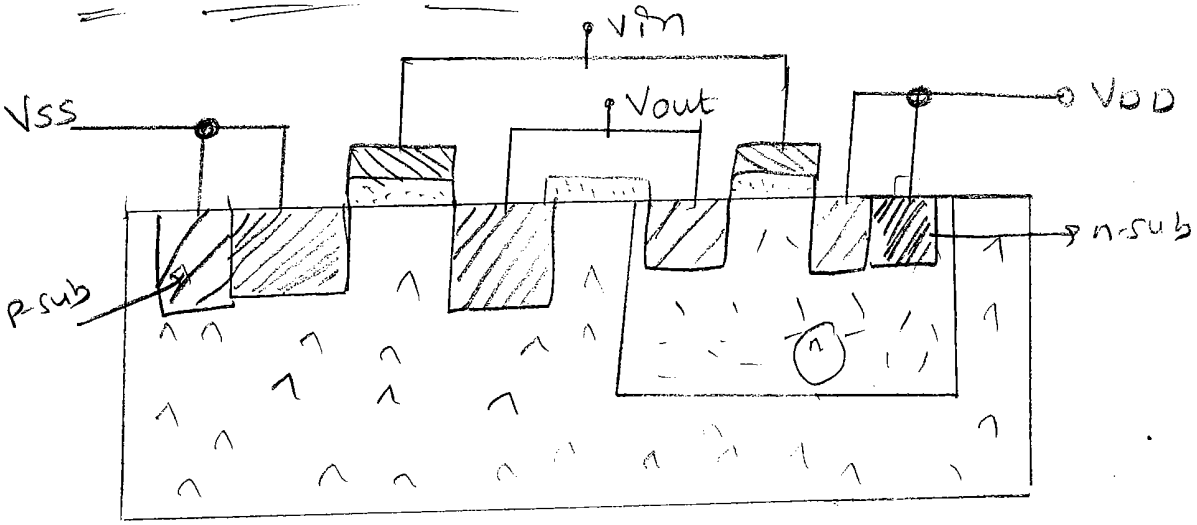
→ mark areas for S, G, D for both Tr's.

→ Then etch the marked areas & take contact cuts.

→ Finally deposit metal layer & then etch areas for contact cuts.

→ overall glass with cuts for bonding pads.

CMOS n-well inverter :-



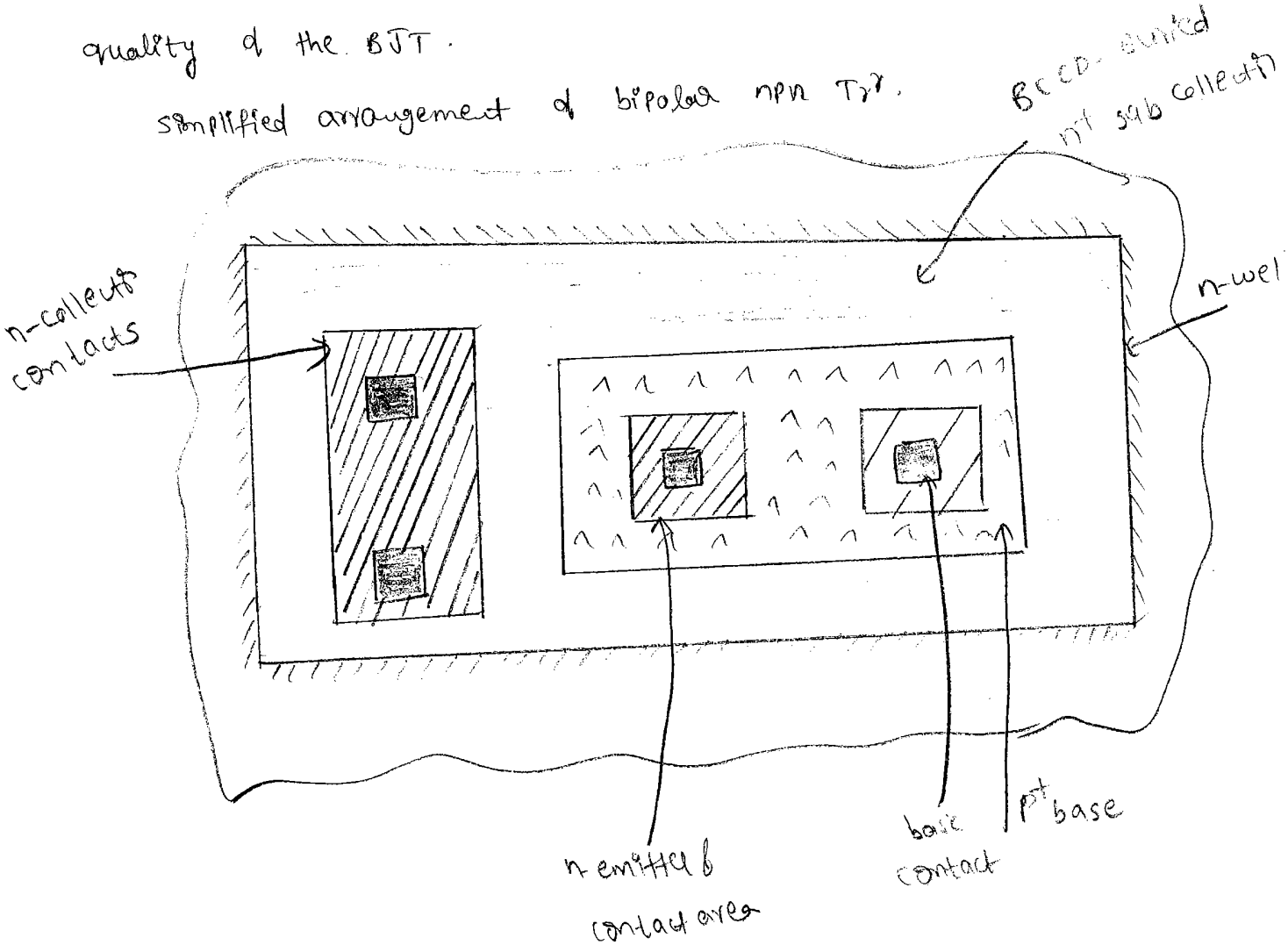
Bi-cmos Technology :-

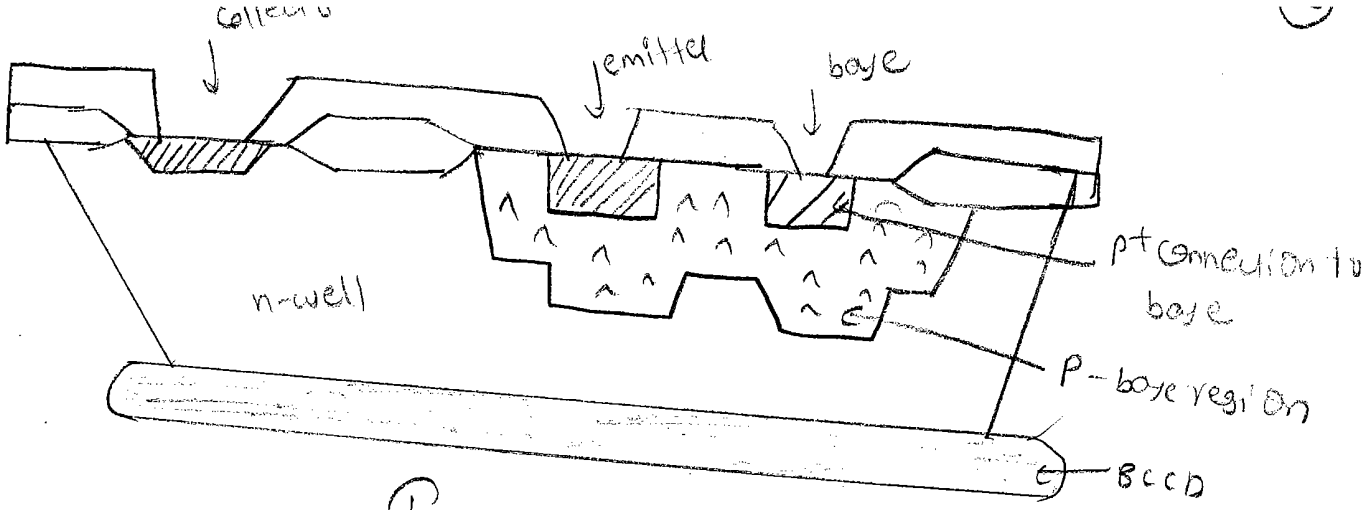
The production of npn bipolar Transistors with good performance ch's can be achieved for example, by extending the standard n-well cmos processing to include further masks to add 2 additional layers — The n^+ subcollector
— p^+ base layer

The npn Tr is formed in an n-well and additional p^+ base region is located in the well to form the p-base region of Tr.

→ The 2nd layer (additional), the Buried n^+ subcollector (BCCD) is added to reduce n-well (collector) resistance & thus improve quality of the BJT.

simplified arrangement of bipolar npn Tr.





(b) cross section

Bicmos fabrication in an n-well process:

→ Form n-well & form source, gate, drain for both pmos & nmos.

→ Then additional masks to define

(1) pt base region
(2) nt collector region
(3) Buried sub collector.

Cmos

(1) Form n-well
(3) Define active area
(5) Vt adjustment
(6) Define poly/gate area
(7) Form nt active area
(8) Form pt active area
(10) Contact cuts
(11) metal area

Additional steps for Bipolar.

(2) Form buried nt layer
(4) Form deep nt collector
(9) Form pt base for bipolars

Bicmos Technology goes some way toward combining the virtues of both Technologies.

Comparison b/w CMOS & BJT:-

CMOS	BJT
(1) Low static power dissipation	(1) High power dissipation.
(2) High i/p impedance	(2) Low i/p impedance (high drive current)
(3) High packing density	(3) Low packing density
(4) High delay sensitivity to load	(4) Low delay sensitivity to load.
(5) Low o/p drive current	(5) High o/p drive current
(6) Low ~~o/p~~ ~~drive~~ gm (gm α Vin)	(6) High gm (gm α eVin)
(7) Bidirectional capability (source & drain interchangeable)	(7) Essentially unidirectional
(8) Ideal switching device → scalable threshold voltage → High noise margin	

To take maximum advantage of si Technology one might envisage the following mix of Technologies in a si system

CMOS for logic

Bi-CMOS for I/o & driver circuits

ECL for critical high speed parts of the system.

Diffusion:- In order to achieve selective doping, the technique most commonly used in silicon processing is called as "diffusion".

→ The basic principle underlying this process is that the dopant atoms migrate from a region of high concentration to the region of low concentration.

→ In simple diffusion is the process of introducing controlled amounts of dopants into the semiconductors.

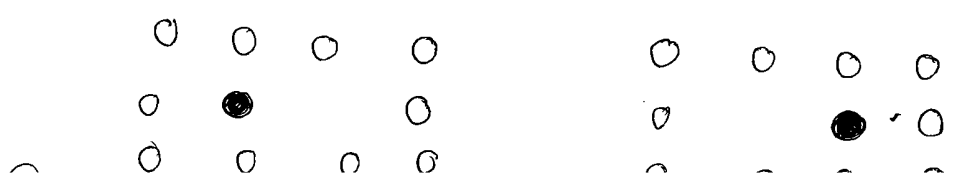
Three kinds of situations arise in the process of diffusion.

1. substitutional diffusion
2. Interstitial "
3. Interstitialcy "

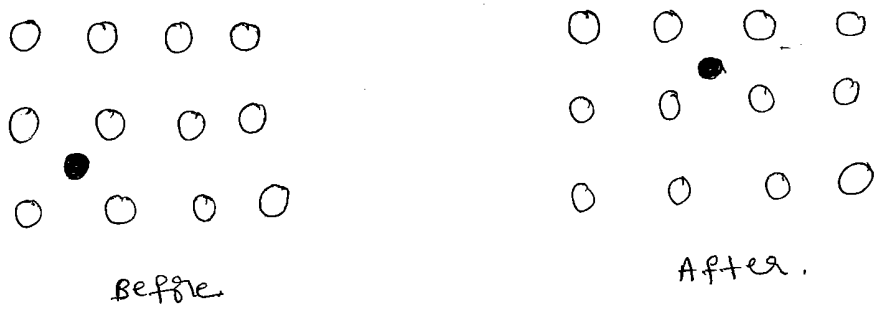
Substitutional Diffusion:—

An impurity atom wanders through the crystal by jumping from one lattice site to the next, thus substituting for the original host atom. It is necessary that this adjacent site be vacant. i.e. vacancy must be present to allow substitutional diffusion to occur.

Note: Due to high temperature, silicon atoms get removed from its lattice position in the crystal & the impurity atom takes its place.

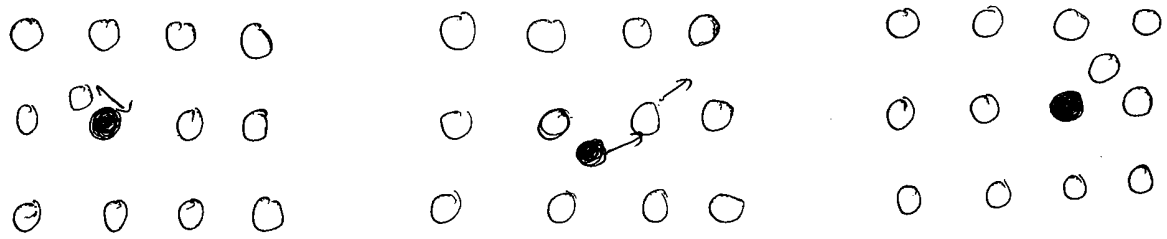


Interstitial diffusion :— An impurity atom move through the crystal lattice by jumping one interstitial site to the next. Interstitial diffusion requires that jump motion occurring from one interstitial site to another adjacent interstitial site. This process is relatively fast, because of large number of vacant interstitial place in the semiconductor crystal.



Before. After.

Interstitialy diffusion :— This is modified version of substitutional diffusion. Interstitial host atoms can be annihilated by pushing substitutionally located impurity atoms in interstitial sitey. Theye impurities can now diffuye to adjacent substitutional sitey & create new self-interstitialy.



Diffusion Equation :

The basic diffusion proces is similar to that of charge carriers (Es & holes). we define flux 'F' as the no. of dopant atoms passing through a unit area in unit time and 'C' as

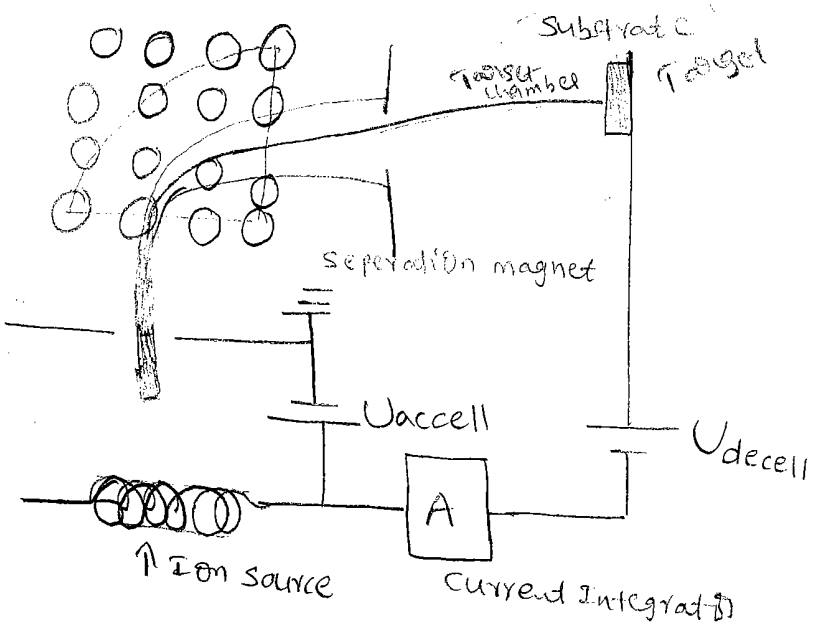
then $F = -D \frac{\partial C}{\partial X}$

C = Carrier concentration

D = diffusion coefficient (or) diffusivity.

Ion implantation :-

Ion implantation is alternative technique for selective doping of semiconductors. The doping profile is more precisely controlled by this Technique.



Ion implantation setup with mass seperator.

→ Ion implantation equipement typically consists of an ion source, where ions of the desired element are produced, an accelerator where the ions are electrostatically accelerated to a high energy & a target chamber where the ions impinge on a target, which is the material (silicon substrate/ wafer) to be implanted.

→ Each ion is typically a single atom & thus the actual amount of material implanted in the target is the integral over time of the ion current. This amount is called "dose". [material implanted: $\int_t I$ (ion current)] dose

→ When these ions enter into the semiconductor, they loose the kinetic energy through a series of collisions with the electrons as well as nuclei of the lattice atoms.

→ Finally the impurity atom comes to rest when its K.E Fall to zero.

→ ion energy: 10 to 500 eV

implantation dose ⇒ $Q_0 = \frac{J_t}{q}$ ion beam current density & time t,

Thermal oxidation :— → By varying energy of ion beam, we can change dose

In micro fabrication, "Thermal oxidation" is a way to produce a thin layer of oxide on the surface of a wafer. This is usually carried out in an open tube furnace at the temperature range of 900–1200°C. A single furnace accepts many wafers at the same time, in a specially designed quartz rack called a "boat". The boat enters the oxidation chamber from one side & holds the wafers vertically, beside each other.

Types

① Dry oxidation ② Wet oxidation.

Dry oxidation:- If oxidation is carried out in an atmosphere of dry oxygen, it is known as "dry oxidation".

⇒ Oxygen is passed through the tube where it reacts with the silicon to form SiO_2

$$Si(s) + O_2(g) \rightarrow SiO_2(s)$$

Wet oxidation :- If oxidation is carried out in water vapour, it is known as "wet oxidation".

→ high purity de-ionized water kept in quartz bubbler at the inlet of the furnace is heated to a temperature close to the boiling point. High purity oxygen or nitrogen is passed through it so that the gas flowing into the furnace is saturated with the water vapour.

$$Si(s) + 2H_2O(l) \rightarrow SiO_2(s) + 2H_2(g).$$

(liquid)

Kinetic of Thermal oxidation :-

Deal-Grove model :-

The Deal-Grove model mathematically describes the growth of an oxide layer on the surface of a material.

→ It is used to analyze the thermal oxidation of silicon in semiconductor device fabrication.

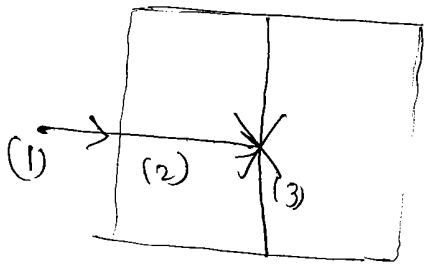


Fig. oxidation process

→ The model assumes that oxidation occurs at the interface b/w the oxide and substrate, rather than b/w the oxide and the ambient gas.

(1) Indicates, It diffuses from the bulk of the ambient gas to the surface.

(2) It diffuses through the existing oxide layer to the oxide-

③ It reacts with the substrate.

→ The oxide thickness grown on the silicon by the process of dry & wet oxidation is dependent on the oxidation time and temperature. This thickness can be expressed as a linear-parabolic relation

$$d^2 + Ad = B(t + \tau)$$

d = oxide thickness

A & B are co-efficients that depend on the oxidation time and temperature.

t = oxidation time

τ = parameter for fitting the initial value of the oxide thickness.

For short duration of time, $d \ll A$ then

$$Ad = \frac{B(t+\tau)}{d^2}$$ (we can neglect d^2).

$$\frac{B(t+\tau)}{d^2} \simeq B(t+\tau)$$

$$d = \frac{B(t+\tau)}{A}.$$

Above equation says, when oxidation is carried out for short duration of time, the oxide thickness increases linearly with time.

For longer duration of oxidation $(t+\tau) >> \left(\frac{A^2}{4B}\right)$, the oxide thickness can be expressed as,

$$d = \sqrt{Bt}.$$

Lithography :-

Semiconductor lithography is a process of drawing patterns on a silicon wafer. The patterns are drawn with a light-sensitive Polymer called "Photoresist".

→ These patterns define various regions in an Integrated circuit such as Implantation regions, contact windows etc.

→ The choice for performing this patterning is "optical lithography". It is basically a photographic process by which the light-sensitive Polymer (photoresist) is exposed and developed to form three-dimensional images on the substrate.

Optical lithography systems :-

Photomask :- The photomask is an essential component in semiconductor lithography. It contains the detailed blueprint of the designed circuit.

→ Using the photomask, specific images of detailed devices are transferred onto the surface of the silicon wafers by means of "Photolithography".

→ A photomask is used just like the negative in Photography that captures specific image for later reproduction.

→ In photography, multiple copies of photos are reproduced using the original image captured on the negative.

Likewise a photomask produces duplicate images of patterns onto

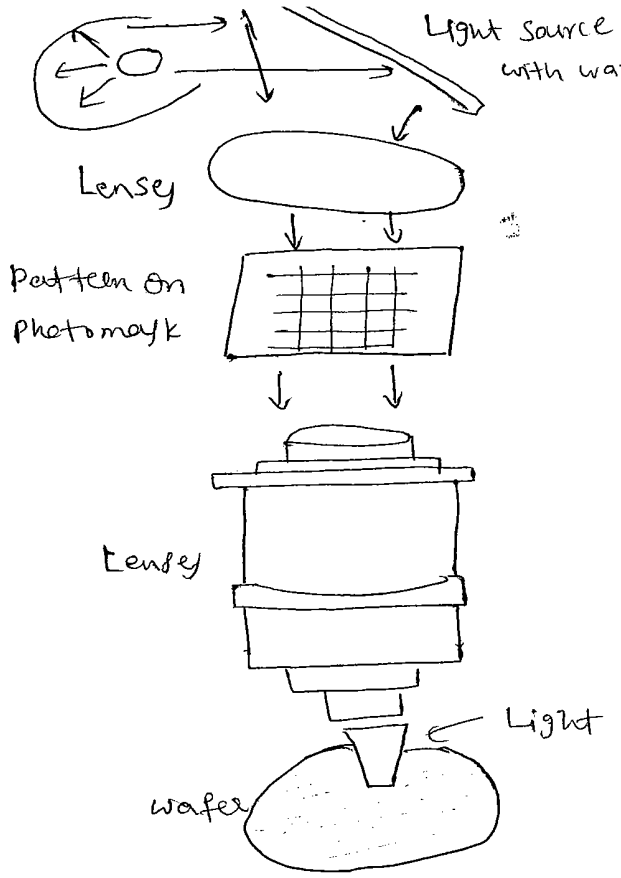


Fig: Optical lithography system.

→ A single photomask plate produces identical image on thousands of wafers.

→ As the quality of the finished photograph is determined by the quality of the original film, the quality of the photomask determines the ultimate quality of semiconductor chips.

→ The material used for building photomasks is a quartz plate upon which detailed image of patterns are formed.

→ The Pattern & image are then transferred onto the wafer surface by shining light through the quartz plate.

General methods used to expose photoresist are

① Contact photolithography
② Proximity "
③ Projection "

Contact photolithography :-

In this, the mask is kept in direct contact with the substrate and exposure is done.

→ It offers high resolution. But practical problems such as mask damage and resultant low yield make this process unusable in most production environments.

Proximity photolithography :-

→ Similar to contact lithography & except that there is a small gap of a few microns b/w wafer and mask during exposure.

→ This results in optical diffraction which results a limit on the resolution.

Projection photolithography :-

The most common method of exposure is projection printing.

→ An image of the mask is projected onto the wafer.

→ 2 main classes of projection lithography tools

① Scanning
② Step-and-Repeat systems

Electron Beam lithography:

This is a direct analogy with photolithography, where electron beam exposure alters the chemistry of the resist instead of light exposure.

→ The most common EBL resist is Polymethyl — PMMA.

Ion-Beam lithography :-

→ It can achieve higher resolution than optical, X-ray and e beam lithography because ions have higher mass and therefore scatter less than electrons.

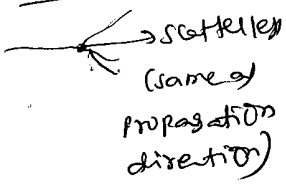
→ Ion-beam lithography scans an ion beam across a surface to form a pattern.

2 Types of ion-beam lithography

① Scanning focussed beam systems

② mask beam system.

Scatter



→ Former system is similar to beam lithography in which ion source can be Gas or H+.

→ 2nd method, similar to an optical 5x reduction projection step and repeat system in which project 100 keV light ions such as H+ through a stencil mask.

Metallization :-

In semiconductor process technology, metal refers to a material with very high electrical conductivity.

→ metal is evaporated on the substrate and is patterned into wires whenever a connection is needed on an IC.

→ Aluminium is the most process - friendly metal & has low resistivity.

Group of metal layers

1. metal1, first level of interconnect
2. via1, to connect metal1 & metal2
3. metal2, second level of interconnect
4. via2, to connect metal2 & metal3
5. metal3
6. via3, 3 & 4
7. metal4
8. via4 4 & 5
9. metal5
10. via5 5 & 6
11. metal6
12. via6 6 & 7
13. metal7, 7th level of interconnect.

Encapsulation (Packaging) :-

A package is the housing of a semiconductor chip. It protects and preserves the performance of the semiconductor device from electrical, mechanical & chemical

Corruption & Impairment.

→ It electrically interconnects the chip with outside circuitry.

→ It is designed to dissipate heat generated by the chip.

A Package is a plastic, ceramic, laminate, & metal seal that encloses the chip or die inside.

Package classified into 2 categories.

① pin-through-hole (PTH) package:

have pins are inserted into through-holes in the board and soldered in place from the opposite side of the board.

→ The through-hole mounting approach offers a mechanically reliable & sturdy connection.

② surface-mount-technology (SMT) Package:-

have leads that are soldered directly to the metal leads on the surface of the circuit board.

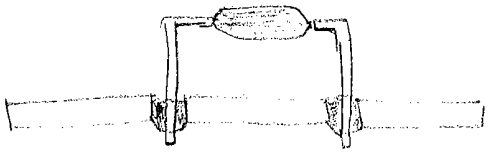
→ Preferred one (SMT)

→ Packing density is increased for the following reasons

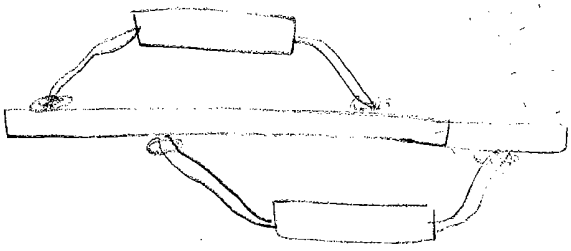
① through holes are eliminated, which provide more wiring space.

② lead pitch is reduced

③ Chips can be mounted on both sides of the board.



① through-hole mounting



surface mount

Resistors :-

Resistors have been available for use in IC's for many years.

→ Some of these are made in silicon, so they are directly integrated with the rest of the IC processes.

→ Usually resistors in IC's are characterized in terms of their sheet resistance rather than their absolute resistance value.

→ Sheet Resistance, R_{sheet} is defined as the resistance of a resistive strip with equal length and width

$$R = R_{sheet} * \text{number of squares where } W = L.$$

$\rho \rightarrow$ material resistivity (Ωm)

$t \rightarrow$ thickness (m).

Integrated semiconductor Resistors :-

→ In this category, the existing semiconductor is used as the resistive material.

→ The resistor may be fabricated at a no. of stages during the IC process giving rise to different resistors with different characteristics.

Types

(1) Diffused Resistors :-

Formed during either the base or emitter diffusion of bipolar process.

→ For an npn process the base diffusion resistor is a P-type of moderate sheet resistivity typically in the range of 100 – 200 Ω/m. This can provide resistors in 50 – 10kΩ range.

→ The heavily doped n+ emitter diffusion will produce an n+ type resistor with low sheet resistivity of 2–10 Ω/m. Provide resistors in 1–100Ω range.

Pinched resistors :–

→ variation to the diffused resistor that is used to increase the sheet resistivity of base region is to use the n+ type emitter as a means to reduce the cross-sectional area of the base region thereby increasing sheet resistivity.

Epitaxial Resistors :–

→ High resistor values can be formed using the epitaxial layer since it has higher resistivity than other regions.

→ These resistors can have sheet resistances around 5kΩ/m.

MOS Resistors :–

A MOSFET can be biased to provide a non-linear resistor.

→ such a resistor provides much greater value than diffused one while occupying a much smaller area.

→ with the gate shortened to the drain in a MOSFET a quadratic relation b/w current and voltage conducts current only when the

voltage exceeds the threshold voltage.

→ Under these circumstances, the current flowing in this resistor (i.e, the MOSFET drain current) depends on the $\frac{W}{L}\mu_n C_{ox}$ of the channel.

→ To ↑ resistor value, aspect ratio of the MOSFET should be reduced to give longer channel length & narrower channel width.

Capacitors :-

most integrated capacitors are either junction capacitors or MOS capacitors.

Junction capacitors :-

→ Is formed when a P-n Junction is reverse-biased.

→ This can be formed using the base-emitter, base-collector or collector-substrate junctions of an npn structure in bipolar Ic's.

→ Particular Jn must be maintained in reverse bias to provide desired capacitance.

→ The capacitance is voltage dependent decreasing with increased Reverse bias. Capacitence depends on Reverse voltage.

→ base-emitter Jn provides 1000 pF/mm² highest capacitance per unit with low breakdown voltage. (~5V)

→ base-collector jn provides ~100 pF/mm² with higher breakdown voltage (~40V)

Mos capacitors:-

→ mos capacitors are usually formed as parallel plate devices with a top metallization & high conductivity n+ emitter diffusion as the 2 plates with a thin oxide dielectric sandwiched in b/w.

→ mos capacitors can provide around 1000pF/mm² with breakdown voltage upto 100V.

→ These are voltage independent & can be biased either positively or negatively.

Probe testing :-

A wafer prober is a machine used to test IC's.

→ For electrical testing a set of microscopic contacts or probes called a "Probe card" are held in place whilst the wafer, vacuum-mounted on a wafer chuck, is moved into electrical contact.

→ The wafer prober is responsible for loading or unloading the wafers from their carrier and is equipped with automatic pattern recognition optics capable of aligning the wafer with sufficient accuracy to ensure accurate Registration b/w contact pads on the wafer & the tips of the probes.