# Basics of Operational Amplifiers
# UNIT – I

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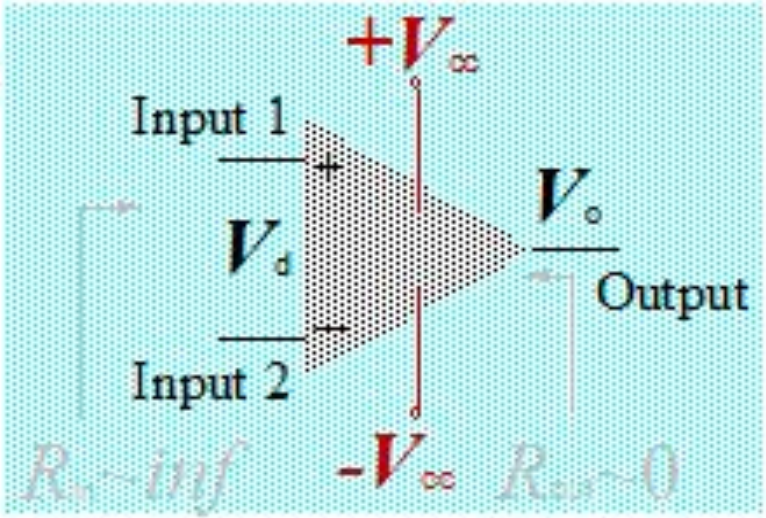
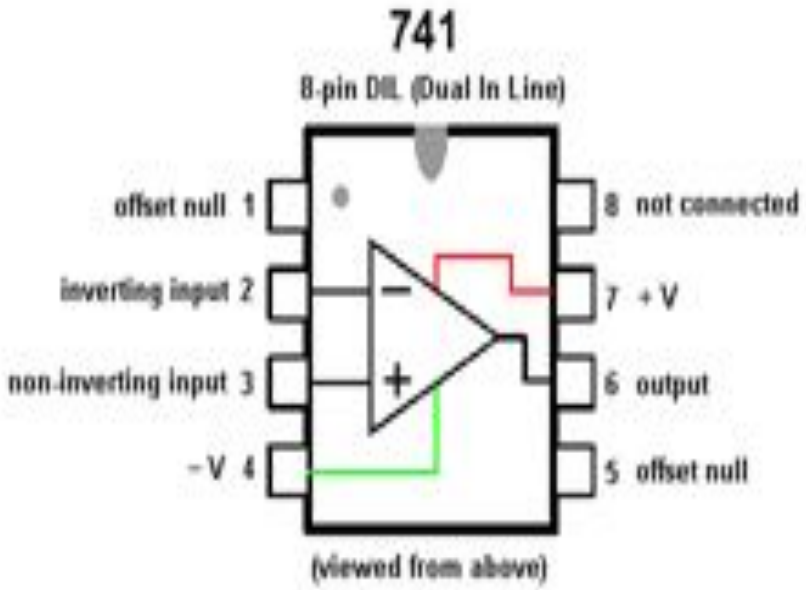
# Operational Amplifier (Op-Amp)

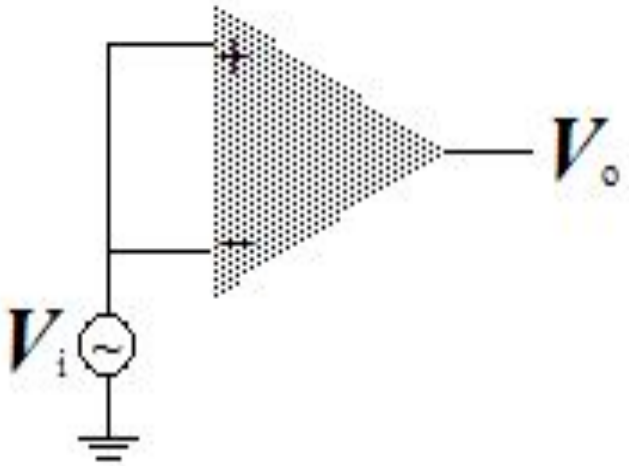
- Very high differential gain
- High input impedance
- Low output impedance
- Used in oscillator, filter and instrumentation
- Accumulate a very high gain by multiple stages






# Common-Mode Operation

- Same voltage source is applied at both terminals
- Ideally, two input are equally amplified
- Output voltage is ideally zero due to differential voltage is zero
- Practically, a small output signal can still be measured



# Common-Mode Rejection Ratio (CMRR)

Differential voltage input :

$$V_d = V_+ - V_-$$

Common voltage input :

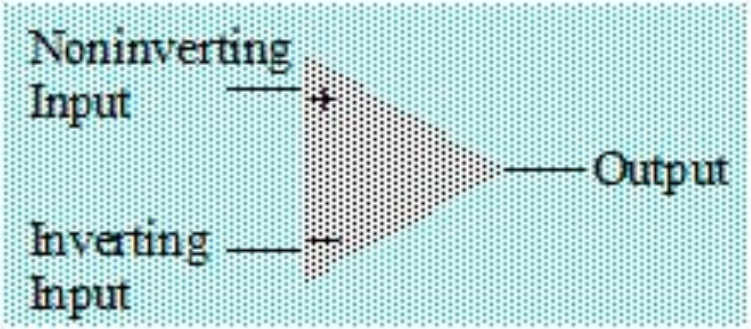
$$V_c = \frac{1}{2}(V_+ + V_-)$$

Output voltage :

$$V_o = G_d V_d + G_c V_c$$

$G_d$ : Differential gain

$G_c$ : Common mode gain



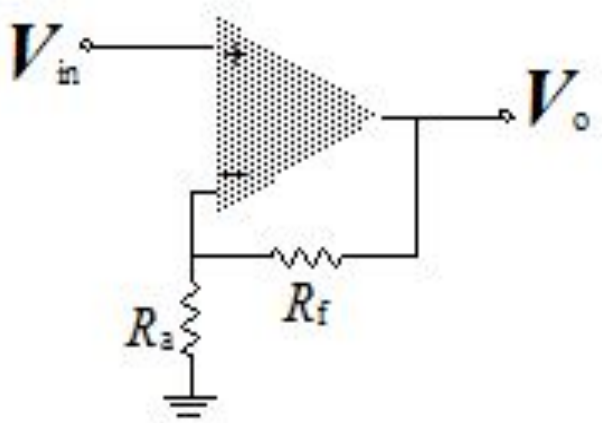

Common-mode rejection ratio:

$$\text{CMRR} = \frac{G_d}{G_c} = 20\log_{10}\frac{G_d}{G_c}(\text{dB})$$

# Noninverting Amplifier

(1) Kirchhoff node equation at $V_+$ yields, $V_+ = V_i$

(2) Kirchhoff node equation at $V_-$ yields, $\frac{V_- - 0}{R_a} + \frac{V_- - V_o}{R_f} = 0$



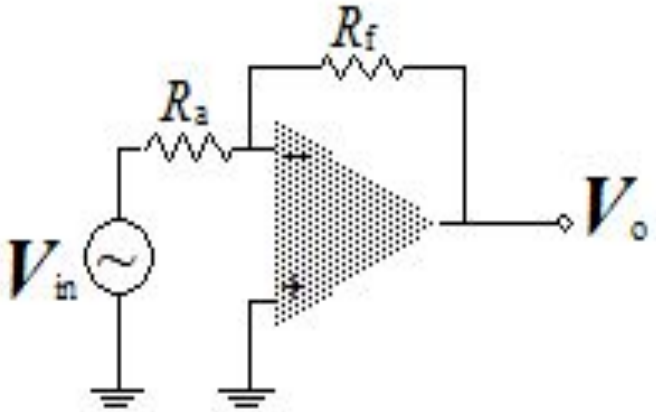

$V_+ = V_-$ yields

$$\frac{V_i}{R_a} + \frac{V_i - V_o}{R_f} = 0 \quad \text{or} \quad \frac{V_o}{V_i} = 1 + \frac{R_f}{R_a}$$

# Inverting Amplifier

(1) Kirchhoff node equation at $V_+$ yields, $V_+ = 0$

(2) Kirchhoff node equation at $V_-$ yields, $\frac{V_{in} - V_-}{R_a} + \frac{V_o - V_-}{R_f} = 0$




$V_+ = V_-$ yields

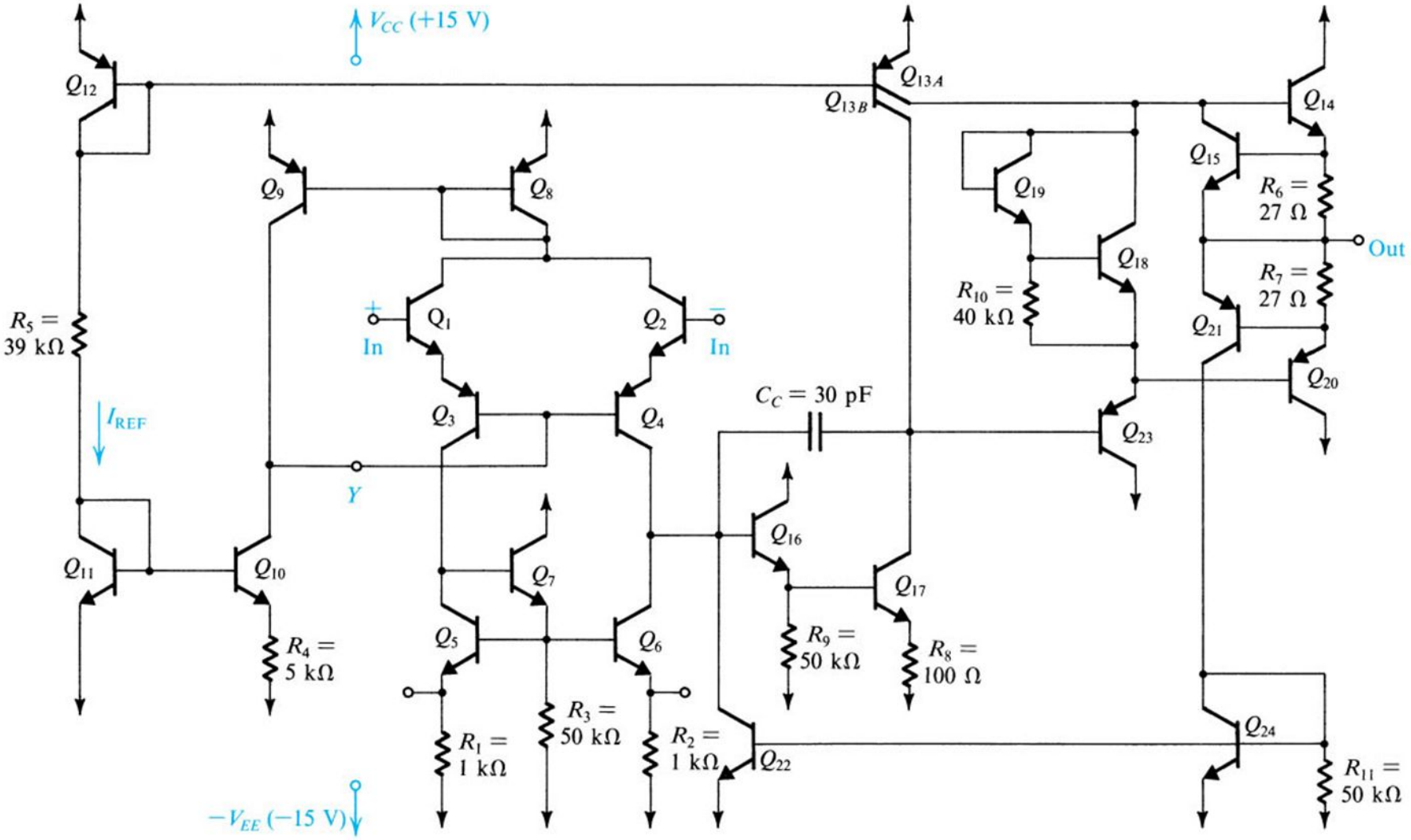
$$\frac{V_o}{V_{in}} = \frac{-R_f}{R_a}$$

# Characteristics of Ideal Op-Amp

- For an ideal Op-Amp, $V_1 = V_2 = 0$ and hence $I_1 = i_2 = 0$
- Open loop voltage gain $A_{OL} = \infty$
- Input Impedance $R_i = \infty$
- Output Impedance $R_o = 0$
- Bandwidth BW $= \infty$

# Stages and Internal circuit of general Op-Amp (IC 741)

- General Stages
  - Input Stage
  - Intermediate Stage
  - Buffer and Level Shifting Stage
  - Output Stage



# The Input Stage

- The input stage consists of transistors *Q1* through *Q7*.
- *Q1*-*Q4* is the differential version of CC and CB configuration.
- High input resistance.
- Current source (*Q5*-*Q7*) is the active load of input stage. It not only provides a high-resistance load but also converts the signal from differential to single-ended form with no loss in gain or common-mode rejection.

# The Intermediate Stage

- The intermediate stage is composed of $Q_{16}$, $Q_{17}$ and $Q_{13B}$.
- Common-collector configuration for $Q_{16}$ gives this stage a high input resistance as well as reduces the load effect on the input stage.
- Common-emitter configuration for $Q_{17}$ provides high voltage gain because of the active load $Q_{13B}$.
- Capacitor Cc introduces the miller compensation to insure that the op amp has a very high unit-gain frequency.

# Level Shifting Stage

- All stages coupled to each other, hence voltage level of previous stage applied to next stages.
- So stage by stage d.c level increases , such high voltage drives the transistors into saturation
- Hence before output stage, it is necessary to bring such high voltage to zero volt.
- Level shifter brigs the d.c level down to ground potential when no signal is applied
- The buffer is an emitter follower whose input impedance is very high.

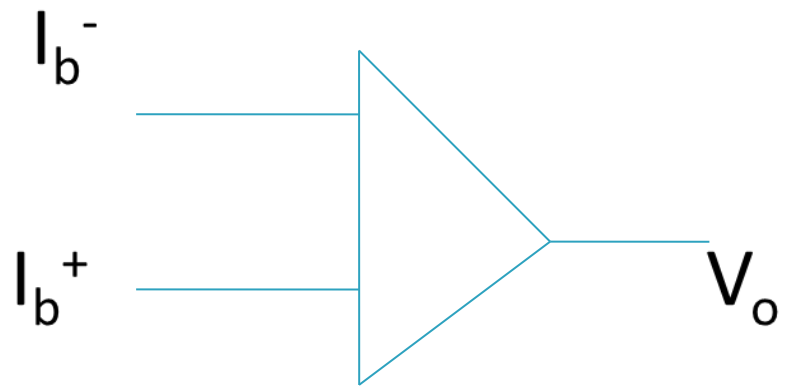
# The Output Stage

- The output stage is the efficient circuit called class AB output stage.
- Voltage source composed of $Q_{18}$ and $Q_{19}$ supplies the DC voltage for $Q_{14}$ and $Q_{20}$ in order to reduce the cross-over distortion.
- $Q_{23}$ is the CC configuration to reduce the load effect on intermediate stage.
- Short-circuit protection circuitry
  - Forward protection is implemented by $R_6$ and $Q_{15}$.
  - Reverse protection is implemented by $R_7$, $Q_{21}$, current source($Q_{24}$, $Q_{22}$) and intermediate stage.

# DC Characteristics

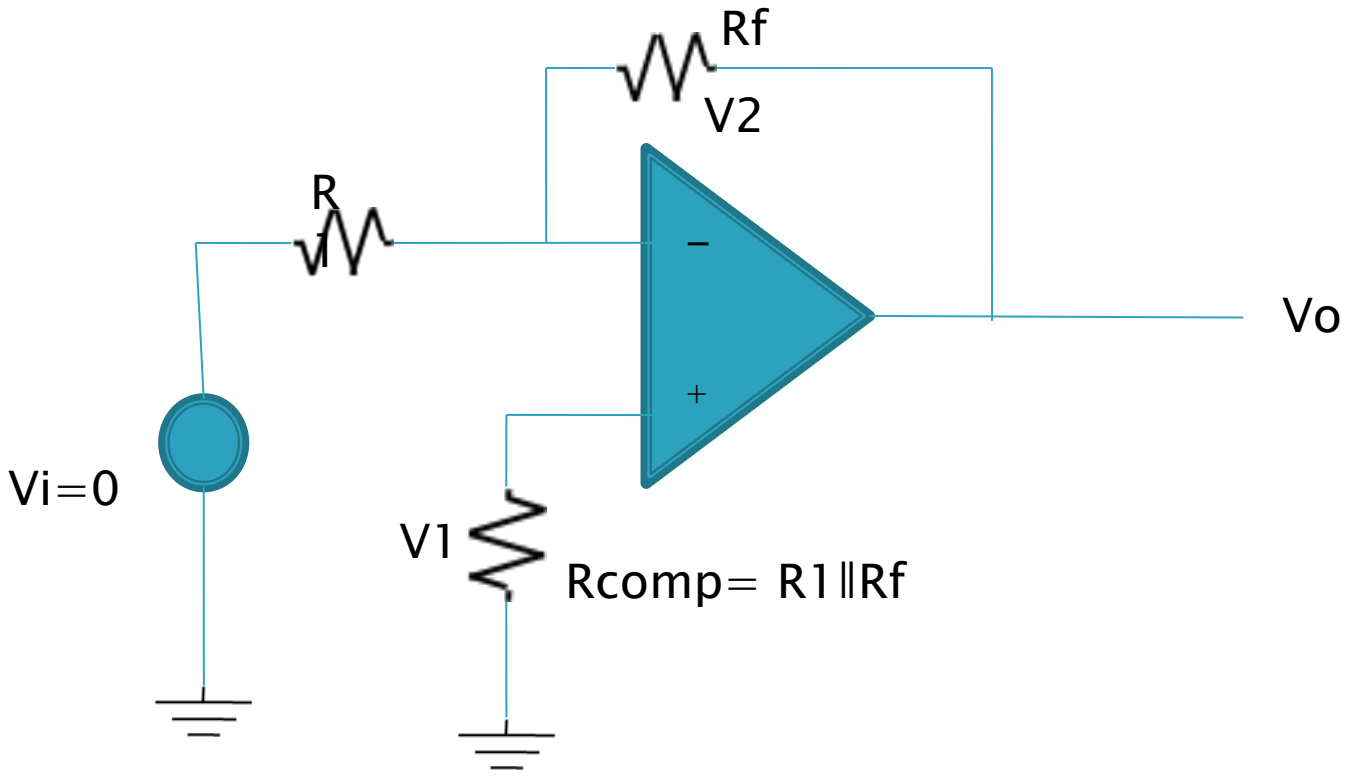
- Input Bias Current ($I_b$)
- Input Offset Current($I_{os}$)
- Input Offset Voltage ($V_{ios}$)
- Thermal Drift

# Input Bias Current

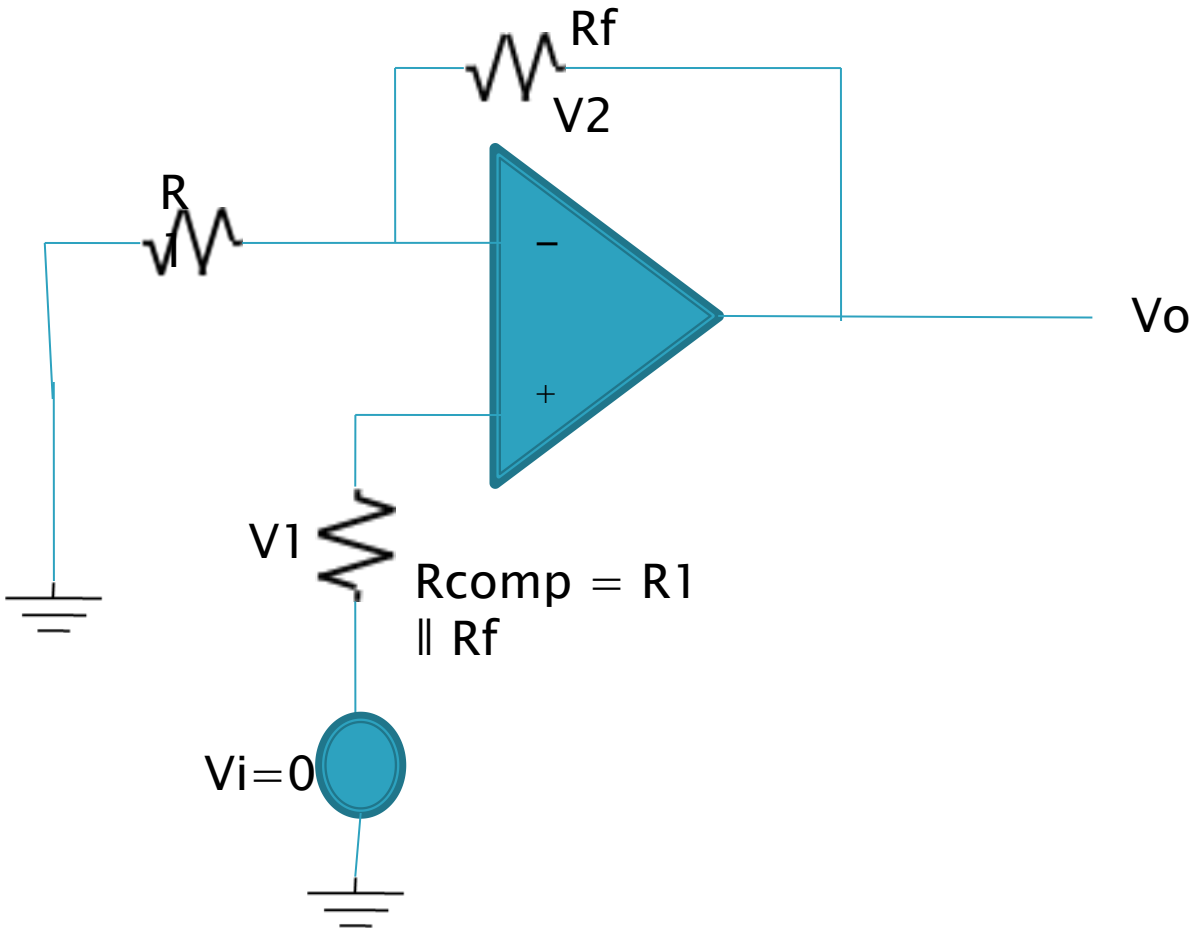



Bias Current $I_B = \frac{I_b^+ + I_b^-}{2}$

# Bias Current Compensation in Inverting mode



# Bias Current Compensation in Non Inverting mode



# Input Offset Current

- Input Offset current will work if both bias currents are equal.
- If they are not equal, the difference between them is know as Input Offset current

$$I_{os} = I_b^+ - I_b^-$$

# Input Offset Voltage

- Due to unavoidable imbalances inside the op-amp, the output voltage will not be zero with zero input voltage. This voltage is called as input offset voltage.

Considering this voltage $V_{ios}$,

Output Voltage $V_o = (1 + \frac{R_f}{R_1})V_{ios}$

# Thermal Drift

- Bias current, Offset current and Offset voltages change with temperature. This change is called as drift.
- Offset current drift is expressed in nA/$^0$C
- Offset voltage drift is expressed in mV/$^0$C
- To avoid this drift careful printed circuit board layout must be used and forced air cooling may be used to stabilize the ambient temperature.

# AC Characteristics (Slew Rate – SR)

- The maximum rate of change of output voltage caused by step input voltage , specified in V/μs
- **Cause of SR**:

There is a **capacitor** within an op-amp which prevent the output voltage from responding immediately to a fast change in input. This capacitor caused the SR

- For example, if $V_o = V_m \sin \omega t$

Then the rate of change of output is,

$$\frac{dv_o}{dt} = V_m \omega \cos \omega t$$

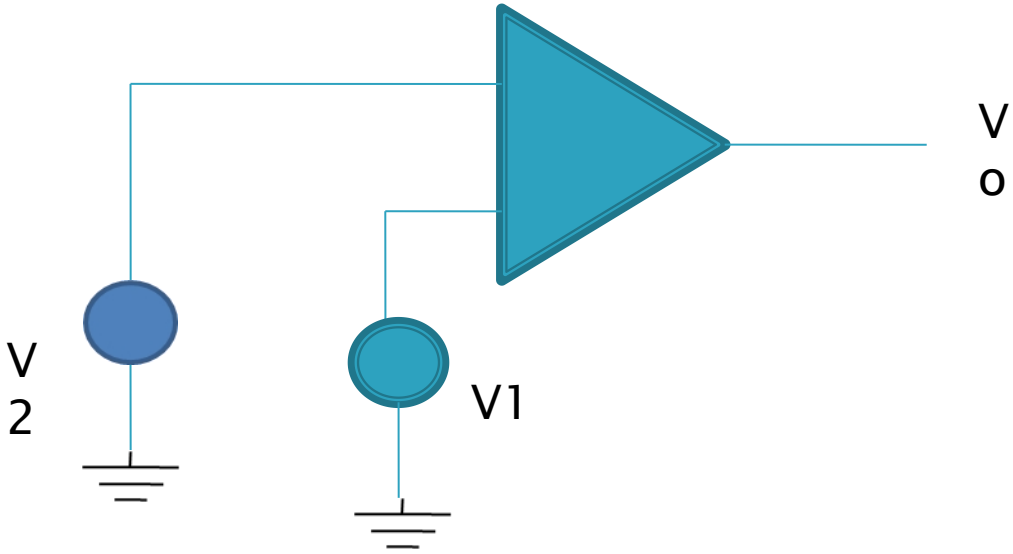
The maximum rate of change occurs when $\cos \omega t = 1$

Therefore SR = $(dv_o/dt)\max = \omega V_m$

Or SR = $2\pi f V_m$ V/s

Or SR = $\frac{2\pi f V_m}{10^6}$ V/μs

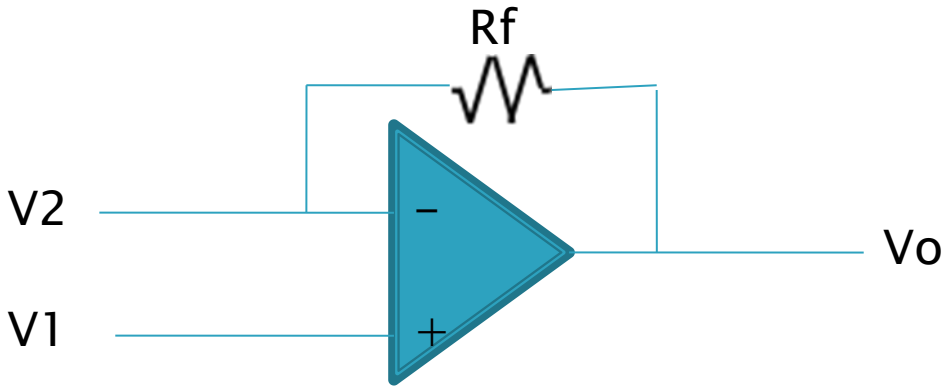
# Open Loop Operation



# Open loop operation

- Simplest way of operation in op-amp
- $V_1$ and $V_2$ applied to non-inverting and inverting terminals respectively
- Vo will be either at positive saturation or negative saturation as $V_1 > V_2$ or $V_2 > V_1$ respectively
- Hence amplifier acts as switch only
- Applications as voltage comparator, zero crossing detector.

# Closed Loop Operation

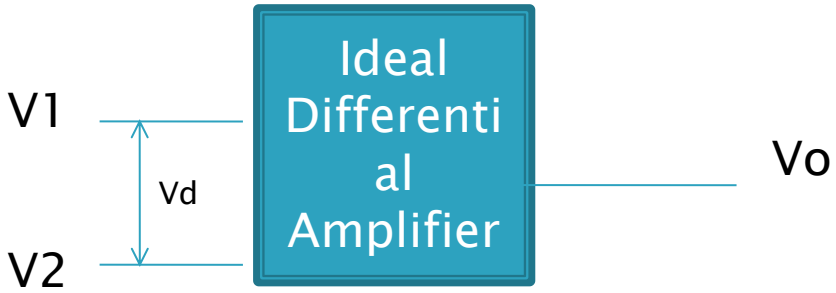


# Closed loop Operation

- Mostly used configuration
- The feedback allows to feed the some part of output back to input
- The feedback is said to be negative as the resistor connects the output to inverting terminal
- Closed loop gain is much less than Open loop gain
- It reduces the possibility of distortion, increases the BW.

# Differential Amplifier

- Amplifies the difference between two input voltages. ($V_d = V_1 - V_2$)




- $V_o$ ά $(V_1 - V_2)$
- $V_o = A_d(V_1 - V_2)$ where $A_d$ = Differential Gain

  $V_o = A_d V_d$, hence $A_d = V_o / V_d$

  $A_d = 20 \log A_d$ (dB)

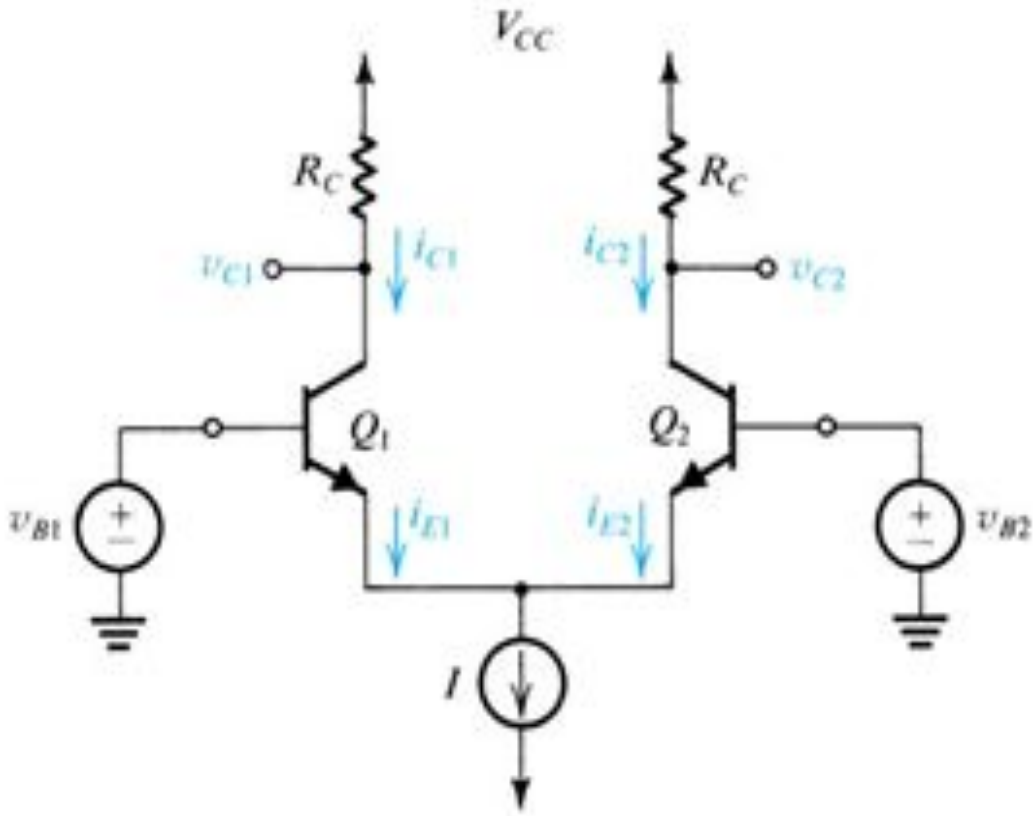
# Common Mode Gain

- If two input voltages are equal , it is common mode
- Then common mode voltage $V_c = (V_1+V_2) / 2$
- Now output voltage $V_o = A_cV_c$
- Total voltage for any differential amplifier is

$$Vo = A_dV_d + A_cV_c$$

- CMMR $= A_d/A_c$ (or) 20 log $(A_d/A_c)$ dB

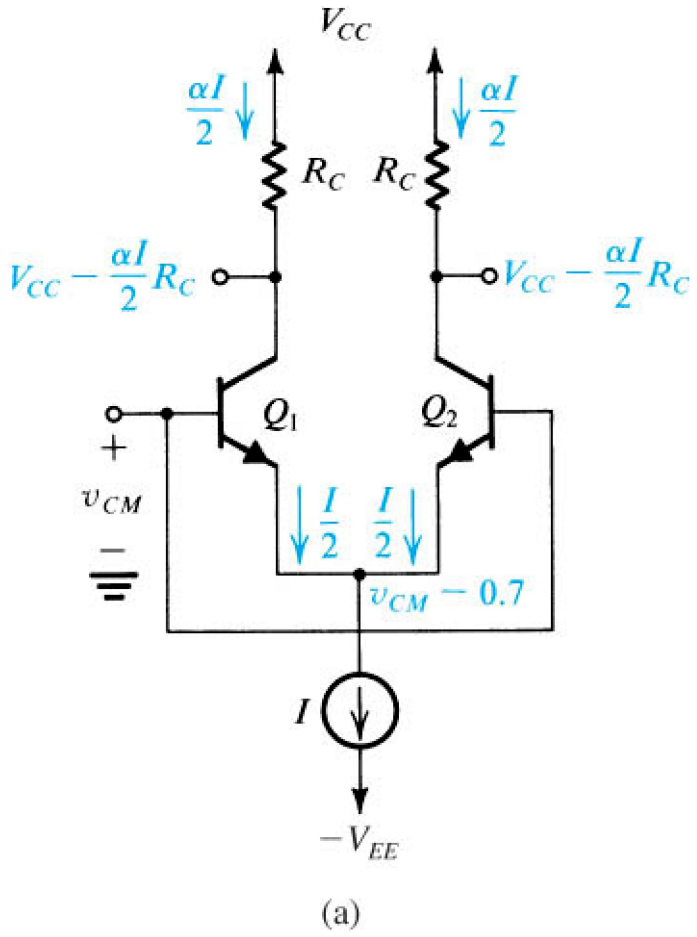
# BJT Differential Amplifier




The basic BJT differential-pair configuration.

# Difference Mode Operation

- Q1 positive going, Q2 negative going signal
- Hence there will be negative going output at the collector of Q1 and positive going output at the collector of Q2
- So the difference between two voltages Vo is the twice as large as the signal voltage.




(a)

## ➢Common Mode Operation

➢The differential pair with a common-mode input signal $V_{CM}$.

➢Two transistors are matched.

➢Current is divided equally between two transistors.

➢The difference in voltage between the two collector is zero.

# Configurations of Differential Amplifier

- Dual input , balanced output
- Dual input, unbalanced output
- Single input, balanced output
- Single input, unbalanced output

**Note:**

- If output is taken between two collectors – balanced output
- If output is taken between one collector with respect to ground then it is unbalanced output

# D.C Analysis of Differential Amplifier

Applying KVL to base-emitter loop,

$-I_B R_S - V_{BE} - 2I_E R_E + V_{EE} = 0$ ------(1)

But, $I_C = \beta I_B$ and $I_C \approx I_E$

Therefore, $I_B = I_E/\beta$ -------(2)

(2) In (1) we get,

$[-I_E R_S/\beta] - V_{BE} - 2I_E R_E + V_{EE} = 0$

$I_E[(-R_S/\beta) - 2R_E] + V_{EE} - V_{BE} = 0$ ---------(3)

Therefore

$$IE = \frac{V_{EE} - V_{BE}}{\left(\frac{R_S}{\beta}\right) - 2R_E}$$ ----------(4)

In practical,

$R_s/ 2R_E$, hence $I_E = [V_{EE}-V_{BE}]/2R_E$ ----------(5)

- The collector voltage of Q1

$$V_c = V_{cc} - I_c R_c \qquad \text{----(5)}$$

And $V_{CE} = V_c - V_E = (V_{CC} - I_C R_C) - (-V_{BE})$

$$V_{CE} = V_{CC} + V_{BE} - I_C R_C \qquad \text{----(6)}$$

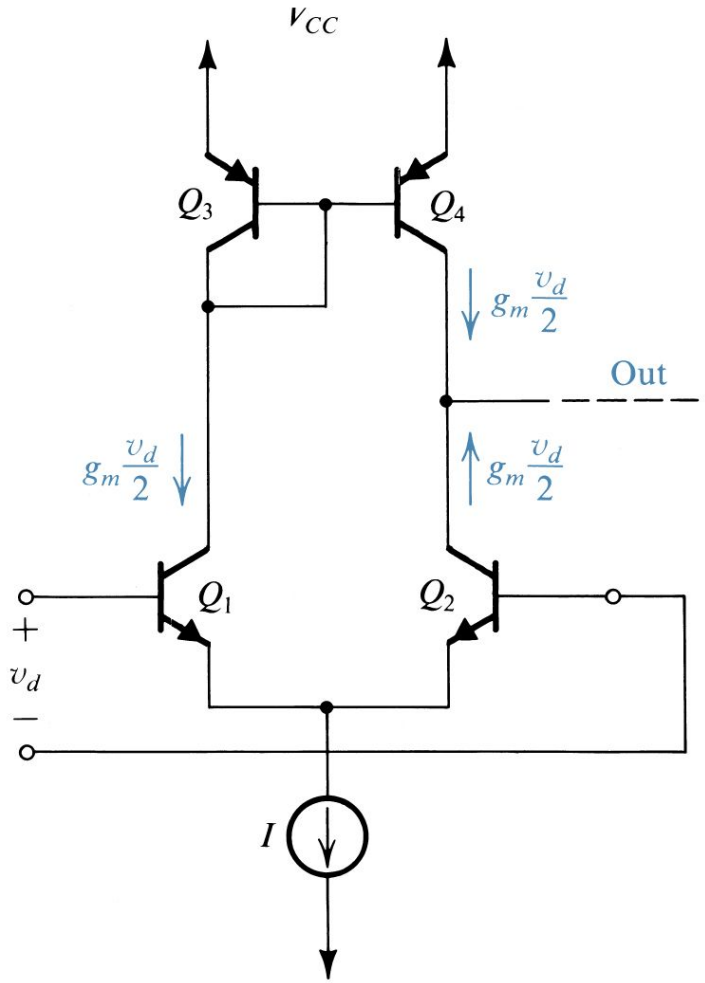
For the differential amplifier,

The operating point values

$$V_{CEQ} \approx V_{CE}$$

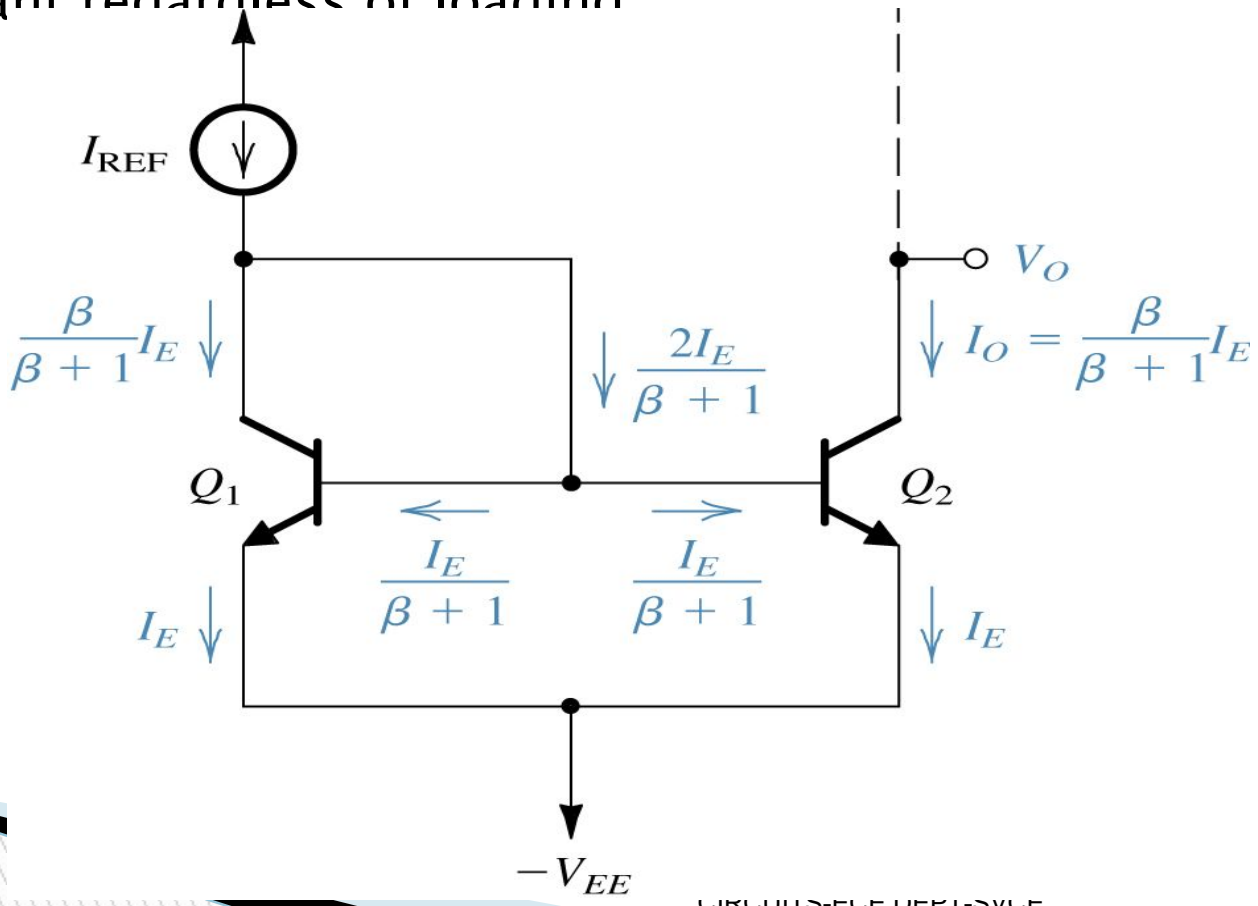
And $I_{CQ} \approx I_E$

# Differential Amplifier with active load

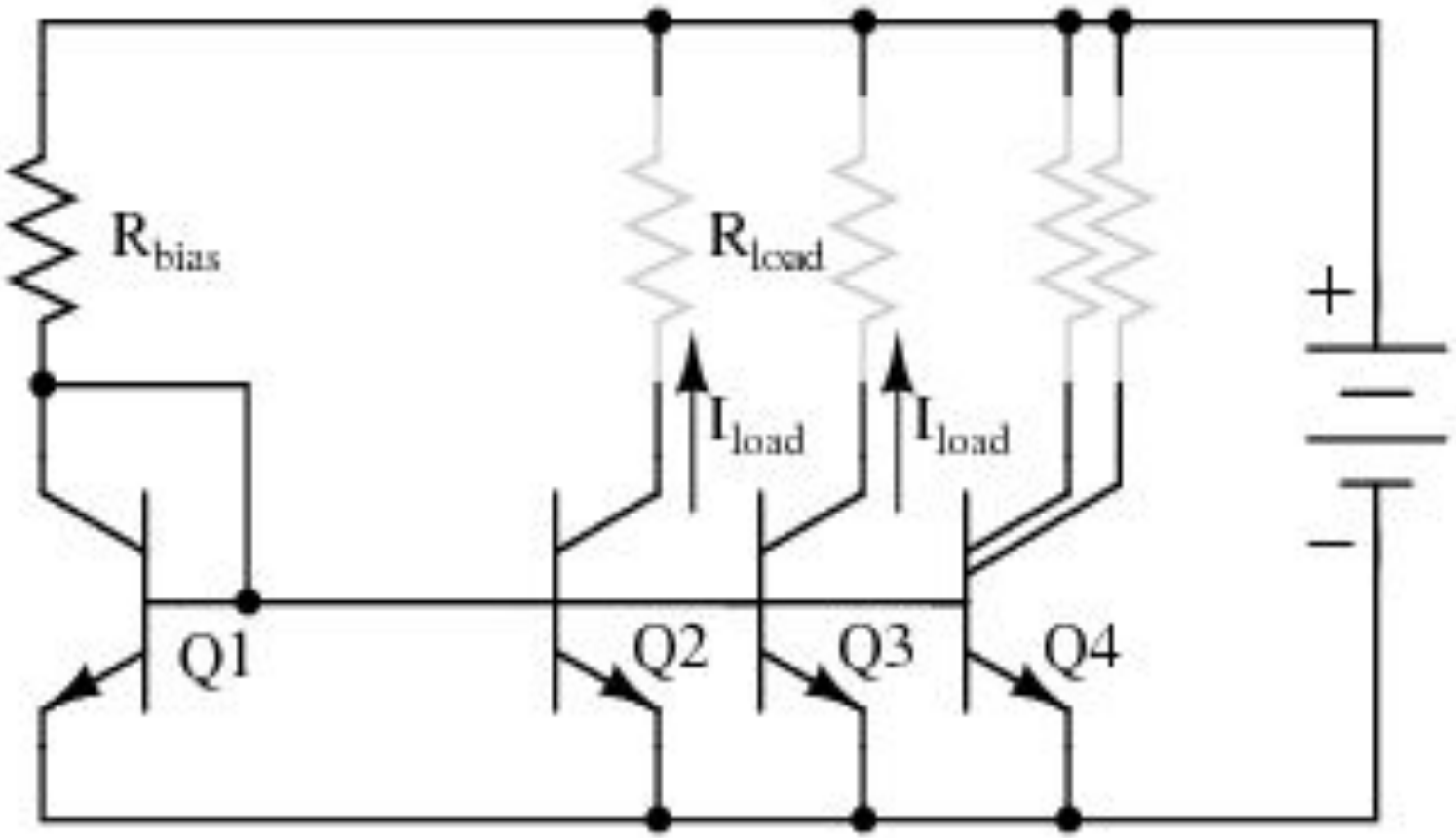


# Current Mirror Circuit

- A current mirror is a circuit designed to copy a current through one active device by controlling the current in another active device of a circuit, keeping the output current constant regardless of loading



# Multiple current mirror



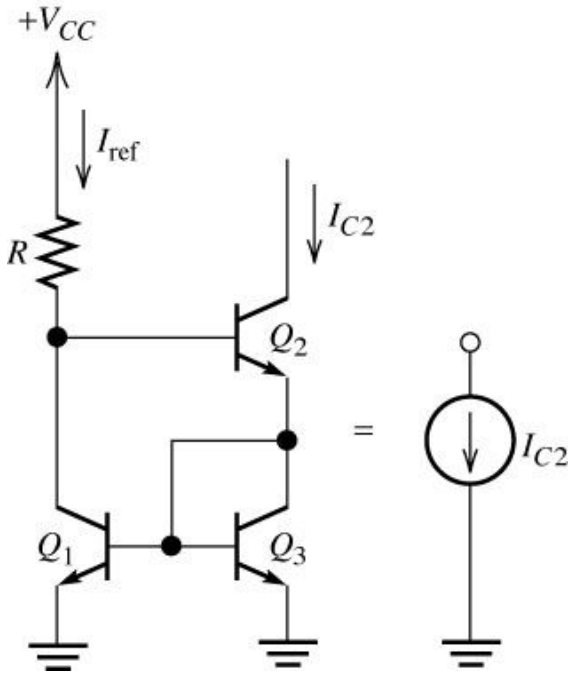
# The Wilson current source

An improved circuit, called Wilson current source, with higher output impedance that the previous current mirror.

For the Wilson current source, the following

$$I_{ref} = \frac{V_{CC} - V_{BE2} - V_{BE3}}{R}$$

$$I_{C2} \approx \frac{A_3}{A_1} I_{ref}$$



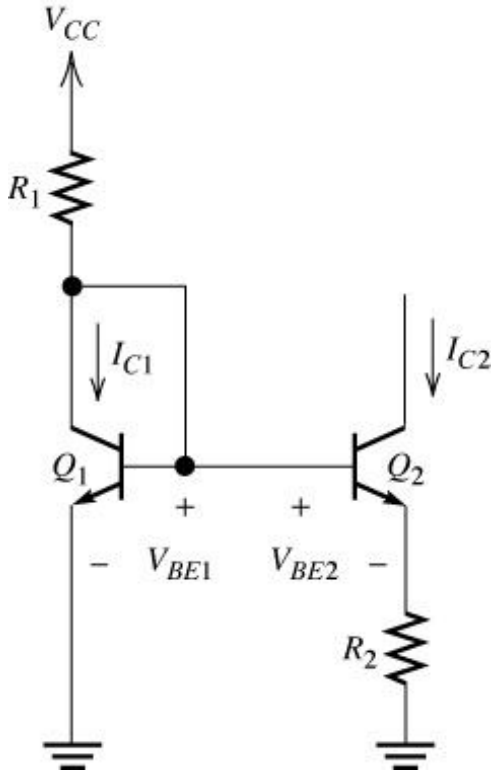
# The Widlar current source

When the desired current is small, the Widlar current source may be a better alternative, as shown in the Figure.

For Widlar current source,

$$R_2 \approx \frac{V_T}{I_{C2}} \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

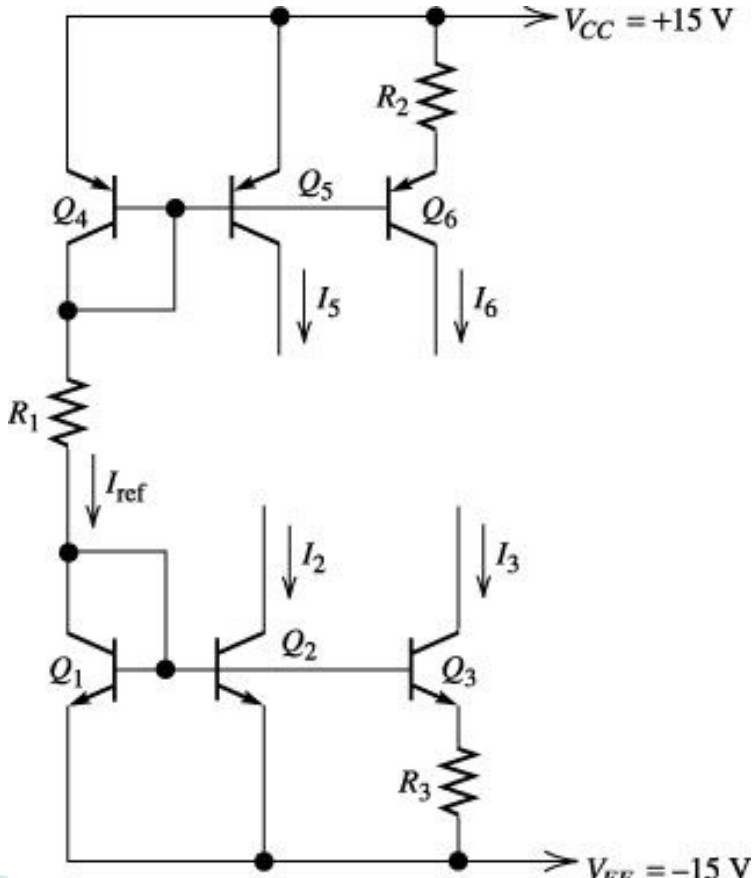
$$I_{C1} \approx I_{ref} = \frac{V_{CC} - V_{BE1}}{R_1}$$



# The combined current sources

In an Integrated Circuit amplifier, several current sources use the same reference current, as shown below.

The current through R1 is the reference current for all four current sources. Q1, Q2 forms a current mirror, and Q1, Q3 forms a Widlar source. Notice the pnp current source by Q4, Q5 and Q6.



# Voltage Reference Circuits

- Used to provide a constant d.c voltage, which acts as a reference for other circuits
- It is independent of changes in the parameters like temperature, input line voltage and load current

- Accuracy and stability with temperature are the basic characteristics of any voltage reference circuit

- Temperature coefficient TC = $\Delta Vo/\Delta T$ in $mV/^0C$
- % of temperature coefficient

$$\%TC = 100\left[\frac{\Delta Vo/Vo}{\Delta T}\right] \quad \text{in } \%/^0C$$

# Performance parameters of Voltage reference circuits

- **Line regulation** (Input/Supply regulation)

$$\text{Line Regulation} = \frac{\Delta v_o}{\Delta v_i}$$

- **Load regulation**

$$\text{Load Regulation} = \frac{\Delta v_o}{\Delta I_L}$$

- **Long term stability**

The ability of circuit to maintain the output voltage constant with respect to time

- **Ripple Rejection Ratio (RRR)**

$$\text{RRR} = 20 \log \frac{v_{ri}}{v_{ro}}$$

# Problems

- Design an amplifier with a gain of -10 and input resistance equal to 10KΩ
- For an op-amp with $R_1$=10KΩ and $R_2$=100KΩ is given $v_i$=1V. A load 25KΩ is connected to the terminal. Calculate $i_1$,$V_o$,$i_L$ and total current $i_o$ into the output pin.
- Design an amplifier with a gain of +5 using op-amp.
- For an op-amp circuit, $R_1$=5kΩ and $R_f$=20kΩ with $v_i$=1V. A load resistor of 5kΩ is connected at the output. Calculate $V_o$, $A_{CL}$ ,$i_L$ and $i_o$.