Analog to Digital & Digital to Analog converters

UNIT–IV

Analog Signals

Analog signals – directly measurable quantities in terms of some other quantity

Examples:

- Thermometer – mercury height rises as temperature rises
- Car Speedometer – Needle moves farther right as you accelerate
- Stereo – Volume increases as you turn the knob.

Digital Signals

Digital Signals – have only two states. For digital computers, we refer to binary states, 0 and 1. “1” can be on, “0” can be off.

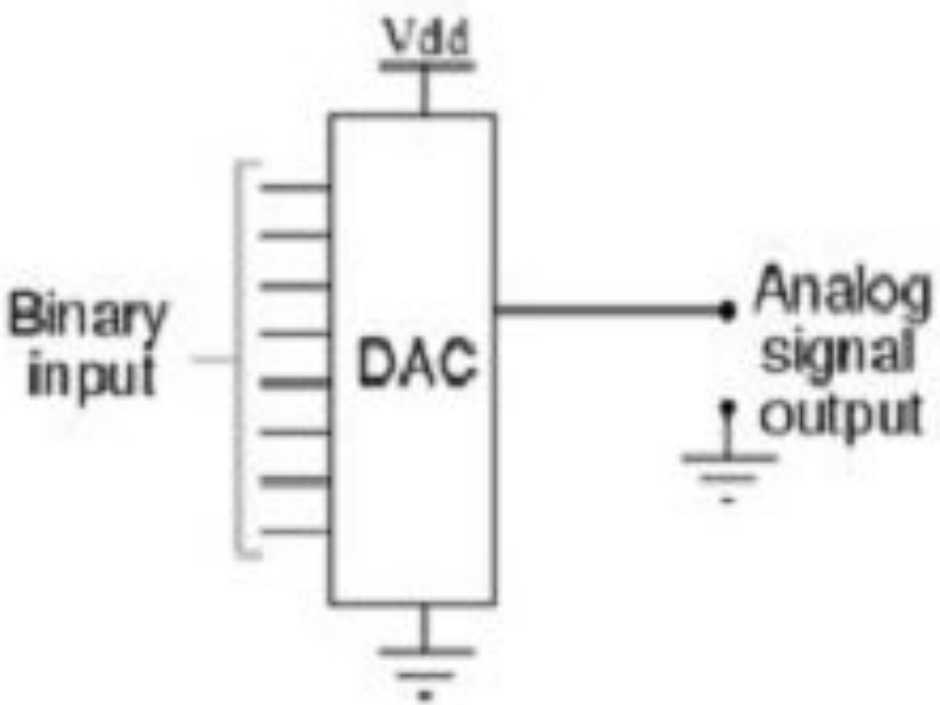
Examples:

- Light switch can be either on or off
- Door to a room is either open or closed

Examples of A/D Applications

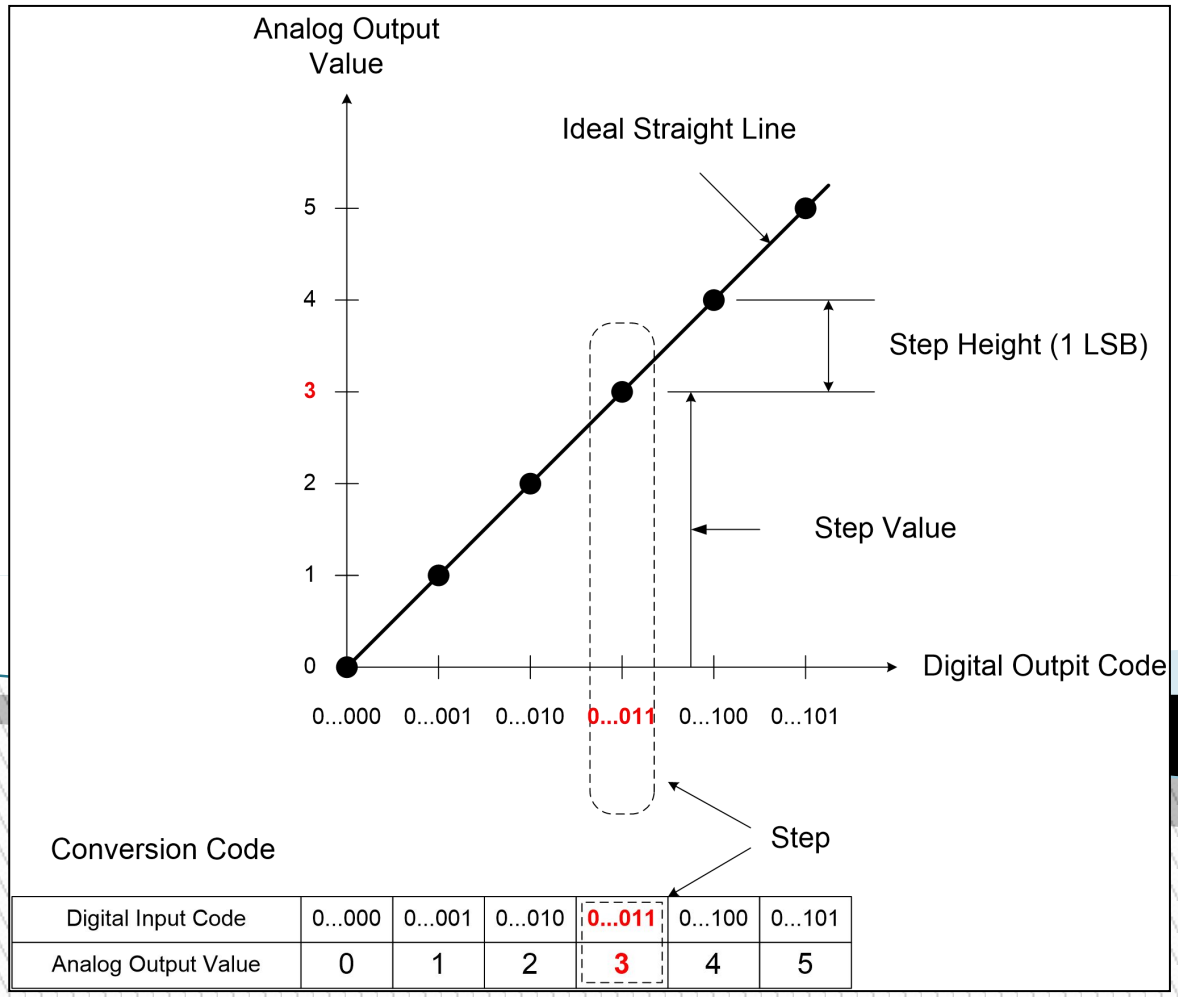
- Microphones – take your voice varying pressure waves in the air and convert them into varying electrical signals
- Strain Gages – determines the amount of strain (change in dimensions) when a stress is applied
- Thermocouple – temperature measuring device converts thermal energy to electric energy
- Voltmeters
- Digital Multimeters

D/A converter (DAC)



The Ideal Transfer Function (DAC)

The DAC theoretical ideal transfer function would also be a straight line with an infinite number of steps but practically it is a series of points that fall on the ideal straight line as shown in Figure



Conversion Code

Digital Input Code	0...000	0...001	0...010	0...011	0...100	0...101
Analog Output Value	0	1	2	3	4	5

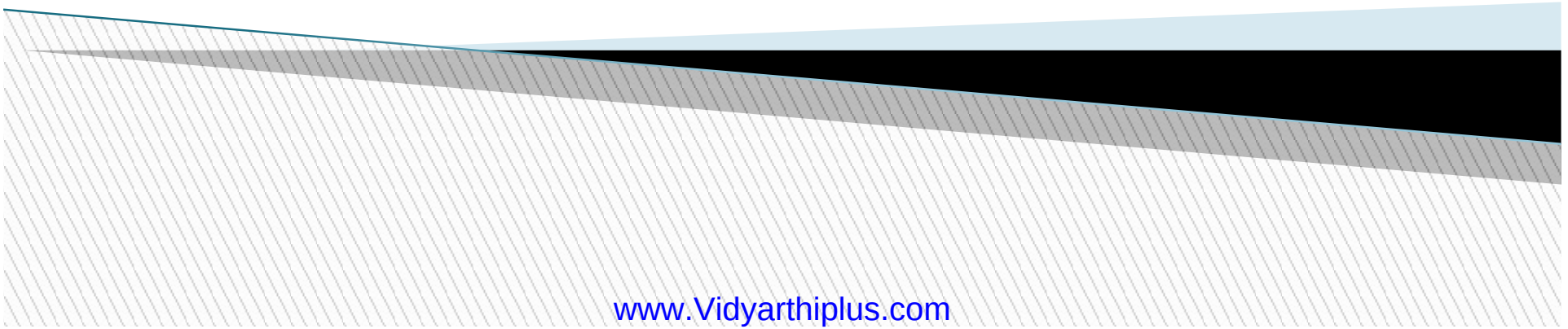
Specifications of DAC

Static errors, that is those errors that affect the accuracy of the converter when it is converting static (dc) signals, can be completely described by just four terms.

These are :

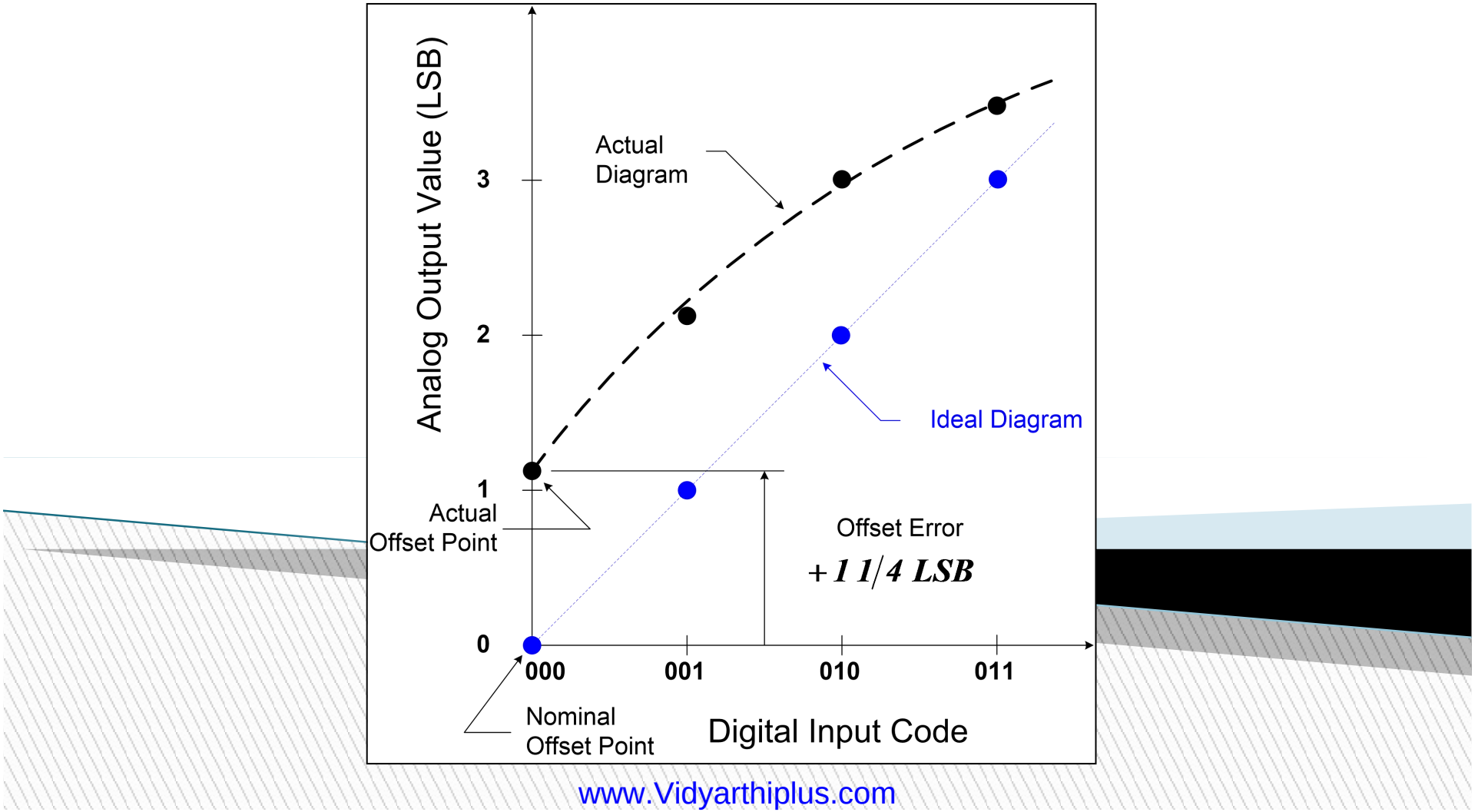
- **offset error,**
- **gain error,**
- **integral nonlinearity and**
- **differential nonlinearity.**

Each can be expressed in LSB units or sometimes as a percentage of the FSR



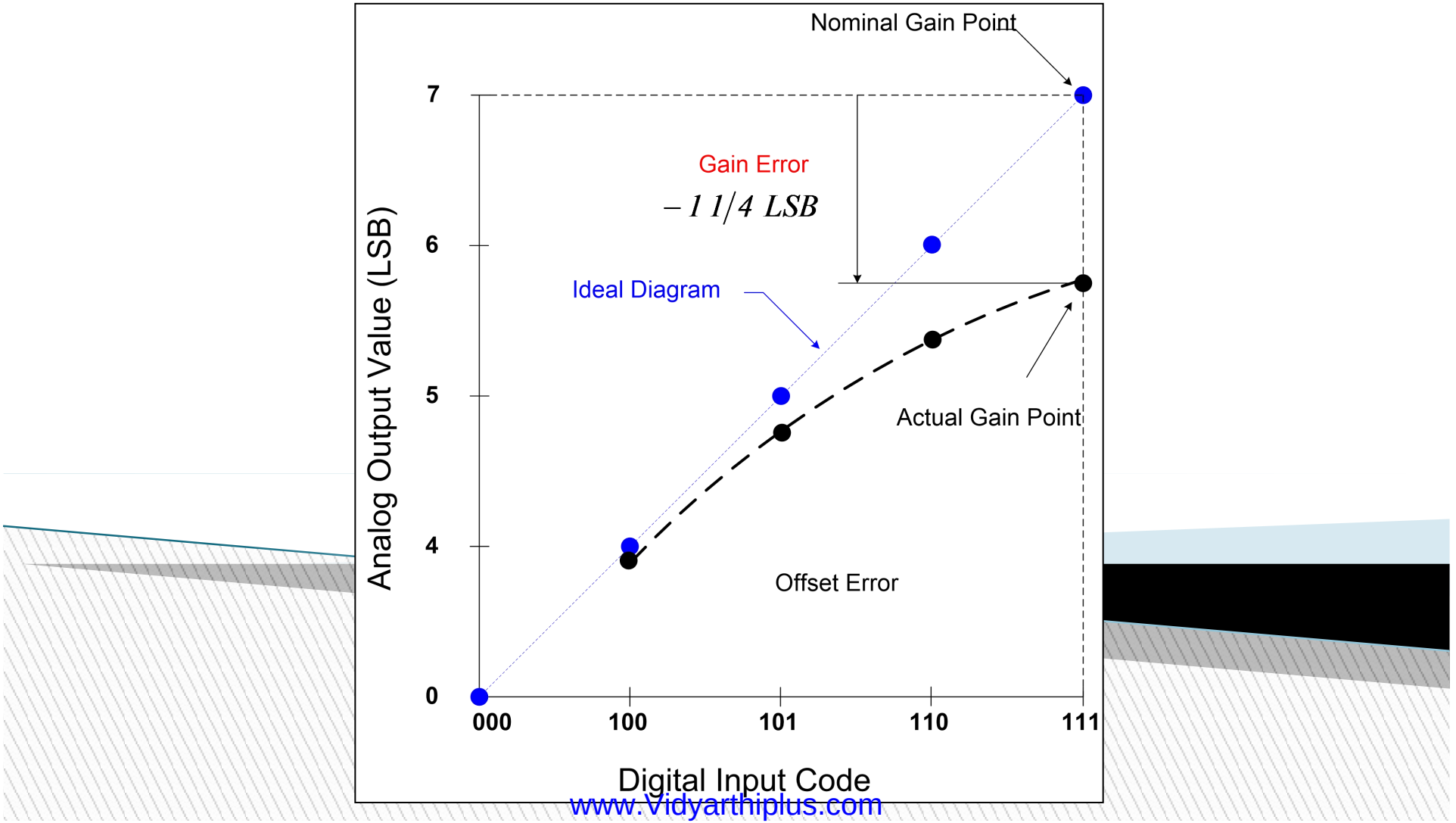
Offset Error – DAC

For a DAC it is the step value when the digital input is zero. This error affects all codes by the same amount and can usually be compensated for by a **trimming process**. If trimming is not possible, this error is referred to as the **zero-scale error**.



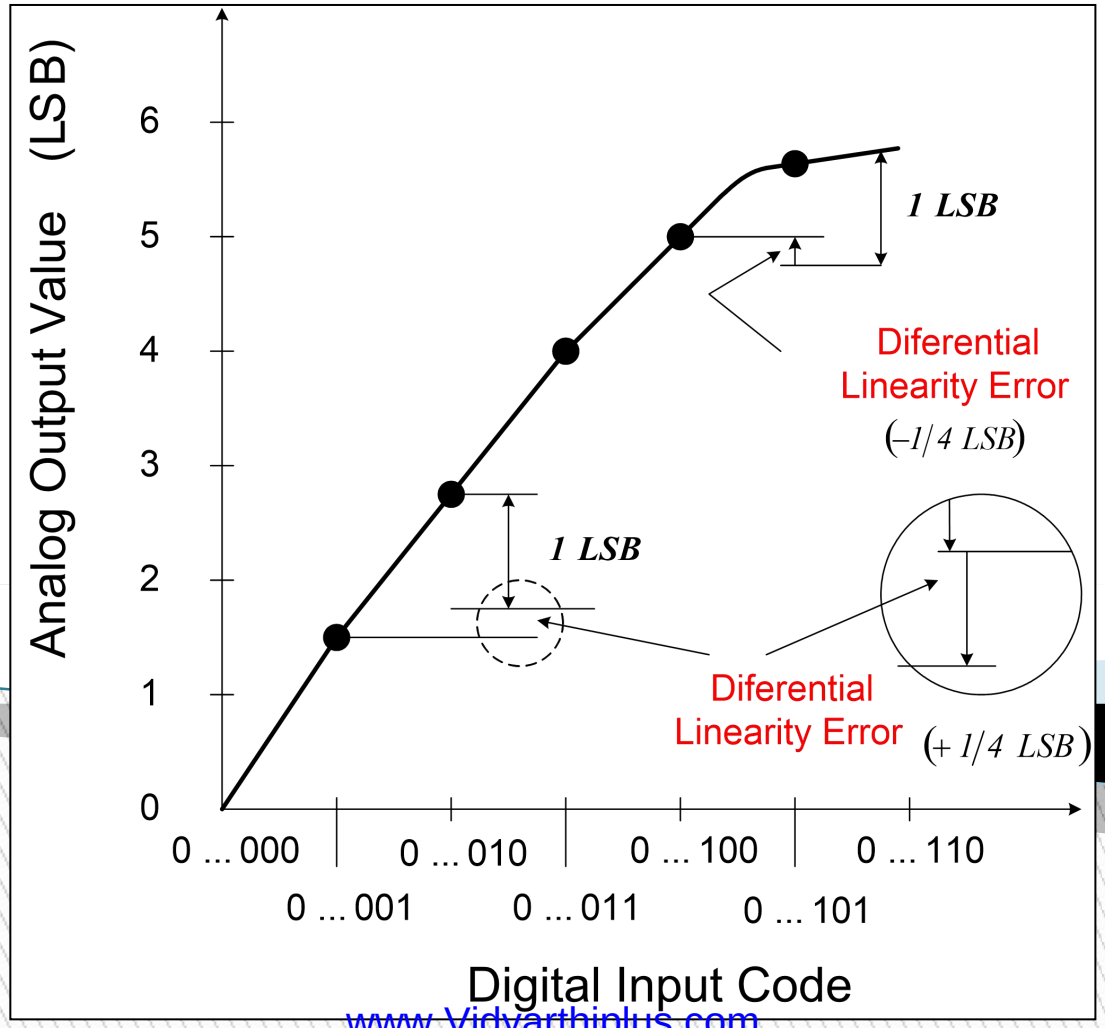
Gain Error – DAC

For a DAC it is the step value when the digital input is full scale. **This error represents a difference in the slope of the actual and ideal transfer functions** This error can also usually be adjusted to zero by trimming.



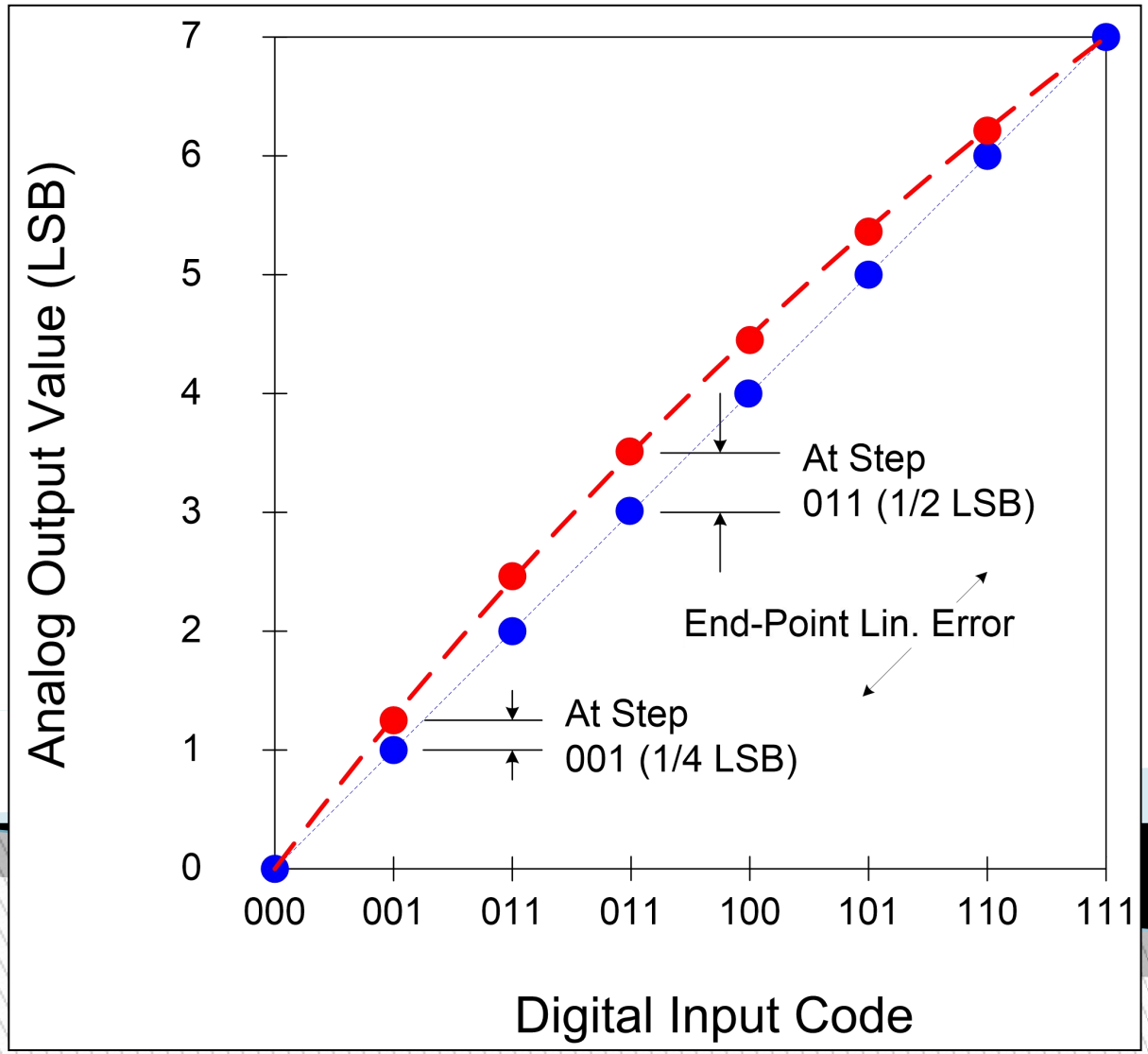
Differential Nonlinearity (DNL) Error – DAC

The differential nonlinearity error shown in Figure is the **difference between an actual step height (for a DAC) and the ideal value of 1 LSB**. Therefore if the step height is exactly 1 LSB, then the differential nonlinearity error is zero

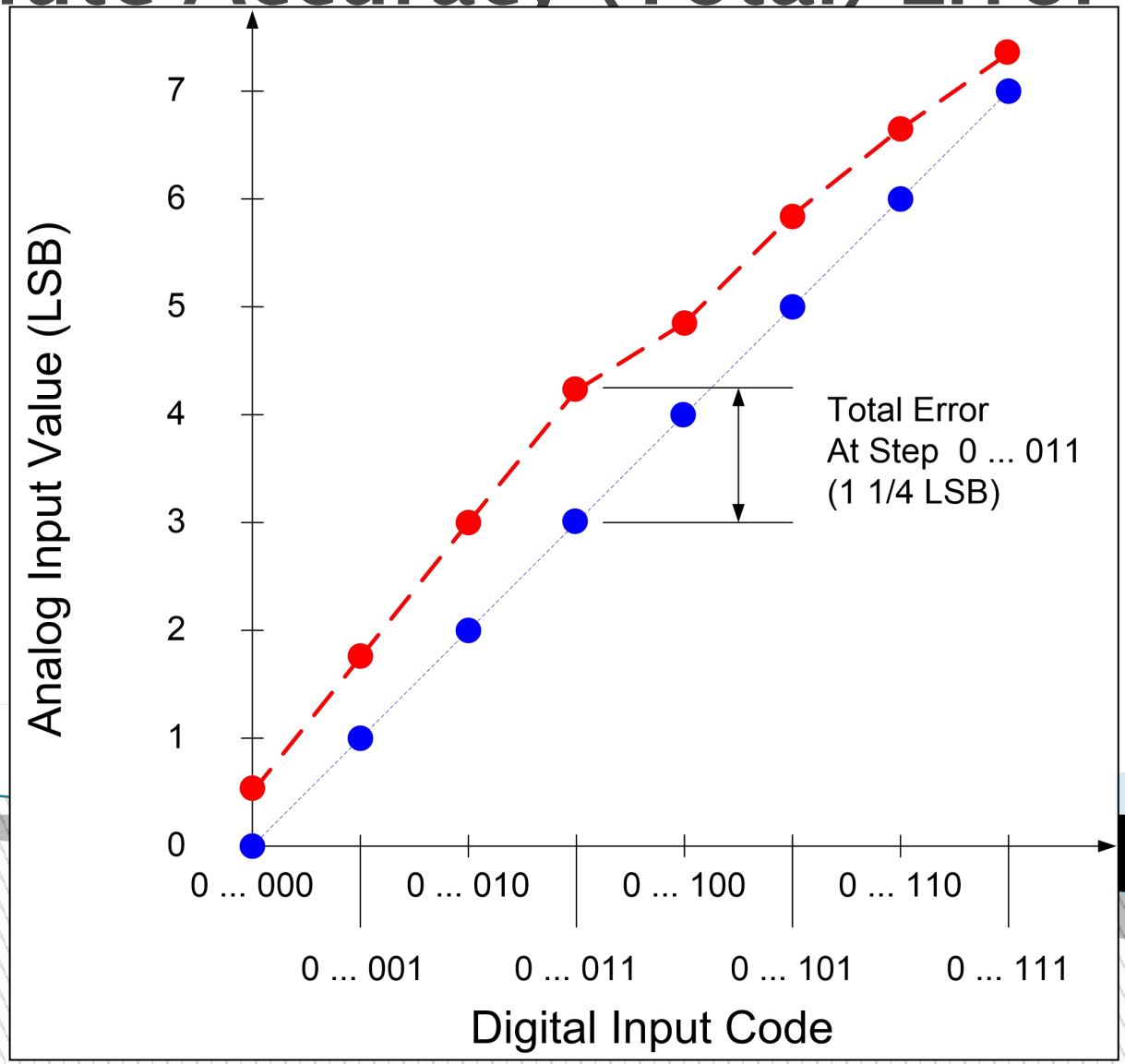


Integral Nonlinerity (INL) Error – DAC

The name integral nonlinearity derives from the fact that the summation of the differential nonlinearities from the bottom up to a particular step, determines the value of the integral nonlinearity at that step.



Absolute Accuracy (Total) Error –DAC–



Resolution:

Resolution is defined as the number of different analog output voltage levels that can be provided by a DAC. Or alternatively resolution is defined as the ratio of a change in output voltage resulting for a change of 1 LSB at the digital input. Simply, resolution is the value of LSB.

Resolution (Volts) = $Vo_{FS} / (2^n - 1)$ = 1 LSB increment

Where 'n' is the number of input bits

'Vo_{FS}' is the full scale output voltage.

Example:

Resolution for an 8 – bit DAC for example is said to have

: 8 – bit resolution

: A resolution of 0.392 of full-Scale (1/255)

: A resolution of 1 part in 255.

Thus resolution can be defined in many different ways.

The following table shows the resolution for 6 to 16 bit DACs

S.No.	Bits	Intervals	LSB size (% of full-scale)	LSB size (For a 10 V full-scale)
1.	6	63	1.588	158.8 mV
2.	8	255	0.392	39.2 mV
3.	10	1023	0.0978	9.78 mV
4.	12	4095	0.0244	2.44 mV
5.	14	16383	0.0061	0.61 mV
6.	16	65535	0.0015	0.15 mV

Accuracy

Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output. The ideal converter is the one which does not suffer from any problem. Whereas, the actual converter output deviates due to the drift in component values, mismatches, aging, noise and other sources of errors.

The relative accuracy is the maximum deviation after the gain and offset errors have been removed. Accuracy is also given in terms of LSB increments or percentage of full-scale voltage. Normally, the data sheet of a D/A converter specifies the relative accuracy rather than absolute accuracy.

Linearity

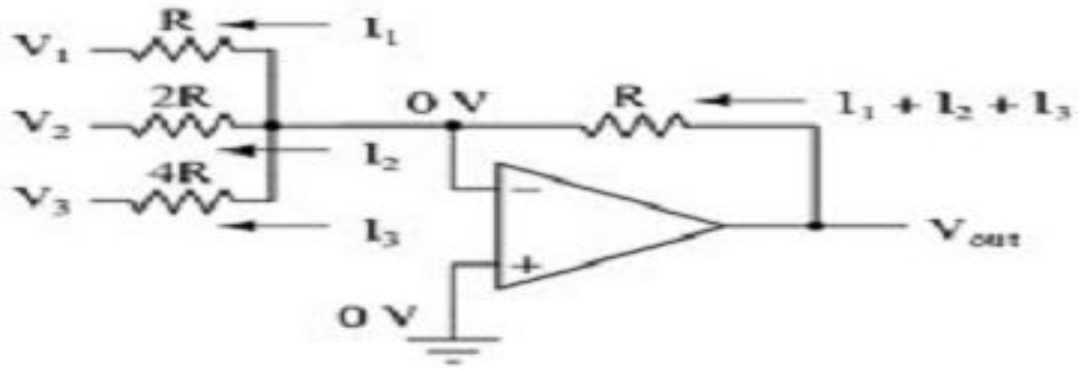
Linearity error is the maximum deviation in step size from the ideal step size. Some D/A converters are having a linearity error as low as 0.001% of full scale. The linearity of a D/A converter is defined as the precision or exactness with which the digital input is converted into analog output. An ideal D/A converter produces equal increments or step sizes at output for every change in equal increments of binary input.

Monotonicity

A Digital to Analog converter is said to be monotonic if the analog output increases for an increase in the digital input. A monotonic characteristics is essential in control applications. Otherwise it would lead to oscillations. If a DAC has to be monotonic, the error should be less than ± (1/2) LSB at each output level. Hence all the D/A converters are designed such that the linearity error satisfies the above condition.

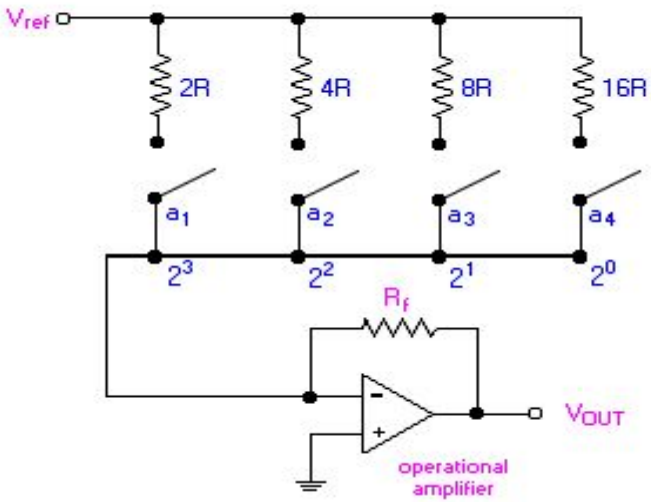
When a D/A Converter doesn't satisfy the condition described above, then, the output voltage may decrease for an increase in the binary input.

Binary weighted Resistor DAC



$$V_{out} = -\left(V_1 + \frac{V_2}{2} + \frac{V_3}{4}\right)$$

4-bit Binary weighted Resistor DAC



$$V_{OUT} = -iR_f$$

$$= -\left[V_{ref}\left(\frac{a_1}{2R}+\frac{a_2}{4R}+\frac{a_3}{8R}+\frac{a_4}{16R}\right)\right]R_f$$

$$= -\frac{V_{ref}R_f}{R}\left(\frac{a_1}{2}+\frac{a_2}{4}+\frac{a_3}{8}+\frac{a_4}{16}\right)$$

$$= -\frac{V_{ref}R_f}{R}\left(\frac{a_1}{2^1}+\frac{a_2}{2^2}+\frac{a_3}{2^3}+\frac{a_4}{2^4}\right)$$

Binary weighted Resistor DAC

For a n-bit DAC, the relationship between V_{out} and the binary input is as follows:

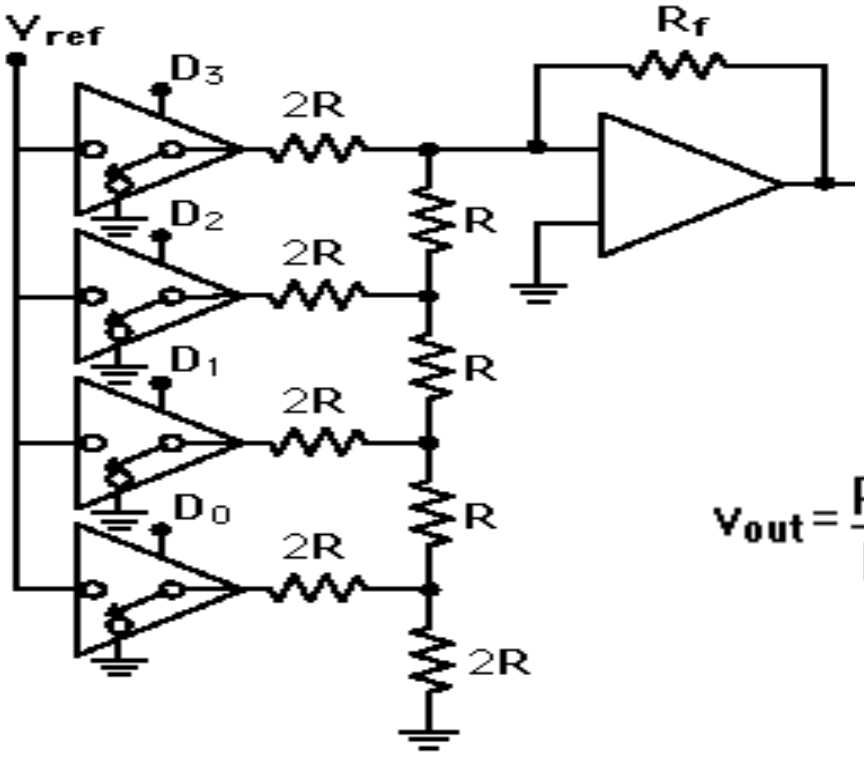
$$V_{OUT} = -\frac{V_{ref} R_f}{R} \sum_{i=1}^{n} \frac{a_i}{2^i}$$

Digital Input				V_{OUT} (Volts)
a_1	a_2	a_3	a_4	
0	0	0	0	0
0	0	0	1	- 0.625
0	0	1	0	- 1.250
0	0	1	1	- 1.875
0	1	0	0	- 2.500
0	1	0	1	- 3.125
0	1	1	0	- 3.750
0	1	1	1	- 4.375
1	0	0	0	- 5.000
1	0	0	1	- 5.625
1	0	1	0	- 6.250
1	0	1	1	- 6.875
1	1	0	0	- 7.500
1	1	0	1	- 8.125
1	1	1	0	- 8.750
1	1	1	1	- 9.375

Weighted Sum DAC

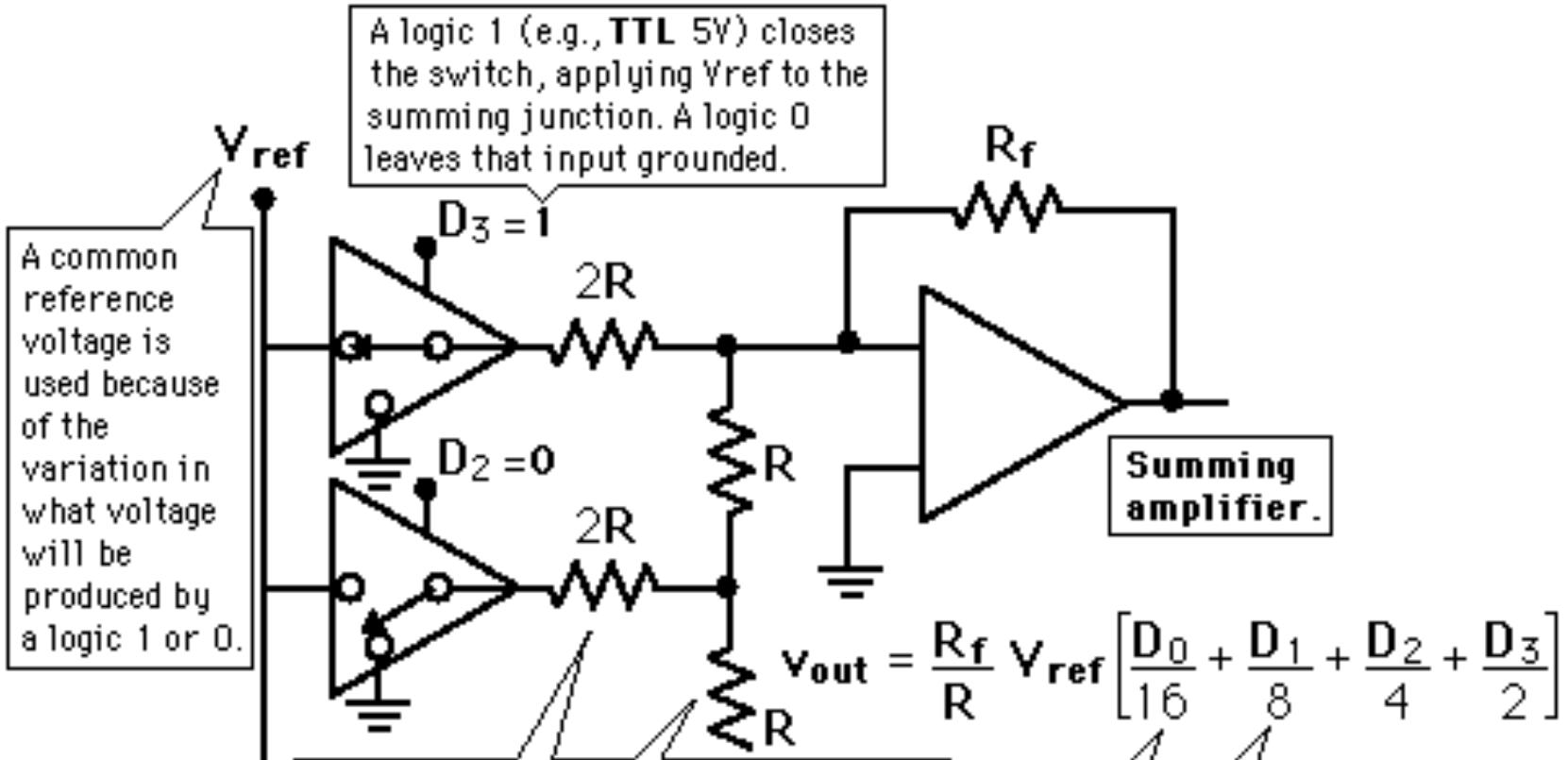
- One way to achieve D/A conversion is to use a summing amplifier.
- This approach is not satisfactory for a large number of bits because it requires too much precision in the summing resistors.
- This problem is overcome in the R-2R network DAC.

R-2R Ladder type DAC



$$V_{out} = \frac{R_f}{R} V_{ref} \left[\frac{D_0}{16} + \frac{D_1}{8} + \frac{D_2}{4} + \frac{D_3}{2} \right]$$

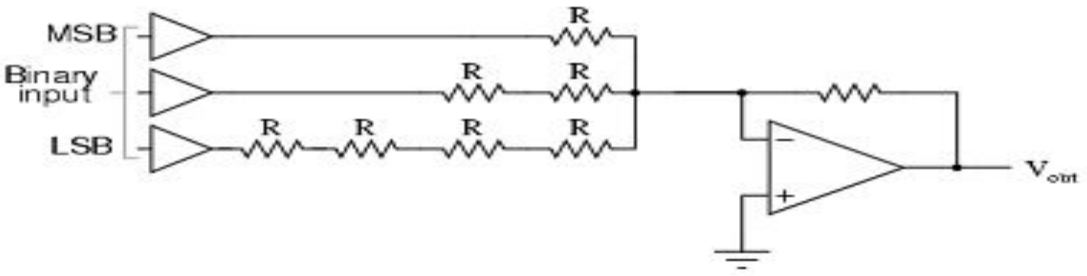
R–2R Ladder DAC

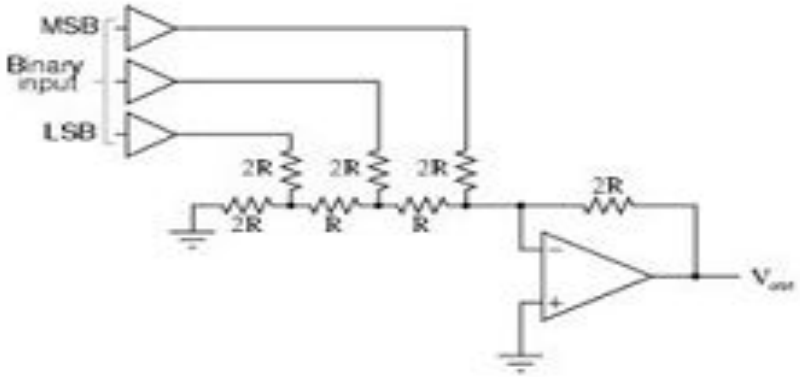


R-2R Ladder DAC

- The summing amplifier with the R-2R ladder of resistances shown produces the output where the D's take the value 0 or 1.
- The digital inputs could be TTL voltages which close the switches on a logical 1 and leave it grounded for a logical 0.
- This is illustrated for 4 bits, but can be extended to any number with just the resistance values R and 2R.

R–2R Ladder DAC



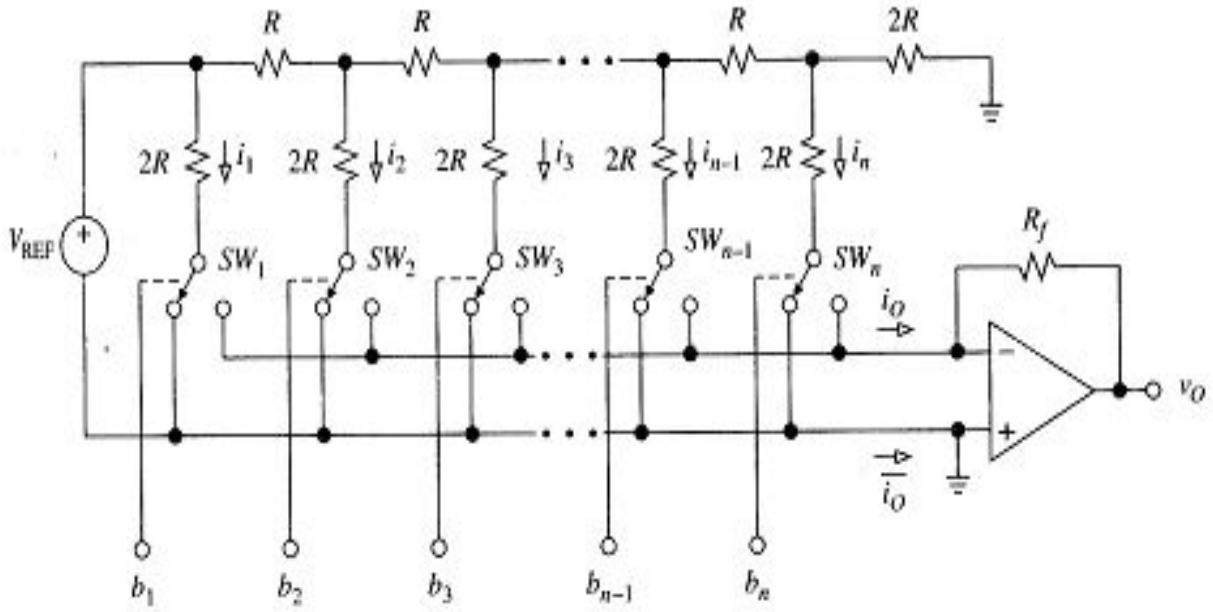


$$V_{out} = -(V_{MSB} + V_n + V_{LSB}) = -(V_{Ref} + V_{Ref}/2 + V_{Ref}/4)$$

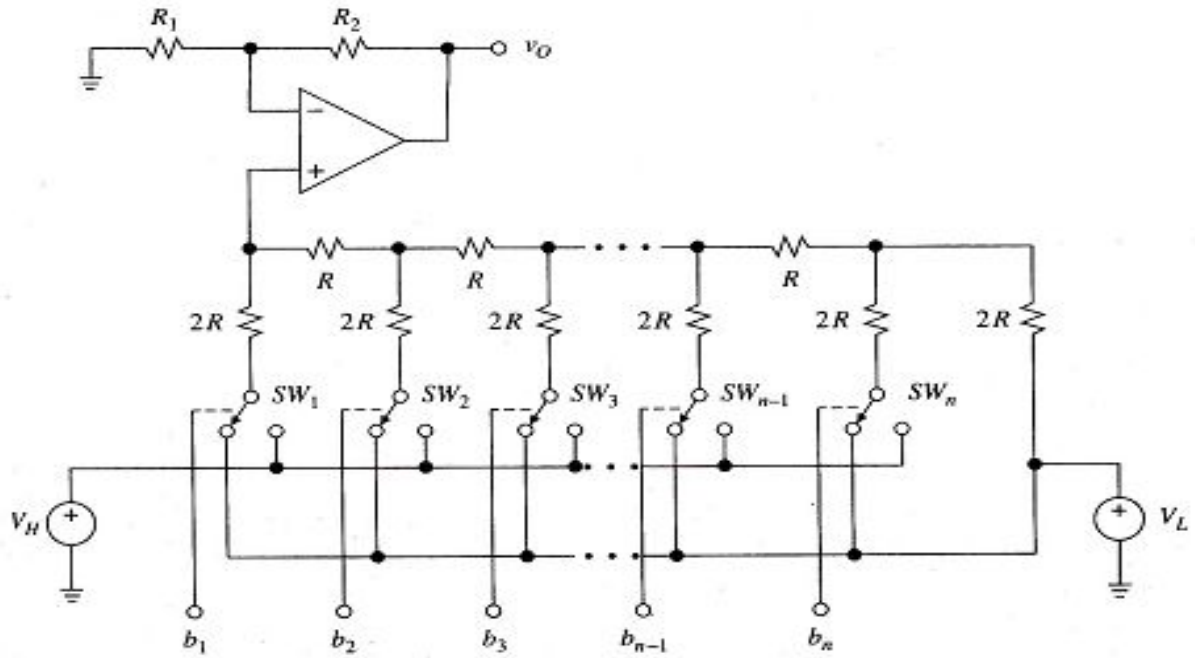
R-2R Ladder DAC

Binary	Output voltage
000	0.00 V
001	-1.25 V
010	-2.50 V
011	-3.75 V
100	-5.00 V
101	-6.25 V
110	-7.50 V
111	-8.75 V

Inverted or Current Mode DAC



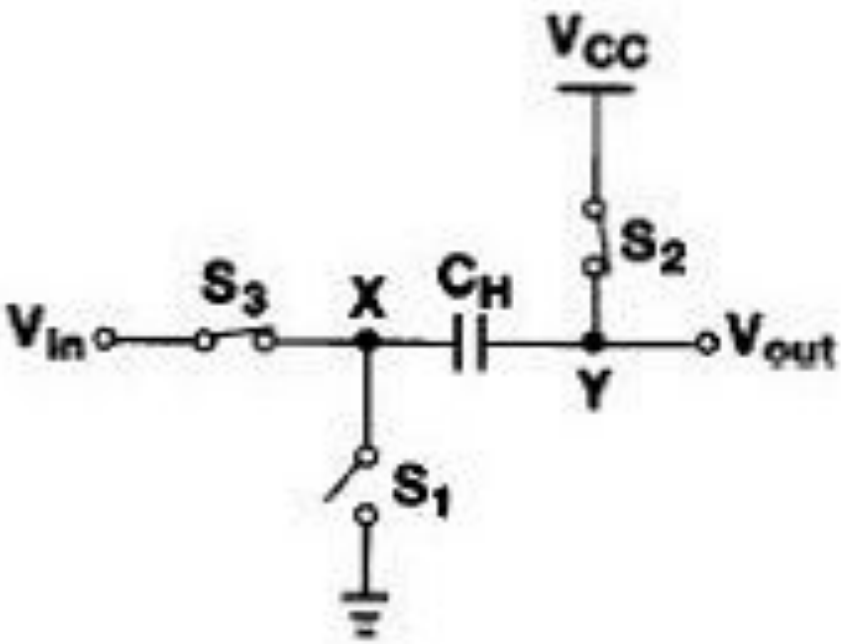
Voltage Mode DAC



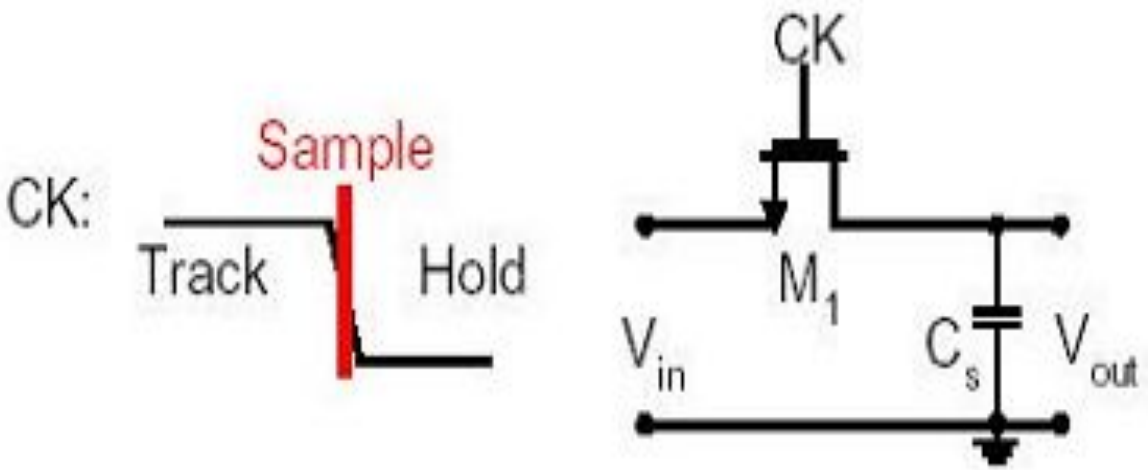
Switches for DAC

- Switches using Over-driven Emitter Followers
- Switches using MOS Transistor-Totem Pole MOSFET switch and CMOS Inverter Switch
- CMOS Switch for Multiplying type DACs
- CMOS Transmission gate switches

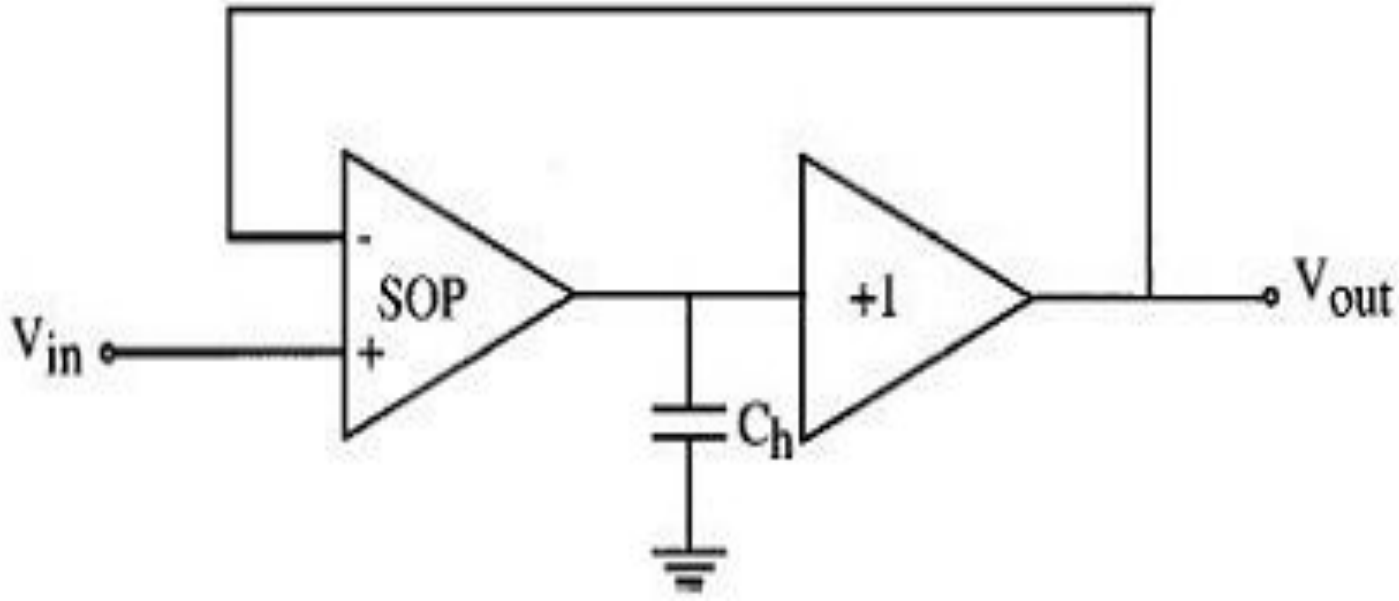
Series Sampling



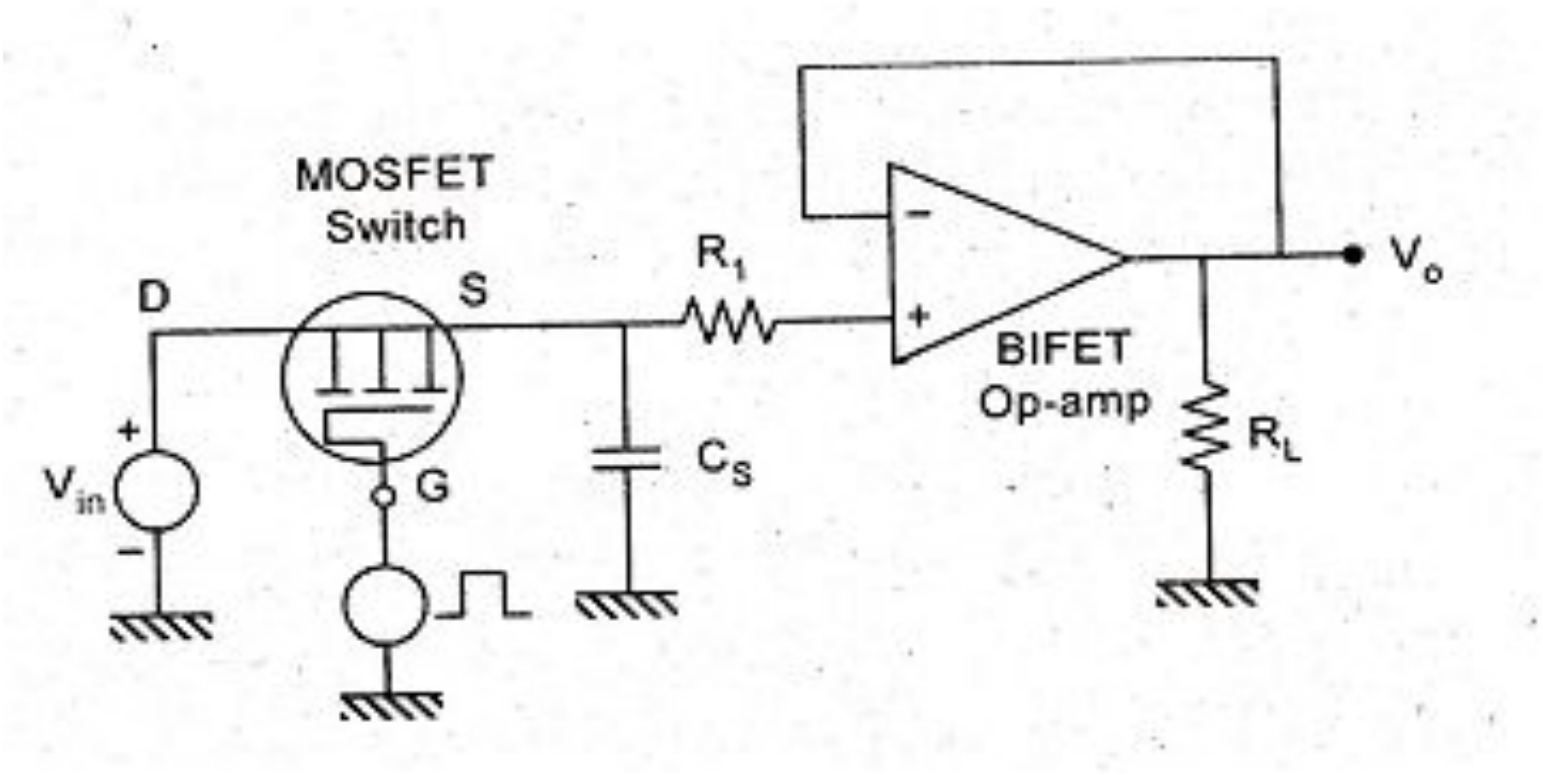
High Speed Sample & Hold circuit



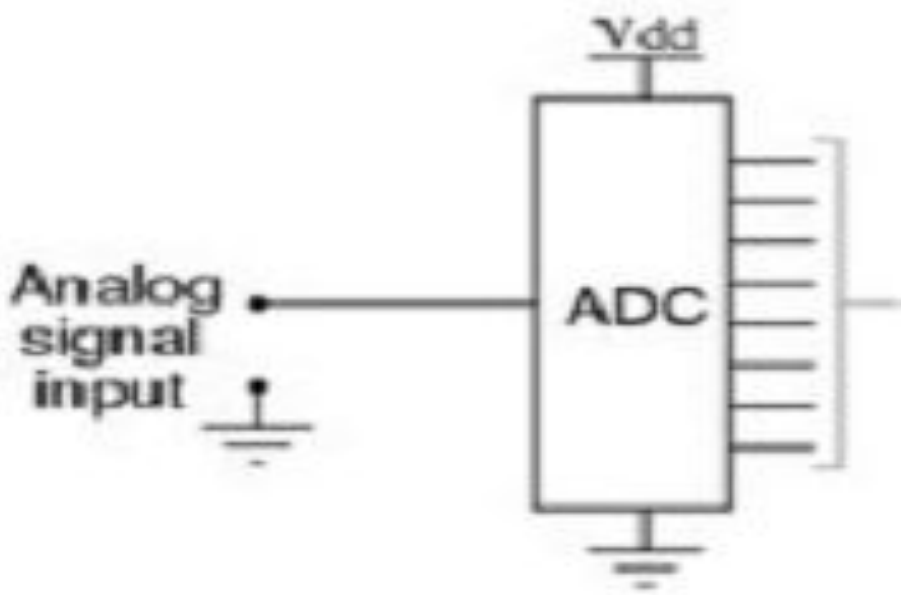
Switched op-amp based Sample and Hold Circuit



Sample and Hold circuit with MOSFET as a switch

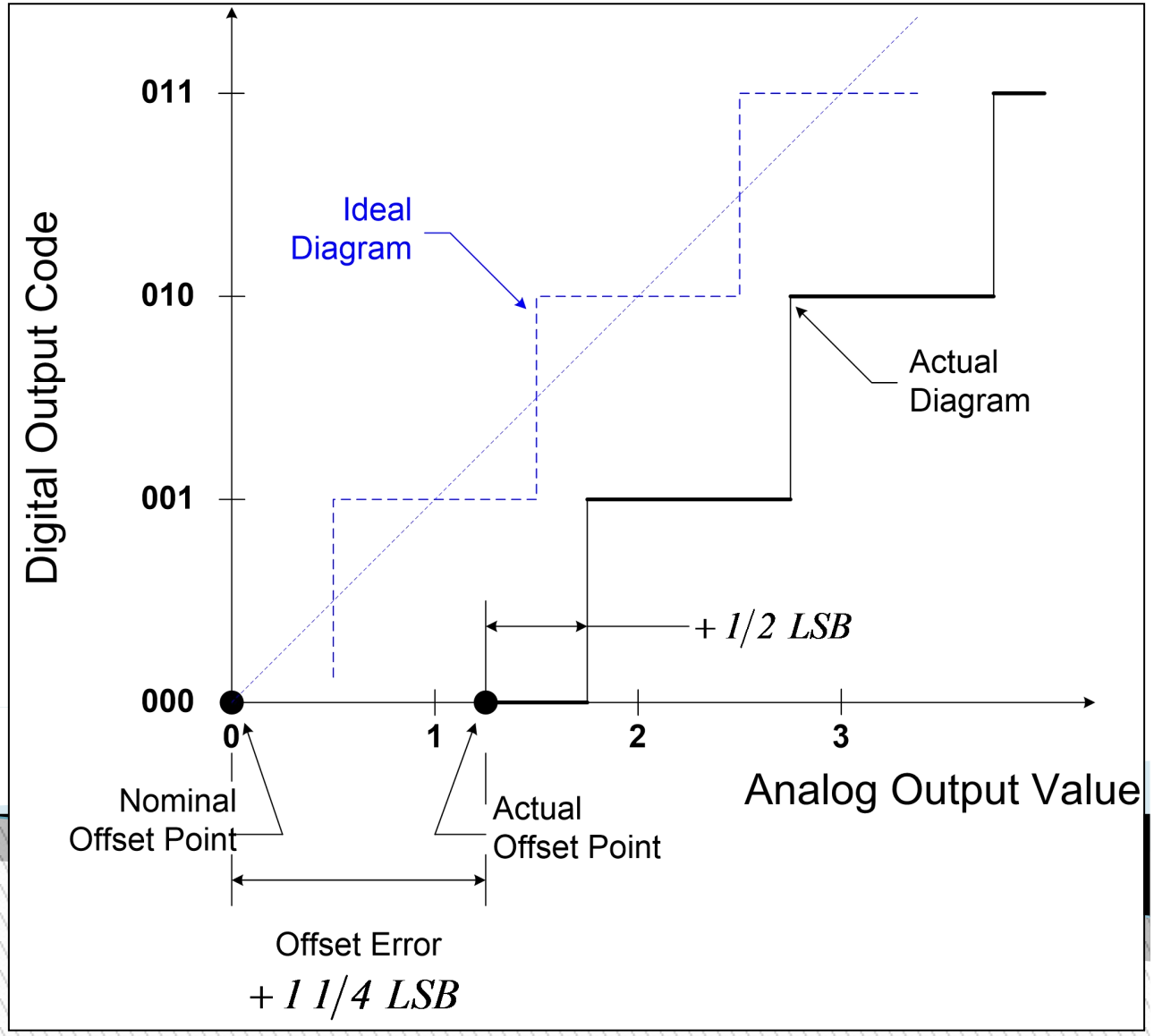


Analog to Digital Converters



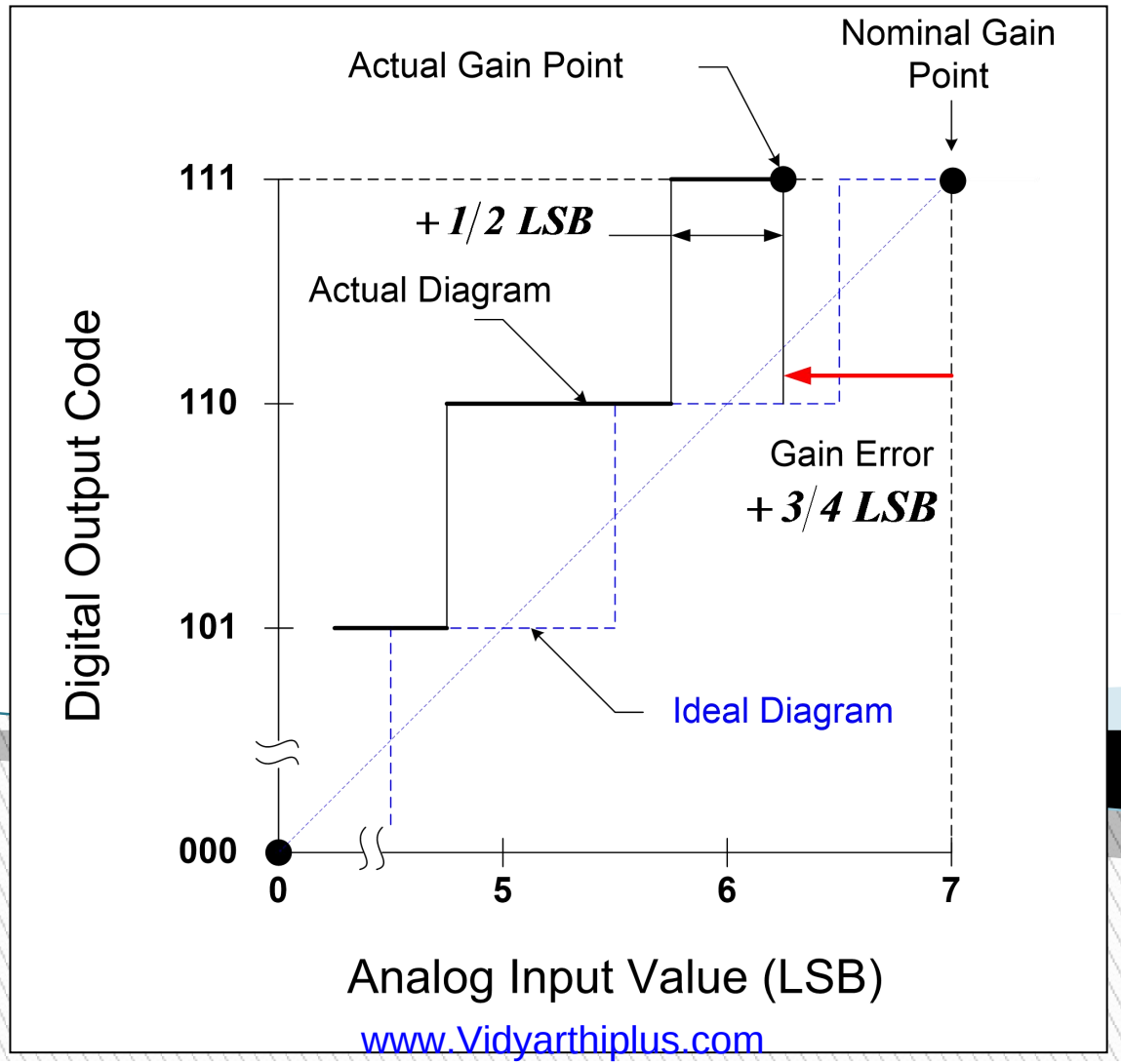
Offset Error – ADC

The offset error is efined as the difference between the nominal and actual offset points.



Gain Error – ADC

The gain error is defined as the difference between the nominal and actual gain points on the transfer function after the offset error has been corrected to zero. For an ADC, the gain point is the midstep value when the digital output is full scale,

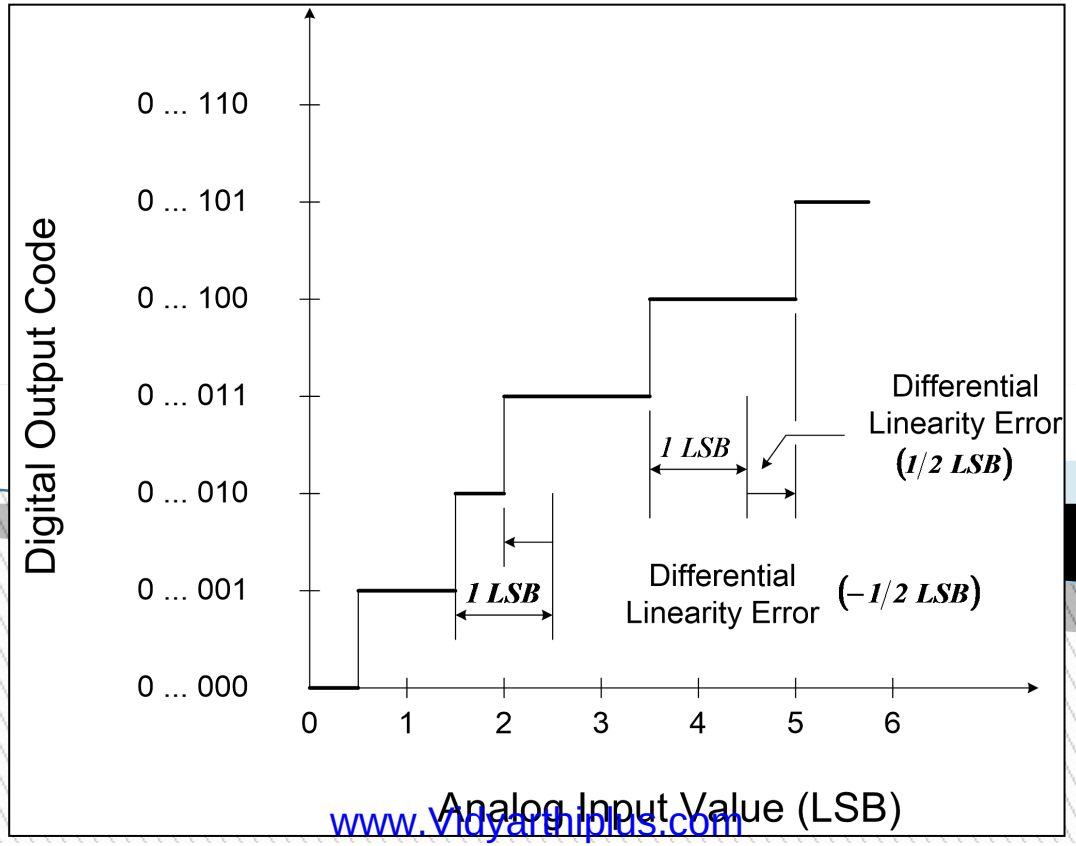


Differential Nonlinearity (DNL) Error – ADC

DNL is the **difference between an actual step width** (for an ADC) **and the ideal value of 1 LSB**. Therefore if the step width is exactly 1 LSB, then the differential nonlinearity error is zero.

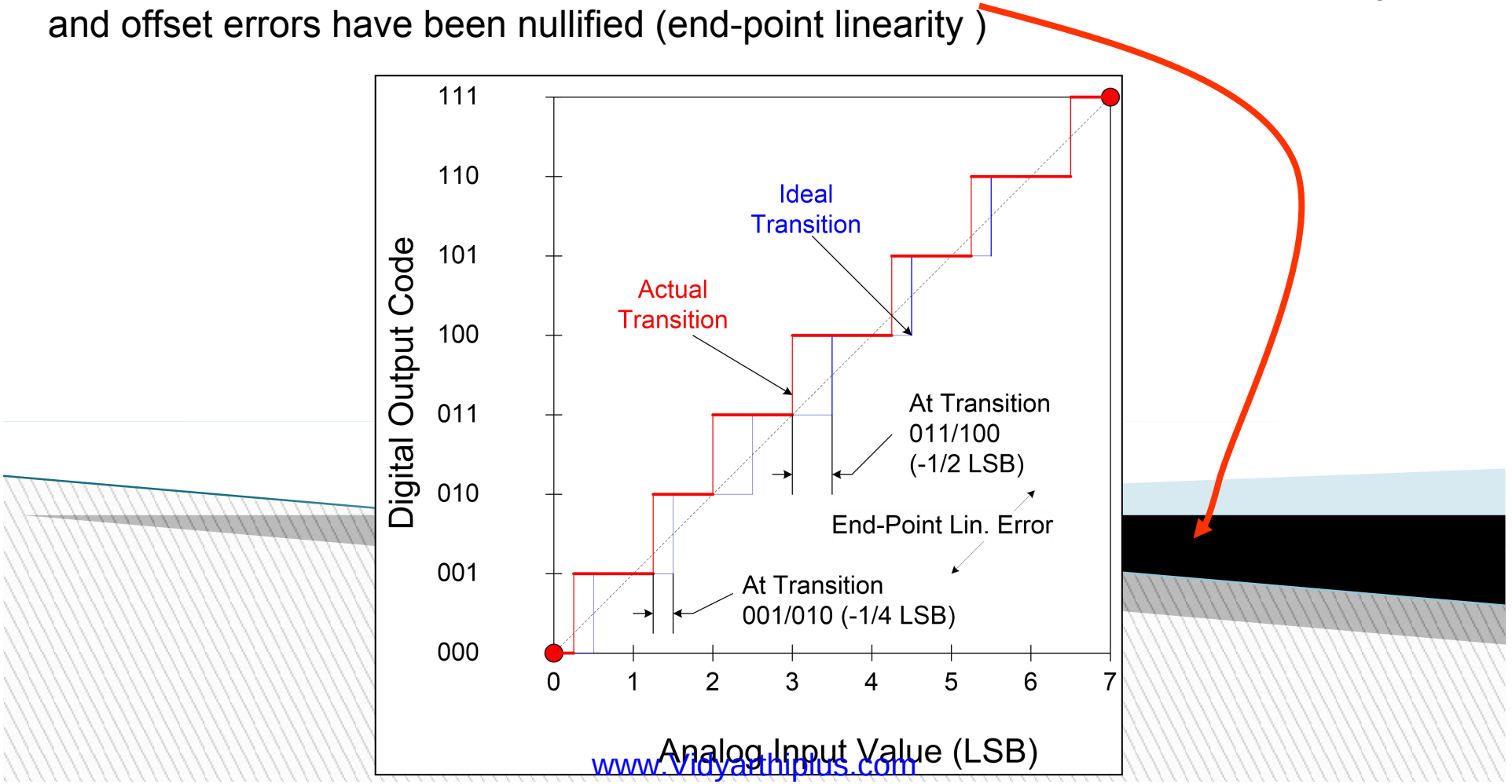
If the DNL exceeds 1 LSB $\Rightarrow$ **nonmonotonic** (this means that the magnitude of the output gets smaller for an increase in the magnitude of the input)

If the DNL error of – 1 LSB there is also a possibility that there can be **missing codes** i.e., one or more of the possible 2n binary codes are never output.



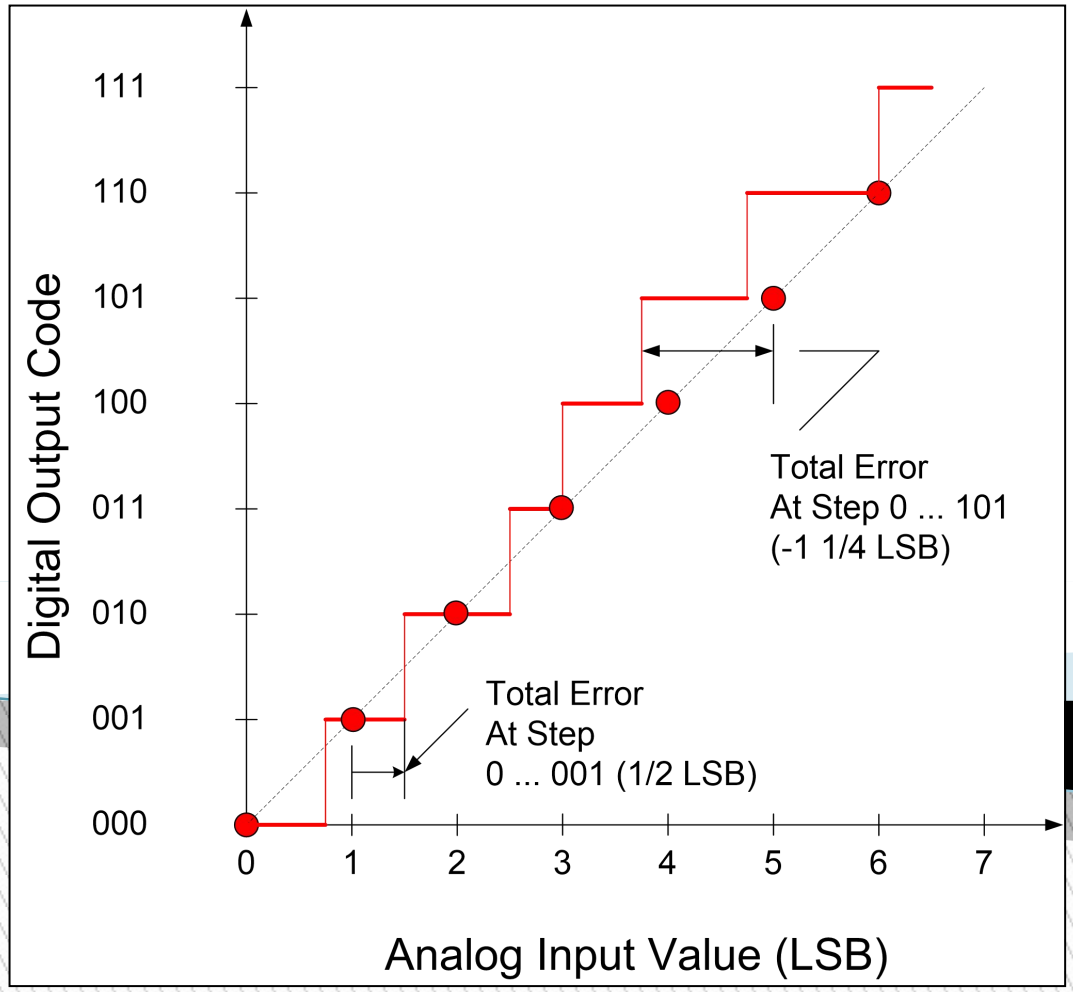
Integral Nonlinerity (INL) Error – ADC

The integral nonlinearity error shown in Figure is **the deviation of the values on the actual transfer function from a straight line**.
This straight line can be either a **best straight line** which is drawn so as to minimize these deviations or
it can be a line drawn between **the end points** of the transfer function once the gain and offset errors have been nullified (end-point linearity)



Absolute Accuracy (Total) Error –ADC

The absolute accuracy or total error of an ADC as shown in Figure is the maximum value of the difference between an analog value and the ideal midstep value.
It includes offset, gain, and integral linearity errors and also the quantization error in the case of an ADC



Resolution

The resolution refers to the finest minimum change in the signal which is accepted for conversion, and it is decided with respect to number of bits. It is given as $1/2^n$, where 'n' is the number of bits in the digital output word. As it is clear, that the resolution can be improved by increasing the number of bits or the number of bits representing the given analog input voltage.

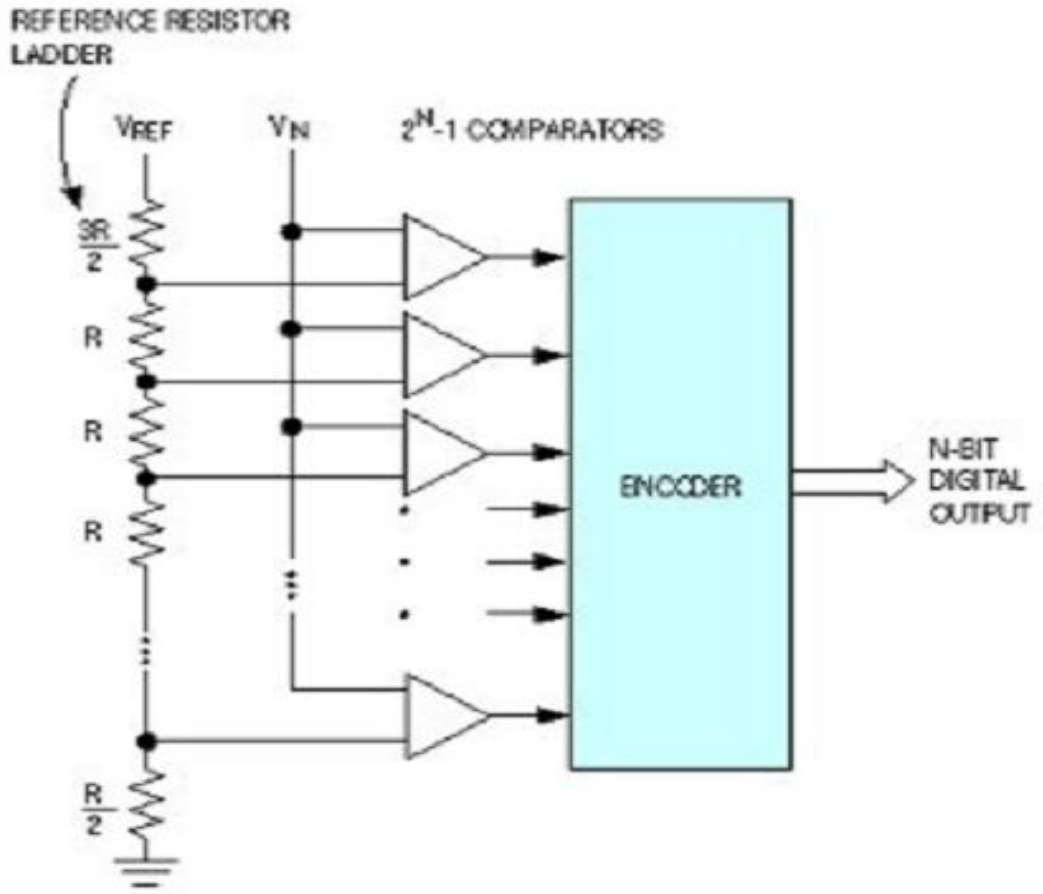
Resolution can also be defined as the ratio of change in the value of input voltage V_i, needed to change the digital output by 1 LSB. It is given as

$$\text{Resolution} = V_{iFS} / (2^n - 1)$$

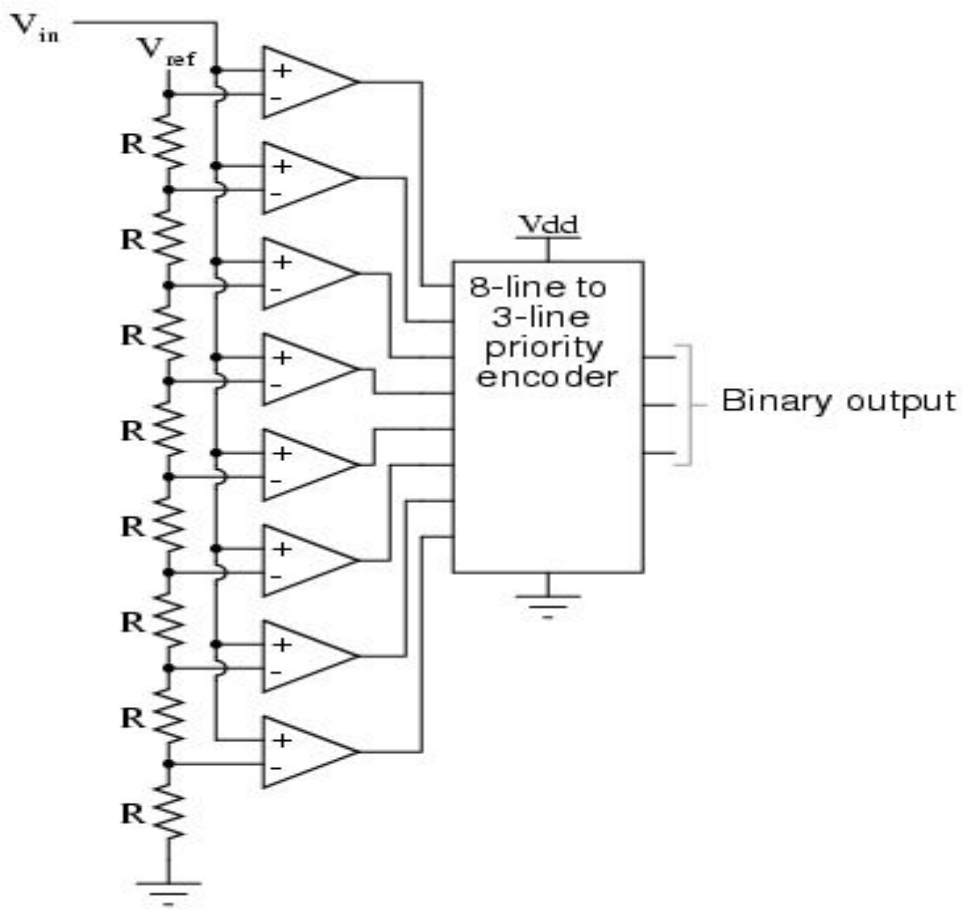
Where 'V_{iFS}' is the full-scale input voltage.

'n' is the number of output bits.

Flash type ADC



Flash ADC Circuit



Flash ADC Circuit

Advantages

- Simplest in terms of operational theory
- Most efficient in terms of speed, very fast
  - limited only in terms of comparator and gate propagation delays

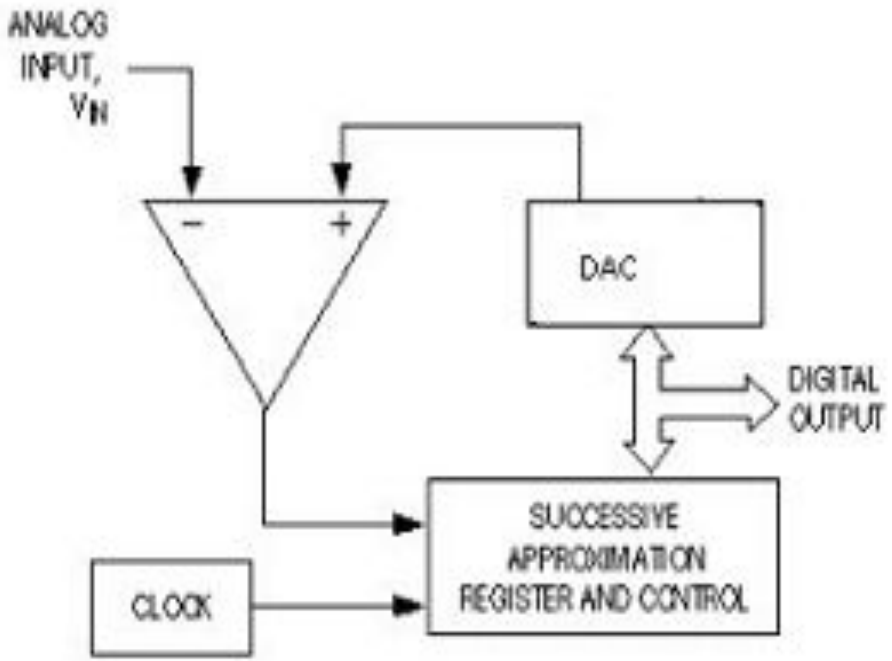
Disadvantages

- Lower resolution
- Expensive
- For each additional output bit, the number of comparators is doubled
  - i.e. for 8 bits, 256 comparators needed

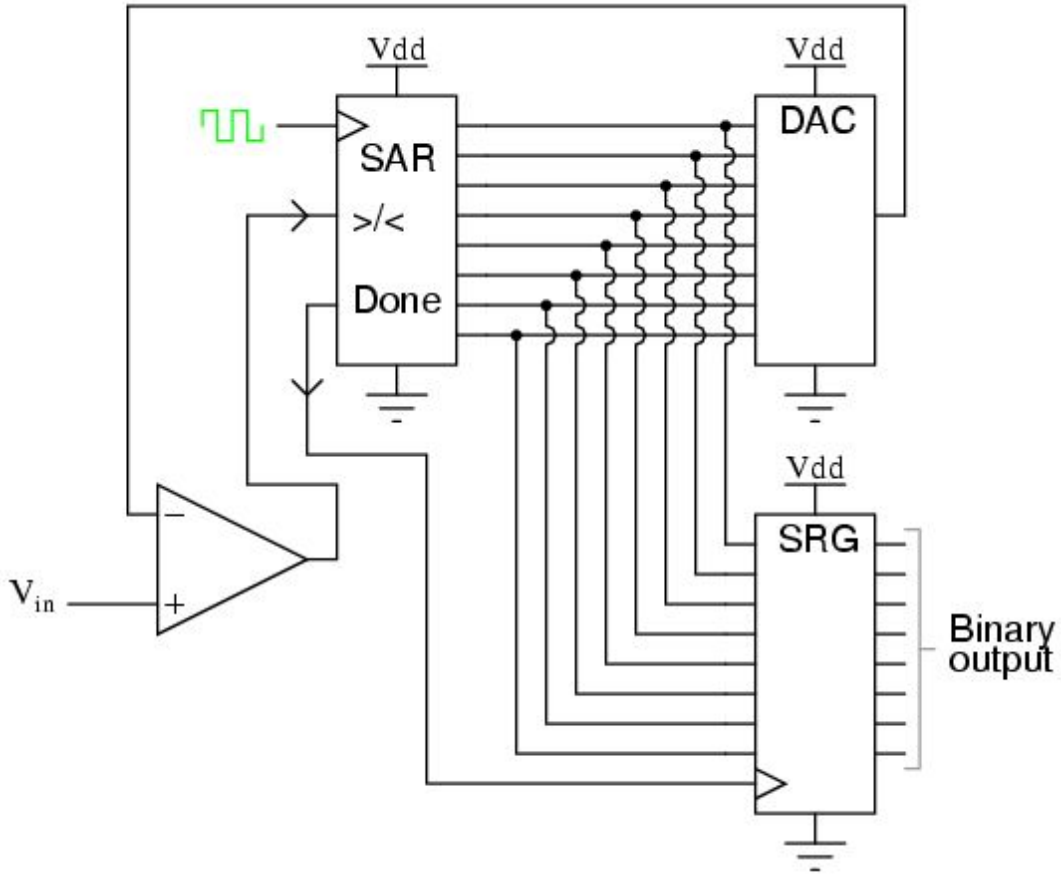
Successive Approximation ADC

- A Successive Approximation Register (SAR) is added to the circuit
- Instead of counting up in binary sequence, this register counts by trying all values of bits starting with the MSB and finishing at the LSB.
- The register monitors the comparators output to see if the binary count is greater or less than the analog signal input and adjusts the bits accordingly

Successive Approximation ADC



Successive Approximation ADC Circuit



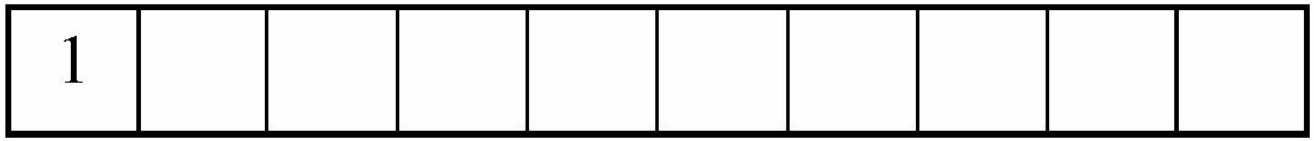
Successive Approximation Example

- 10 bit resolution or 0.0009765625V of Vref
- Vin= .6 volts
- Vref=1volts
- Find the digital value of Vin

Bit	Voltage
9	.5
8	.25
7	.125
6	.0625
5	.03125
4	.015625
3	.0078125
2	.00390625
1	.001952125
0	.0009765625

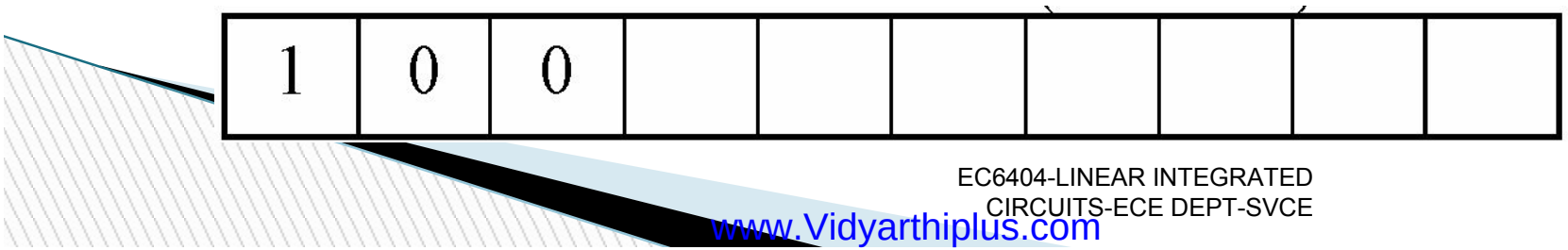
Successive Approximation

- MSB (bit 9)
  - Divided V_{ref} by 2
  - Compare V_{ref} /2 with V_{in}
  - If V_{in} is greater than V_{ref} /2 , turn MSB on (1)
  - If V_{in} is less than V_{ref} /2 , turn MSB off (0)
  - V_{in} =0.6V and V=0.5
  - Since V_{in}>V, MSB = 1 (on)



Successive Approximation

- Next Calculate MSB-1 (bit 8)
  - Compare V_{in}=0.6 V to V=V_{ref}/2 + V_{ref}/4= 0.5+0.25 =0.75V
  - Since 0.6<0.75, MSB is turned off
- Calculate MSB-2 (bit 7)
  - Go back to the last voltage that caused it to be turned on (Bit 9) and add it to V_{ref}/8, and compare with V_{in}
  - Compare V_{in} with (0.5+V_{ref}/8)=0.625
  - Since 0.6<0.625, MSB is turned off



Successive Approximation

- Calculate the state of MSB-3 (bit 6)
  - Go to the last bit that caused it to be turned on (In this case MSB-1) and add it to $V_{ref}/16$, and compare it to V_{in}
  - Compare V_{in} to $V= 0.5 + V_{ref}/16= 0.5625$
  - Since $0.6>0.5625$, MSB-3=1 (turned on)

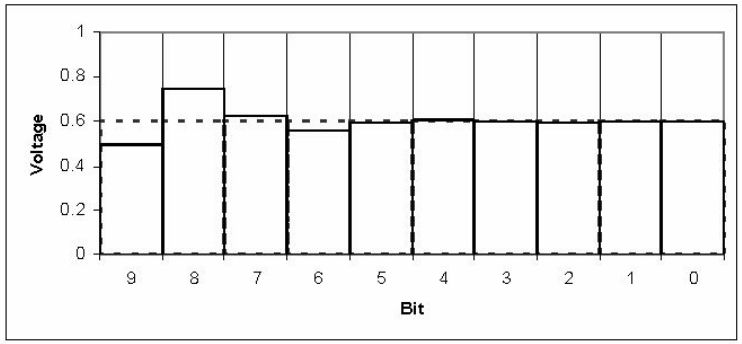
Successive Approximation

- This process continues for all the remaining bits.

•Digital Results:

MSB	MSB-1	MSB-2	MSB-3	…					LSB
1	0	0	1	1	0	0	1	1	0

•Results: $\frac{1}{2}+\frac{1}{16}+\frac{1}{32}+\frac{1}{256}+\frac{1}{512}=.599609375\ \text{V}$



Successive Approximation ADC

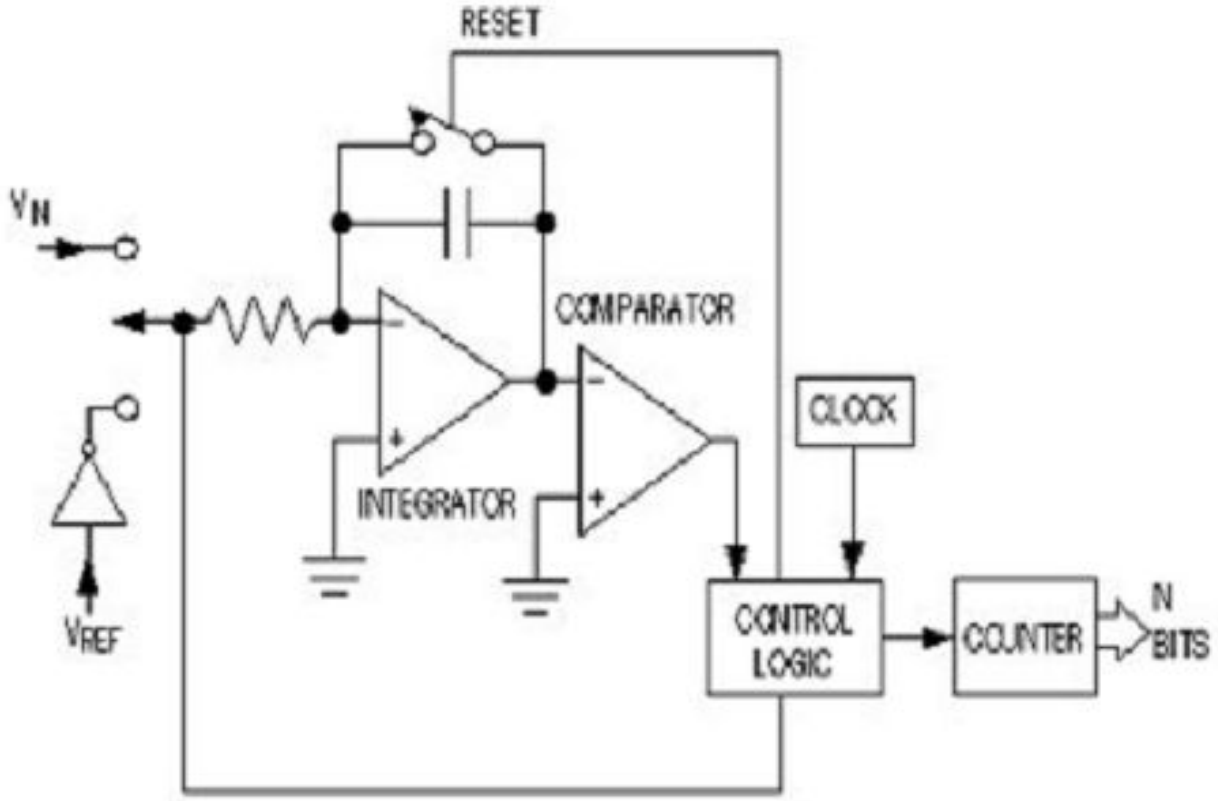
Advantages

- Capable of high speed and reliable
- Medium accuracy compared to other ADC types
- Good tradeoff between speed and cost
- Capable of outputting the binary number in serial (one bit at a time) format.

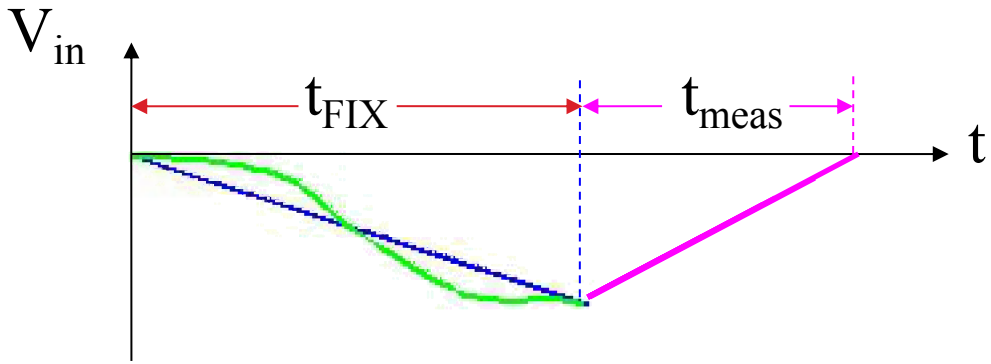
Disadvantages

- Higher resolution successive approximation ADC's will be slower
- Speed limited to ~5Msps

Integrating ADC



Dual Slope Converter



- The sampled signal charges a capacitor for a fixed amount of time
- By integrating over time, noise integrates out of the conversion
- Then the ADC discharges the capacitor at a fixed rate with the counter counts the ADC's output bits. A longer discharge time results in a higher count

Dual Slope Converter

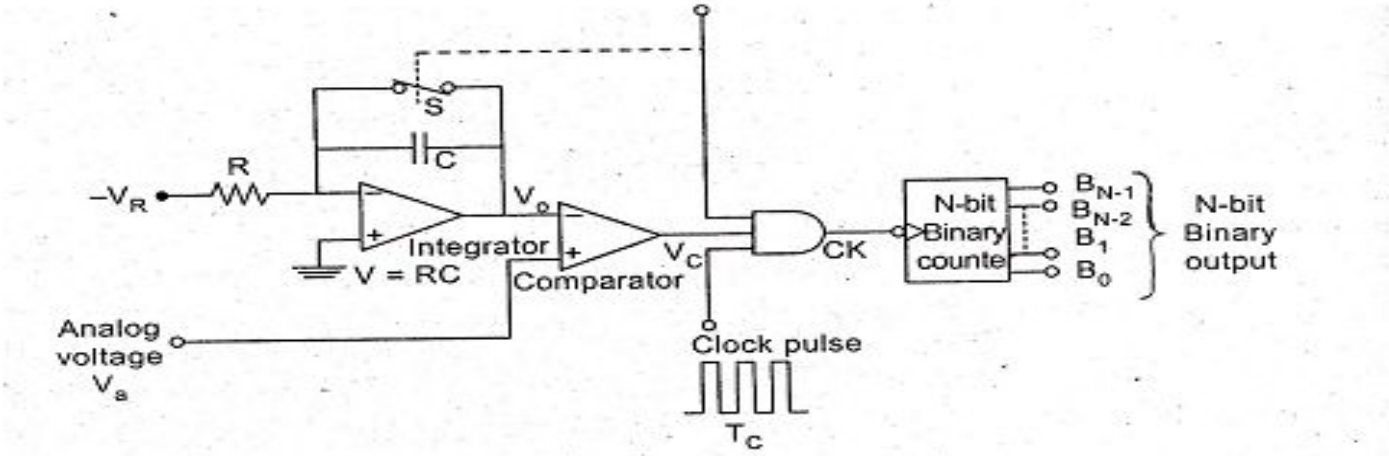
Advantages

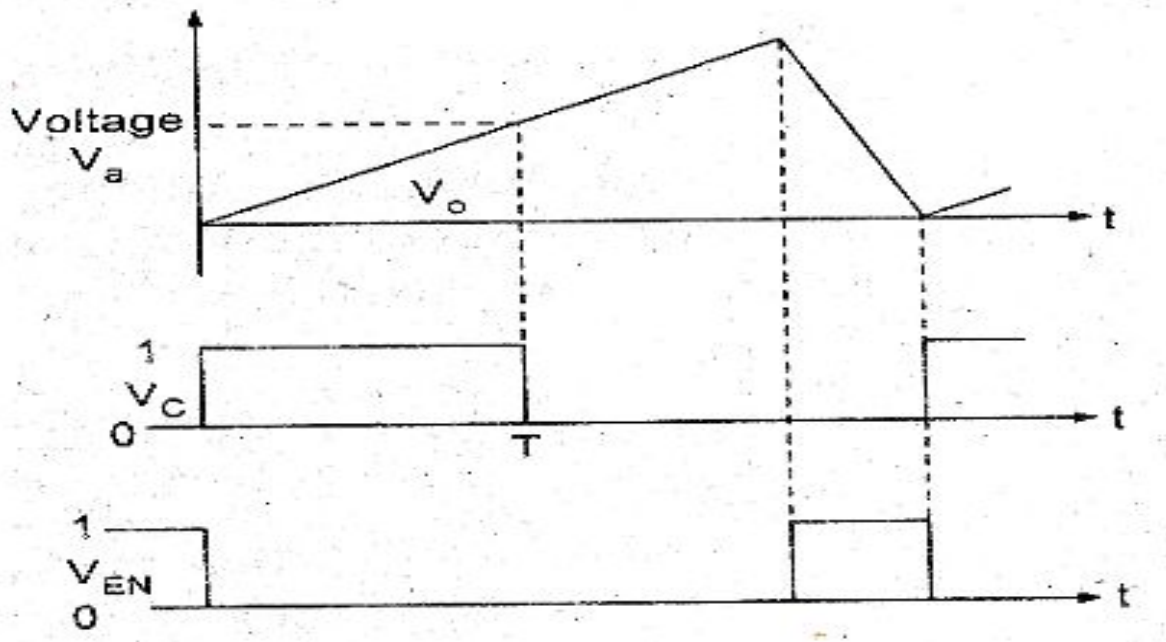
- Input signal is averaged
- Greater noise immunity than other ADC types
- High accuracy

Disadvantages

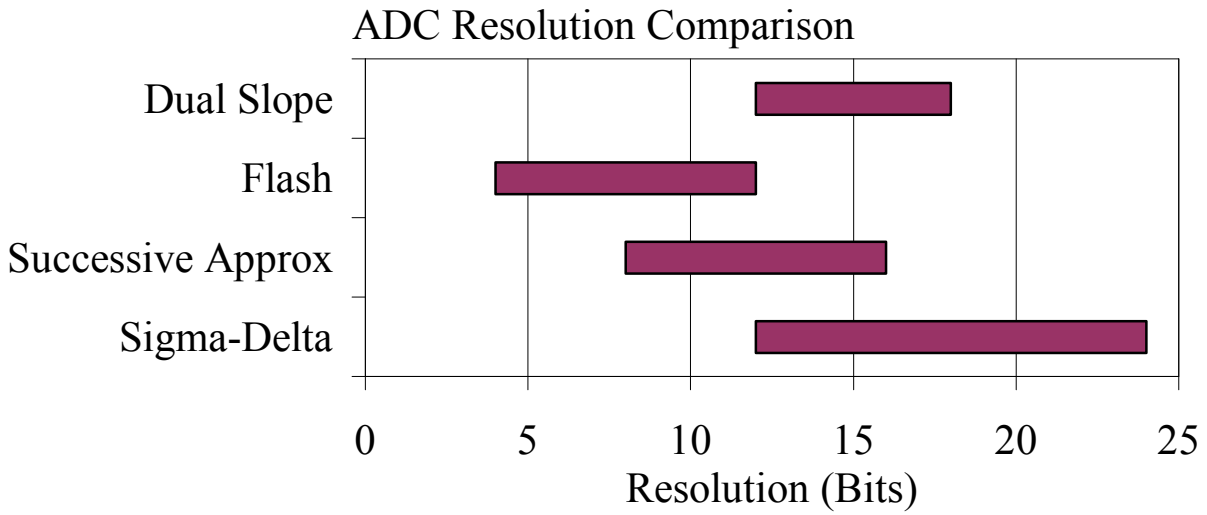
- Slow
- High precision external components required to achieve accuracy

A/D using Voltage to Time conversion





ADC Types Comparison



Type	Speed (relative)	Cost (relative)
Dual Slope	Slow	Med
Flash	Very Fast	High
Successive Appox	Medium – Fast	Low
Sigma-Delta	Slow	Low

Analog Switches

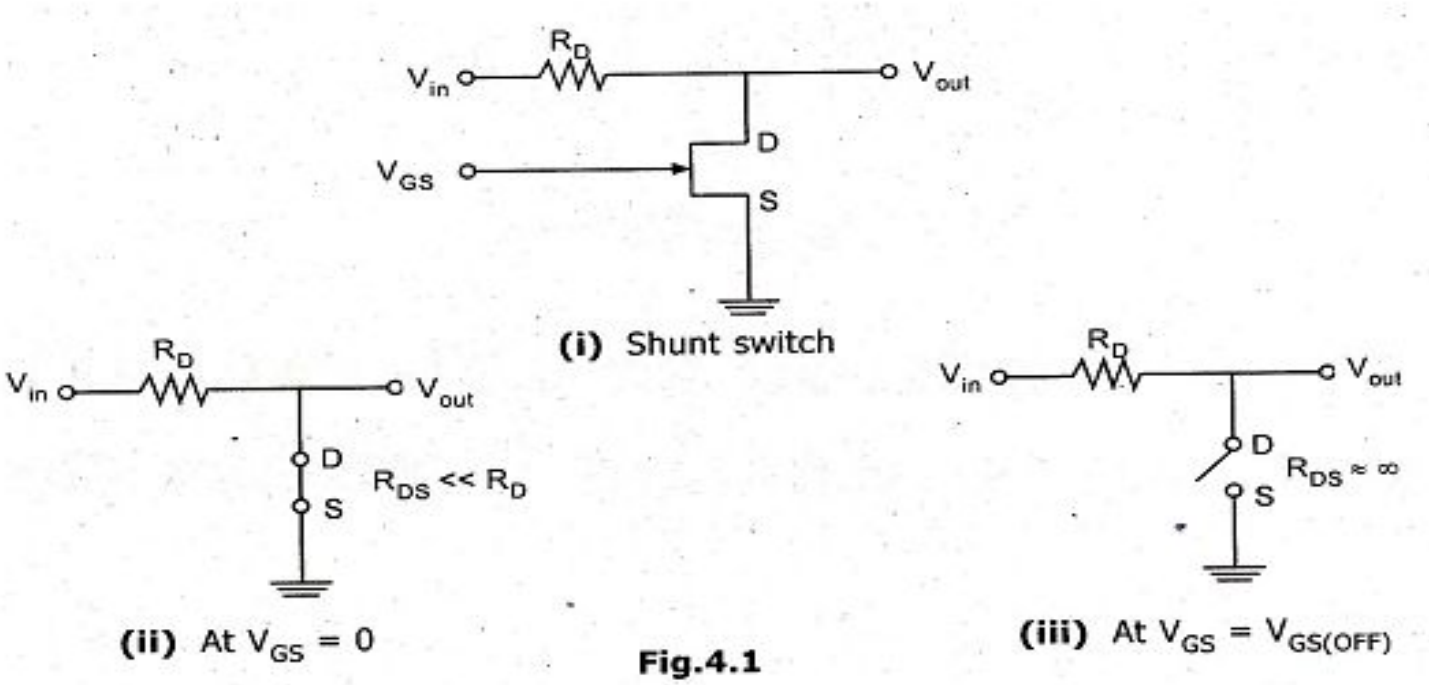


Fig.4.1

Analog Switches

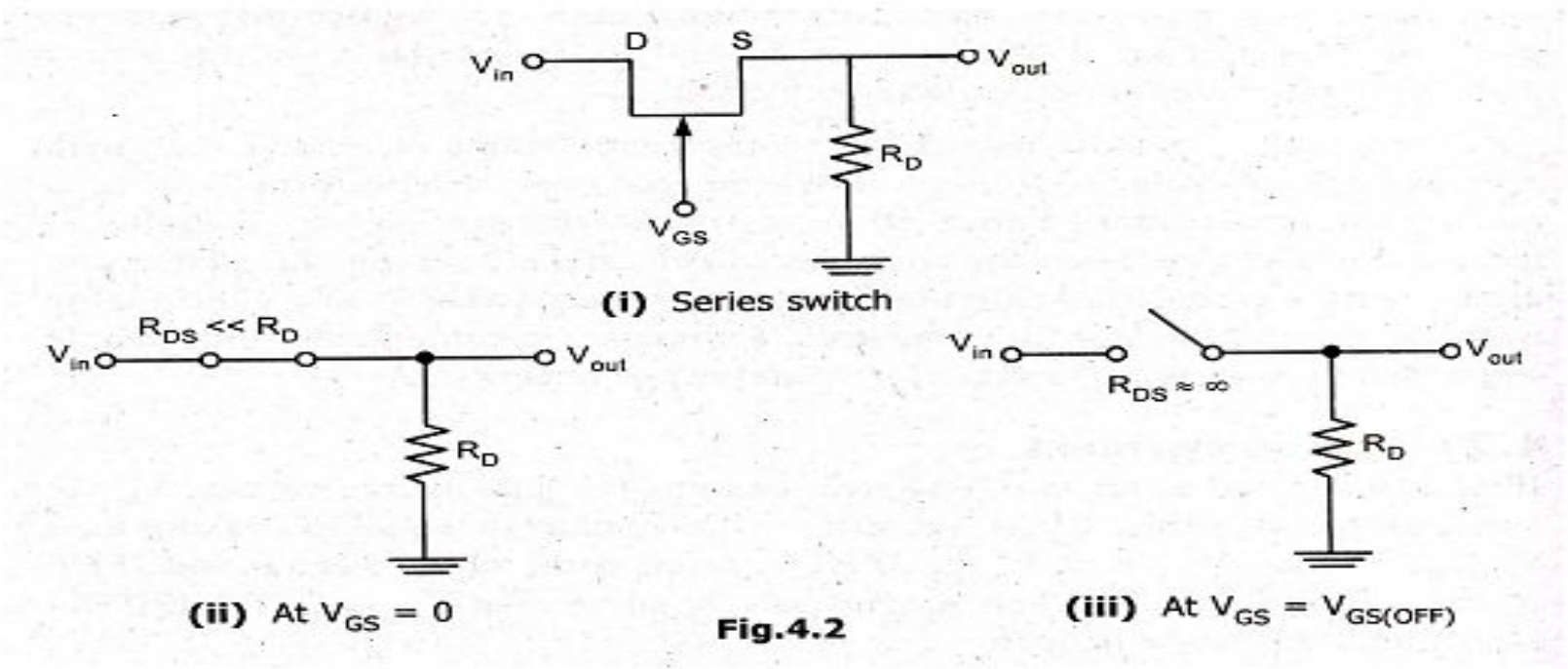
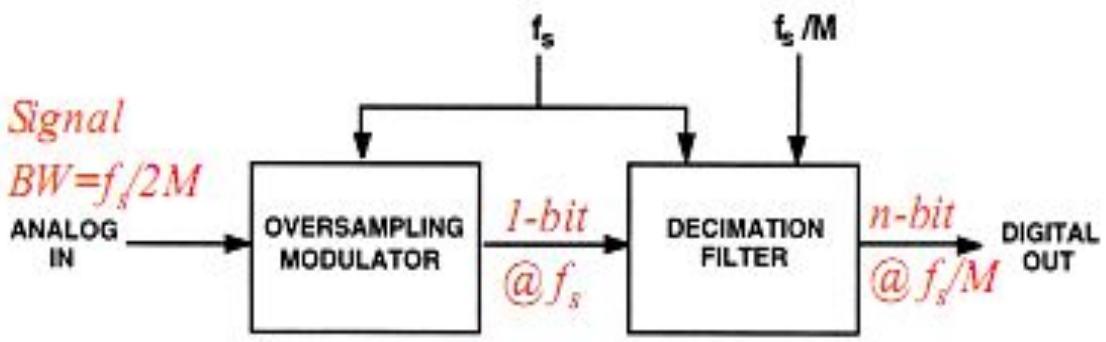


Fig.4.2

Oversampling A/D converters

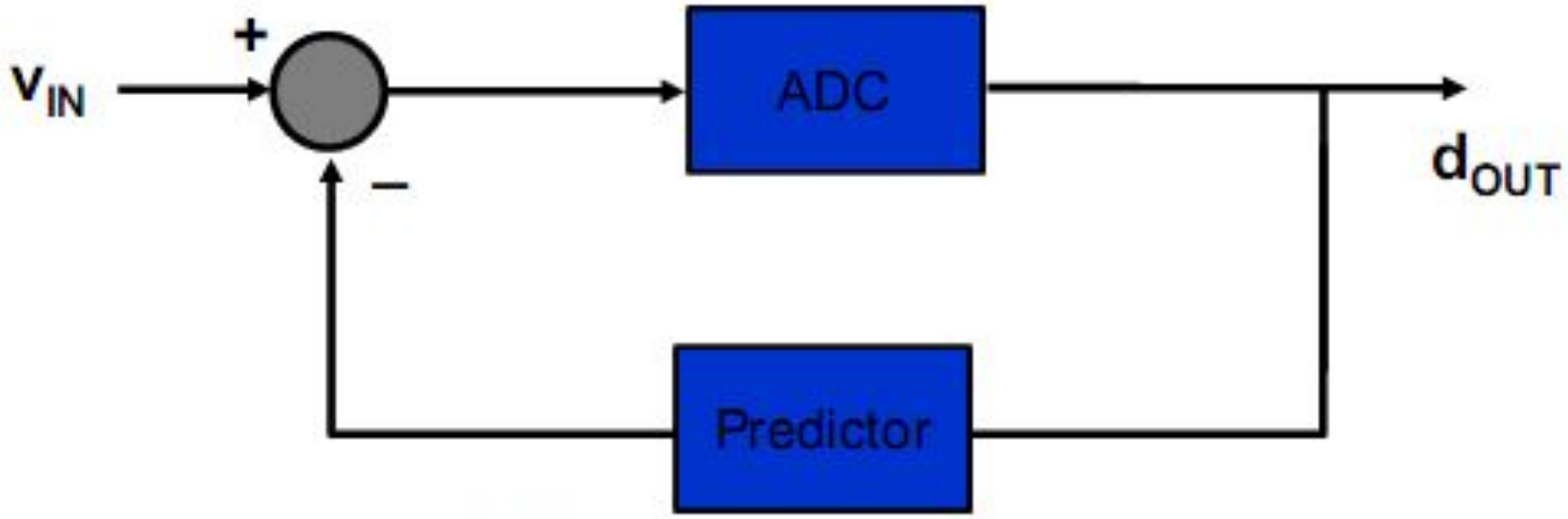


f_s = Sampling Rate

M = Oversampling Ratio

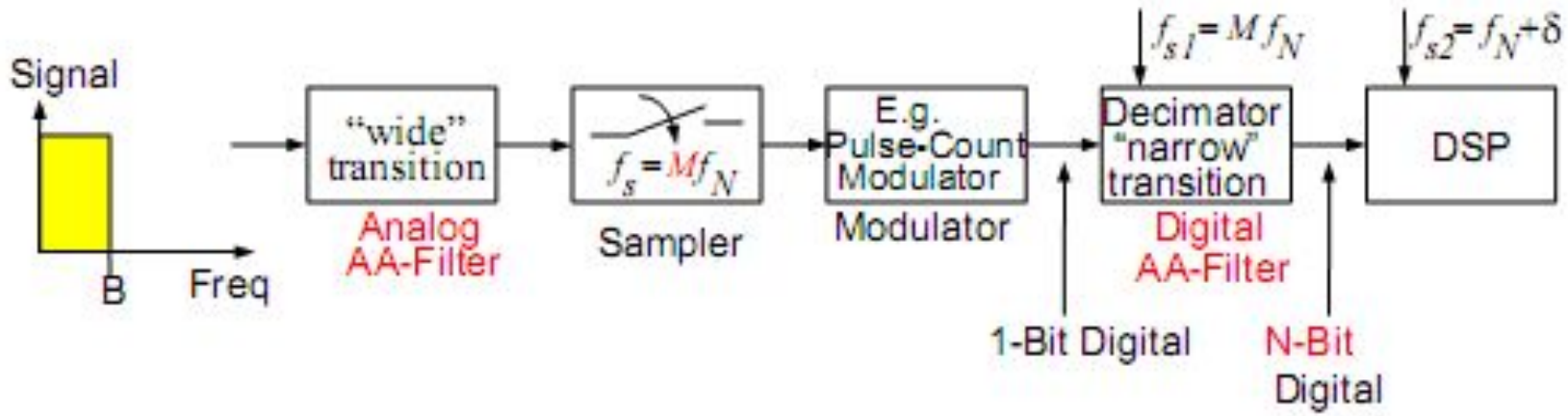
- Analog front-end → oversampled noise-shaping modulator
  - •Converts original signal to a 1-bit digital output at the high rate of $(2MXf_{signal})$
- Digital back-end → digital filter
  - •Removes out-of-band quantization noise
  - •Provides anti-aliasing to allow re-sampling @ lower sampling rate

Oversampled ADC Predictive Coding



- Quantize the difference signal rather than the signal itself
- Smaller input to ADC → Buy dynamic range
- Only works if combined with oversampling
- 1-Bit digital output
- Digital filter computes "average" →n-Bit output

Oversampled ADC



Decimator:

- Digital (low-pass) filter
- Removes quantization error for f > B
- Provides most anti-alias filtering
- Narrow transition band, high-order
- 1-Bit input, N-Bit output (essentially computes "average")