→ The gain factors such as Voltage, Current, transconductance and transresistance of amplifiers are functions of signal frequency.

→ In the amplifier gain versus frequency plot, the gain factor is plotted in terms of decibels and frequency in terms of Hertz on logarithmic scales.

→ The main purpose is to determine the frequency response of amplifier circuits due to circuit capacitors and transistor capacitances. The frequency response will be useful to determine bandwidth of the circuit.

Logarithms:

→ The analysis of amplifiers normally extends over a wide frequency range. Use of logarithmic scale makes it comfortable plotting the response between wide limits.

→ Logarithm taken to the base 10 is common logarithm i.e $\log_{10} a$.

→ Natural logarithm is taken to the base 'e' i.e $\log_e a$.

$e = 2.71828$ and $\log_e a = 2.3 \log_{10} a$.

→ In amplifier analysis a frequency of 10,000 Hz becomes $\log_{10} 10^4 = 4 \log_{10} 10 = 4$ in logarithmic scale.

→ Thus the frequency plot is compressed without major loss of information and the problem of dealing with huge numbers is overcome.

→ In a semilog graph only one of the two scales is a log-scale. In a double log graph both the scales are log scales.

Fig (a) Semi log graph

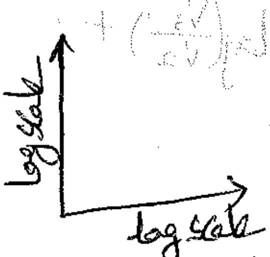


Fig (b) Double log graph

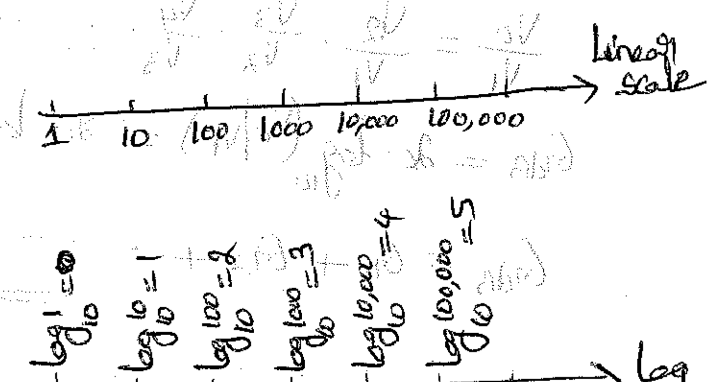


Fig (c): Conversion from linear scale to logarithmic scale.

→ Figure (c) shows how a linear scale is converted into a log scale. Thus logarithmic scale helps to explain variations of parameters over a wide range by a simple graph.

Decibels:

→ Decibel is used to compare two power levels on a logarithmic basis. The term "bel" is derived from the name of telephone invention, Alexander Graham Bell. The unit "bel" (B) is defined relating two power levels P_1 and P_2 as,

$$G = \log_{10}(P_2/P_1) \text{ bel.}$$

As "bel" was found to be a large unit for measurement, the "decibel" (dB) is defined where 10 decibels = 1 bel.

Hence, $$G_{dB} = 10 \log_{10}(P_2/P_1) \text{ dB.}$$

→ In terms of Voltage $P_1 = V_1^2/R_i$ and $P_2 = V_2^2/R_o$ Let $R_i = R_o$

$$\therefore \quad G_{dB} = 10 \log_{10}\left(\frac{P_2}{P_1}\right) = 10 \log_{10} \frac{V_2^2/R_i}{V_1^2/R_i} = 10 \log_{10}(V_2/V_1)^2$$

$$\therefore \quad G_{dB} = 20 \log_{10}(V_2/V_1) \text{ dB.}$$

→ The advantage of logarithmic relationship is that the overall gain of a cascade system is simply the sum of individual gains.

$$G = G_1 \cdot G_2 \cdot G_3 \cdots\cdots G_{n-1} \cdot G_n$$

$$\frac{V_o}{V_1} = \frac{V_2}{V_1} \cdot \frac{V_3}{V_2} \cdot \frac{V_4}{V_3} \cdots\cdots \frac{V_n}{V_{n-1}} \cdot \frac{V_o}{V_n}$$

$$G_{dB} = 20 \log_{10}(V_o/V_1) = 20 \log_{10}\left(\frac{V_2}{V_1}\right) + 20 \log\left(\frac{V_3}{V_2}\right) + \cdots\cdots + 20 \log_{10}\left(\frac{V_o}{V_n}\right)$$

$$G_{dB} = G_1 + G_2 + \cdots\cdots + G_n$$

Prob ①: A three stage amplifier has a first stage voltage gain of 30, second stage voltage gain of 200 and third stage gain of 400. Find the total voltage gain in d

Soln:

$$G_1 = 20 \log_{10} 30 = 20 \times 1.477 = 29.54$$

$$G_2 = 20 \log_{10} 200 = 20 \times 2.3 = 46$$

$$G_3 = 20 \log_{10} 400 = 20 \times 2.6 = 52$$

$$\therefore G = G_1 + G_2 + G_3 = 127.54\,dB$$

Prob ②: In an amplifier the output power is 1.5W at 2KHz and 0.3W at 20Hz, while the input power is constant at 10mW. Determine by how many decibel is the gain at 20Hz below that at 2KHz.

Soln:

At 2KHz output power is 1.5W and input power is 10mW.

$$\therefore G_{dB} = 10 \log_{10} \frac{1.5}{10 \times 10^{-3}} = 10 \log_{10} 150 = 21.76\,dB$$

At 20Hz output power is 0.3W and input power is 10mW.

$$\therefore G_{dB} = 10 \log \frac{0.3}{10 \times 10^{-3}} = 10 \log_{10} 30 = 14.77\,dB.$$

Fall in gain from 2KHz to 20Hz $= 21.76 - 14.77 = 6.99\,dB$

Prob ③: An amplifier has a voltage gain of 15dB. If the input signal voltage is 0.8V, determine output voltage.

Soln:

$$A_{V\,dB} = 20 \log_{10} (V_2/V_1)$$

$$15 = 20 \log_{10} (V_2/0.8)$$

$$0.75 = \log_{10} (V_2/0.8)$$

$$10^{0.75} = \frac{V_2}{0.8}$$

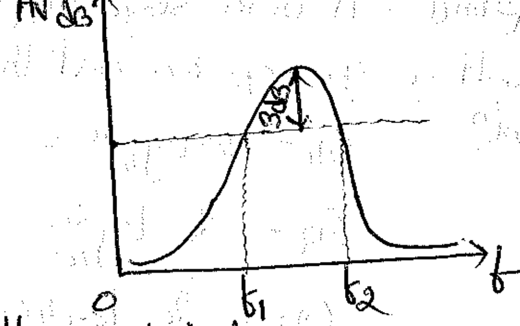
$$\Rightarrow V_2 = 4.5V$$

Half power Bandwidth:

$$\text{Half power gain in dB} = 10 \log_{10} \frac{P_{o(max)}/2}{P_{o(max)}}$$

$$= 10 \log_{10}(1/2)$$

$$= -3 dB$$



Hence, the half power gain is maximum gain minus three decibels.

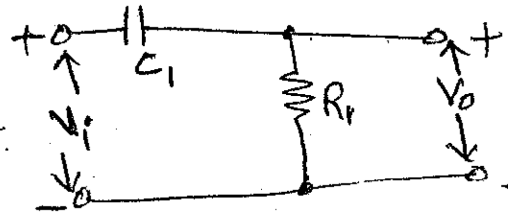
Half power bandwidth i.e $(f_2 - f_1)$ is the frequency range over which gain is more than half power gain.

Frequency response:

→ The voltage gain of the amplifiers and the phase shift of the gain depend on the frequency range over which amplifiers operate.
→ In general the entire frequency range can be divided into three ranges
① Mid frequency range
② Low frequency range
③ High frequency range.

Mid frequency range:

→ In this frequency range the voltage gain is practically constant, that is not affect by the changes of the capacitances in the circuit.
→ The reactance $\frac{1}{\omega C_c}$ of the coupling capacitor in series between the amplifying stages is very small so that it can be neglected.
→ The reactances of the internal capacitances of the transistor are very large because these capacitances have very small values and as these equivalent capacitances come in parallel with the associated resistances, they are not considered in this high frequency range.
→ Thus in the mid frequency range all the capacitive reactances are neglected as compared with the associated resistances.



Low frequency range:

→ In this frequency range, the circuit behaves like the simple high pass circuit as shown in figure with time constant $T_1 = R_1C_1$.

$$A_{OL} = \frac{V_o}{V_i} = \frac{R_1}{R_1 + \frac{1}{j\omega_1 C_1}} = \frac{1}{1 - j\frac{1}{\omega R_1 C_1}} = \frac{1}{1 - j\frac{1}{2\pi f R_1 C_1}} = \frac{1}{1-j\left(\frac{f_L}{f}\right)}$$

where $f_L = \frac{1}{2\pi R_1 C_1}$

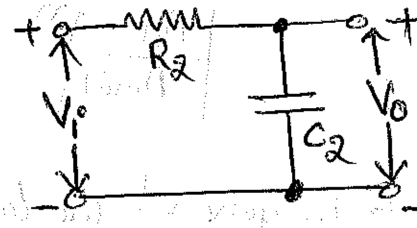
$$\therefore |A_{OL}| = \frac{1}{\sqrt{1 + (f_L/f)^2}} \quad \text{and phase } \theta_1 = -\tan^{-1}(f_L/f)$$

At $f = f_L$, $A_{OL} = \frac{1}{\sqrt{2}} = 0.707$ whereas at midband frequency $A_{o} = 1$.

→ Therefore the frequency at which gain is 0.707 times its midband value A_0 is called f_L. This drop corresponds to a decimal reduction of $20\log(0.707)$ or 3dB and hence f_L is called lower 3dB cut-off frequency.

High frequency range:

→ Above the midband frequency i.e $f > f_H$, the transistor behaves like the simple lowpass circuit shown in figure with time constant $T_2 = R_2C_2$.



$$A_{OH} = \frac{V_o}{V_i} = \frac{\frac{1}{j\omega C_2}}{R_2 + \frac{1}{j\omega C_2}} = \frac{1}{1 + j\omega R_2C_2}$$

$$\therefore A_{OH} = \frac{1}{1 + j2\pi f R_2C_2} = \frac{1}{1 + j(f/f_H)}; \text{ where } f_H = \frac{1}{2\pi R_2C_2}$$

$$\therefore |A_{OH}| = \frac{1}{\sqrt{1 + (f/f_H)^2}} \text{ and the phase is } \theta_2 = -\tan^{-1}(f/f_H).$$

→ At $f = f_H$, $A_{OH} = \frac{1}{\sqrt{2}} = 0.707$ i.e the gain is reduced to 0.707 times its midband value A_0. Hence f_H is called the upper 3dB cut-off frequency.

→ The values θ_1 and θ_2 represents the angle by which the output lags the input signal.

→ The frequency range between f_L and f_H is called the bandwidth of the amplifier.

Effect of cascading on gain:

If A_{mid} is mid frequency gain per stage, the overall mid frequency gain of n identical stages will be,

$$A_{mid(overall)} = |A_m|^n$$

Also,

$$\left|\frac{A_L}{A_{mid}}\right| = \frac{1}{\sqrt{1 + (f_L/f)^2}}$$

$$\therefore \left|\frac{A_L}{A_{mid}}\right|^n = \frac{1}{[1 + (f_L/f)^2]^{n/2}}$$

The lower 3dB frequency for overall low frequency gain can be defined such that at $f = f_{L(n)}$

$$\left|\frac{A_L}{A_{mid}}\right|^n = \frac{1}{\sqrt{2}} = \frac{1}{\left[1+(f_L/f_{L(n)})^2\right]^{n/2}}$$

IIIly overall high frequency gain can be written as,

$$\left|\frac{A_H}{A_{mid}}\right|^n = \frac{1}{\sqrt{2}} = \frac{1}{\left[1+(f_{H(n)}/f_H)^2\right]^{n/2}}$$

→ In general we can determine the gain of multistage amplifier at any frequency below lower cut-off frequency of individual stage can be given as

$$A_{VL} = \frac{(A_{mid})^n}{\left[1+(f_L/f)^2\right]^{n/2}}$$

IIIly the gain of multistage amplifier at any frequency above higher cut-off frequency of individual stage can be given as,

$$A_{VH} = \frac{(A_{mid})^n}{\left[1+(f/f_H)^2\right]^{n/2}}$$

Effect of Cascading on Bandwidth:

→ The frequency response and bandwidth of the amplifier get affected due to the cascade connection. The bandwidth of cascaded amplifier is always less than that of the bandwidth of single stage amplifier.

ⓐ Lower 3dB frequency:

Let the lower 3dB frequency of 'n' identical cascaded stages is $f_{L(n)}$. It is the frequency for which the overall gain falls to $\frac{1}{\sqrt{2}}$ (3dB) of its midband value.

$$\left[\frac{1}{\sqrt{1+(f_L/f_{L(n)})^2}}\right]^n = \frac{1}{\sqrt{2}}$$

$$\therefore \quad \sqrt{2} = \left[\sqrt{1+(f_L/f_{L(n)})^2}\right]^n$$

$$\Rightarrow \quad 2 = \left[1+(f_L/f_{L(n)})^2\right]^n$$

$$\Rightarrow \quad 2^{\frac{1}{n}} = 1+\left(\frac{f_L}{f_{L(n)}}\right)^2$$

$$\Rightarrow \quad 2^{\frac{1}{n}}-1 = (f_L/f_{Ln})^2$$

$$\Rightarrow \quad \frac{f_L}{f_{L(n)}} = \sqrt{2^{\frac{1}{n}}-1}$$

$$\Rightarrow \quad f_{L(n)} = \frac{f_L}{\sqrt{2^{\frac{1}{n}}-1}}$$

(b) upper 3dB frequency:

Let the upper 3dB frequency of 'n' identical stages is $f_{H(n)}$. It is the frequency for which the overall gain falls to $\frac{1}{\sqrt{2}}$ (3dB) of its midband value.

$$\left[\frac{1}{\sqrt{1+(f_{H(n)}/f_H)^2}}\right]^n = \frac{1}{\sqrt{2}}$$

$$\therefore \quad \sqrt{2} = \left[\sqrt{1+(f_{H(n)}/f_H)^2}\right]^n$$

$$\Rightarrow \quad 2^{\frac{1}{n}} = 1+\left(\frac{f_{H(n)}}{f_H}\right)^2$$

$$\Rightarrow \quad \sqrt{2^{\frac{1}{n}}-1} = \frac{f_{H(n)}}{f_H}$$

$$\therefore \quad f_{H(n)} = f_H\sqrt{2^{\frac{1}{n}}-1}$$

→ In multistage amplifier $f_{L(n)}$ is always greater than f_L and $f_{H(n)}$ is always less than f_H.

→ Therefore the bandwidth of multistage amplifier is always less than single stage amplifier.

Prob①: An Amplifier consists of 3 identical stages in cascade, the bandwidth of overall amplifier extends from 20 Hz to 20 KHz. Calculate the bandwidth of individual stages.

Soln: $f_{L(n)} = 20\,Hz \qquad f_{H(n)} = 20\,KHz$

$$f_{L(n)} = \frac{f_L}{\sqrt{2^{\frac{1}{n}}-1}} \Rightarrow f_L = f_{L(n)} \cdot \sqrt{2^{\frac{1}{n}}-1} = 20 \times \sqrt{2^{\frac{1}{3}}-1} = 10.196\,Hz$$

$$f_{H(n)} = f_H\sqrt{2^{\frac{1}{n}}-1} \Rightarrow f_H = \frac{f_{H(n)}}{\sqrt{2^{\frac{1}{n}}-1}} = \frac{20 \times 10^3}{\sqrt{2^{\frac{1}{3}}-1}} = 39.23\,KHz.$$

$$\therefore BW = f_H - f_L = 39.23 \times 10^3 - 10.196 = 39.218\,KHz.$$

NOTE:

→ In general, $A_{VL} = \frac{V_o}{V_i} = \frac{1}{\sqrt{1+(f_L/f)^2}} \boxed{\tan^{-1}(f_L/f)}$

$$|A_{VL}|_{dB} = 20\log_{10}\frac{1}{\sqrt{1+(f_L/f)^2}} = -10\log_{10}\left[1+\left(\frac{f_L}{f}\right)^2\right]$$

If $f_L \gg f$, $|A_{VL}|_{dB} = -10\log_{10}(f_L/f)^2 = -20\log_{10}(f_L/f)$

when $f = f_L$ then $|A_V|_{dB} = -20\log_{10}1 = 0\,dB$

when $f = f_L/2$ then $|A_V|_{dB} = -20\log_{10}2 = -6\,dB$

when $f = f_L/4$ then $|A_V|_{dB} = -20\log_{10}4 = -12\,dB$

when $f = f_L/10$ then $|A_V|_{dB} = -20\log_{10}10 = -20\,dB$

Effect of Various Capacitors on Frequency Response:

① Effect of Coupling Capacitors

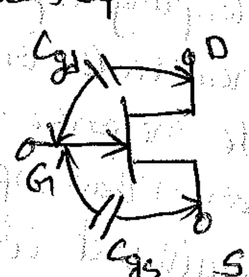
$X_C = \frac{1}{2\pi fC}$, at medium and high frequencies, the factor 'f' makes 'X_C' very small so that all Coupling Capacitors behave as short circuits. At low frequencies X_C increases. This increase in X_C drops the signal voltage across the Capacitor and reduces the circuit gain. As signal frequencies decrease, the Capacitor reactances increase and circuit gain continues to fall, reducing the output Voltage.

② Effect of Bypass Capacitors:

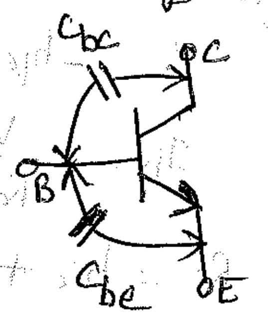
At lower frequencies, the bypass Capacitor C_E is not a short, so, the emitter is not at ac ground. X_C in parallel with R_E (R_S in case of FET) creates an impedance. The signal Voltage drops across this impedance reducing the circuit gain.

③ Effect of Internal Transistor Capacitances:

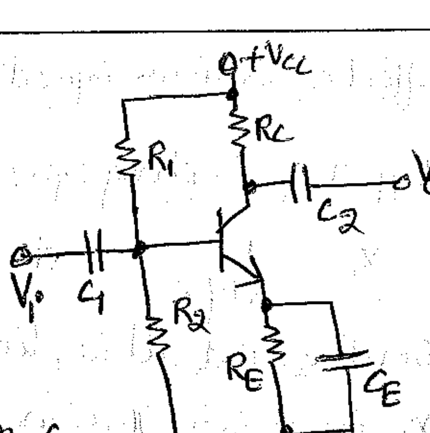
→ At high frequencies, the coupling and bypass Capacitors act as short circuit and do not affect the amplifier frequency response. However at high frequencies, the internal Capacitances Commonly Known as junction Capacitances do Come into play, reducing the circuit gain.



→ At higher frequencies, the reactances of the junction Capacitances are low. As frequency increases, the reactances of junction Capacitances fall. when these reactances become small enough, they provide shunting effect as they are in parallel with junctions. This reduces the circuit gain and hence the output Voltage.



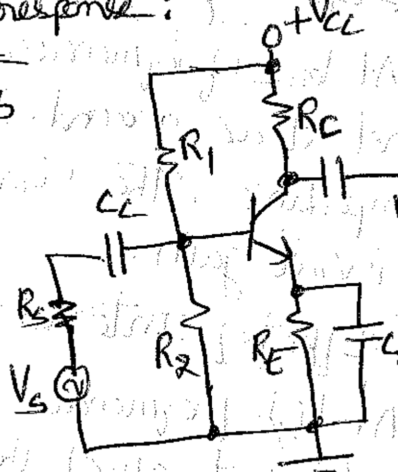
Low frequency Analysis of BJT:



→ The amplifier shown in figure has three RC networks that affect its gain as the frequency is reduced below midrange. These are,

1) RC network formed by the input coupling capacitor C_1 and the input impedance of the amplifier.
2) RC network formed by the output coupling capacitor C_2, the resistance looking in at the collector and the load resistance.
3) RC network formed by the emitter bypass capacitor C_E and the resistance looking in at the emitter.

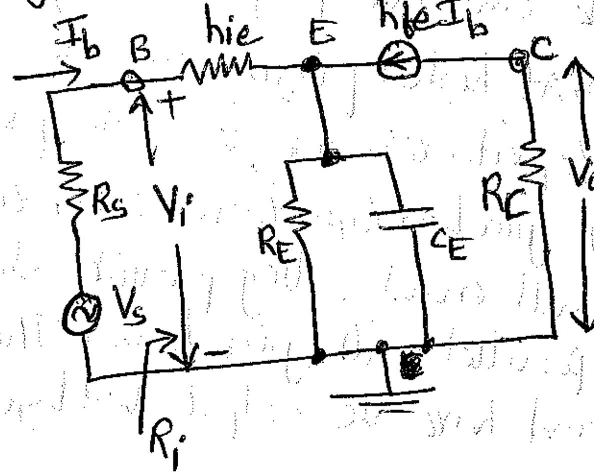
Effect of Emitter Bypass capacitor 'C_E' on low frequency response:



→ Voltage gain in low frequency region A_{VLF} is defined as the ratio of output voltage V_o to the source voltage V_s.

$$A_{V(LF)} = \frac{V_o}{V_s}$$

→ It is assumed that in low frequency region the coupling capacitor 'C_i' is sufficiently large so that its reactance is small and it does not have any effect on the response. Further it is assumed that $R_1 || R_2$ is much larger than input resistance R_i so that they may be neglected in the h-parameter equivalent circuit as shown.



$$V_o = -h_{fe} I_b R_C$$

$$I_b = \frac{V_s}{R_s + R_i}$$

$$R_i = h_{ie} + (1+h_{fe}) Z_E$$

where $Z_E = R_E || X_{CE} = \dfrac{R_E}{1 + j\omega C_E R_E}$

$$\therefore R_i = h_{ie} + \frac{(1+h_{fe}) R_E}{1 + j\omega C_E R_E}$$

$$\therefore \quad I_b = \frac{V_s}{R_s + h_{ie} + \dfrac{(1+h_{fe})R_E}{1+j\omega C_E R_E}}$$

$$V_o = -h_{fe} R_C I_b = -h_{fe} R_C \frac{V_s}{R_s + h_{ie} + \dfrac{(1+h_{fe})R_E}{1+j\omega C_E R_E}}$$

$$\therefore \quad A_{V(LF)} = \frac{V_o}{V_s} = \frac{-h_{fe} R_C}{R_s + h_{ie} + \dfrac{(1+h_{fe})R_E}{1+j\omega C_E R_E}}$$

when 'ω' is large in mid frequency range,

$$A_{V(MF)} = \frac{V_o}{V_s} = \frac{-h_{fe} R_C}{R_s + h_{ie}}$$

$$\therefore \quad \frac{A_{V(LF)}}{A_{V(MF)}} = \frac{R_s + h_{ie}}{R_s + h_{ie} + \dfrac{(1+h_{fe})R_E}{1+j\omega C_E R_E}}$$

$$= \frac{1}{1 + \dfrac{(1+h_{fe})R_E}{R_s + h_{ie}}} \times \frac{1 + j\left(\dfrac{f}{f_0}\right)}{1 + j\left(\dfrac{f}{f_p}\right)}$$

where $f_0 = \dfrac{1}{2\pi C_E R_E}$ and $f_p = \dfrac{1 + \dfrac{(1+h_{fe})R_E}{R_s + h_{ie}}}{2\pi C_E R_E}$

If $\dfrac{(1+h_{fe})R_E}{R_s + h_{ie}} \gg 1$.

$$\therefore \quad f_p \approx \frac{(1+h_{fe})R_E}{(R_s + h_{ie})\, 2\pi C_E R_E}$$

At $f = f_p$,

$$\frac{A_{V(LF)}}{A_{V(MF)}} = \frac{R_s + h_{ie}}{(1+h_{fe})R_E} \times \frac{1 + j\left(\dfrac{f_p}{f_0}\right)}{1+j} \qquad \left\{ \because \frac{(1+h_{fe})R_E}{R_s + h_{ie}} \gg 1 \right.$$

$$\frac{A_V(LF)}{A_V(MF)} \approx \frac{R_s+h_{ie}}{(1+h_{fe})R_E} \times \frac{j(f_P/f_0)}{1+j} \quad \left\{\because \; f_P \gg f_0\right\}$$

$$\therefore \left|\frac{A_V(LF)}{A_V(MF)}\right| = \frac{R_s+h_{ie}}{(1+h_{fe})R_E} \times \frac{(f_P/f_0)}{\sqrt{2}}$$

But $$\frac{f_P}{f_0} \approx \frac{(1+h_{fe})R_E}{R_s+h_{ie}}$$

$$\therefore \frac{A_V(LF)}{A_V(MF)} = \frac{1}{\sqrt{2}}$$

As the ratio of Voltage gain has dropped by $\frac{1}{\sqrt{2}}$, the power gain at this low frequency will be having a drop of $\frac{1}{2}$ or 3dB from the gain at mid frequency.

Thus, the lower 3dB frequency is:

$$f_L \approx f_P = \frac{1+\frac{(1+h_{fe})R_E}{R_s+h_{ie}}}{2\pi C_E R_E} \approx \frac{(1+h_{fe})R_E}{(R_s+h_{ie})2\pi C_E R_E} \approx \frac{1+h_{fe}}{(R_s+h_{ie})2\pi C_E}$$

when $f_P = f_0$, if this condition is not met, $f_L \neq f_P$ and there may not be a 3-dB point.

$$\therefore C_E = \frac{1+h_{fe}}{2\pi f_L (R_s+h_{ie})}$$

Thus 'C_E' determines the lower 3dB frequency f_L. The equation for f_L does not include R_E so that the choice of 'C_E' for a given 'f_L' is dependent only upon the transistor and the source resistance.

Note:

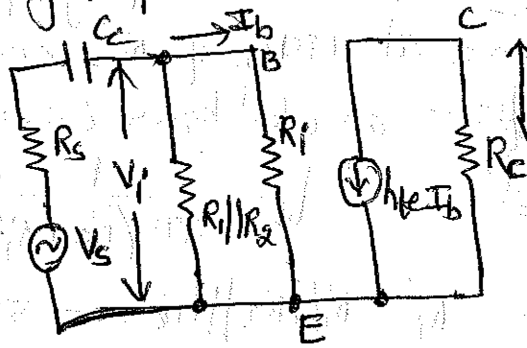
1) The use of electrolytic capacitors for 'C_E' cause reduction in the lower 3dB frequency and the mid frequency gain. If R_{CE} represents series resistance of C_E,

$$A_V(MF) = \frac{-h_{fe}R_C}{R_s+h_{ie}+(1+h_{fe})R_{CE}}$$

2) If the effect of biasing resistors R_1 and R_2 are taken into account,

$$A_V(MF) = \frac{-h_{fe}R_C}{R_s+h_{ie}+(h_{fe}R_s/R_B)}$$ where $R_B = R_1 // R_2$.

Effect of Input Coupling Capacitor 'C_c' on low frequency response:



Assume that C_E is large enough to cause no reduction in low frequency gain. with R_E effectively bypassed the low frequency model for the CE amplifier with the coupling capacitor 'C_c' is shown in figure.

In the mid frequency range reactance of 'C_c' is negligible. Hence, the equations for $A_{V(MF)}$ in previous section are valid.

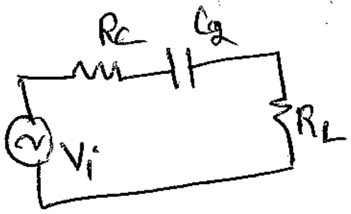
The lower 3dB frequency is $f_L = \dfrac{1}{2\pi(R_s+R_i')C_c}$

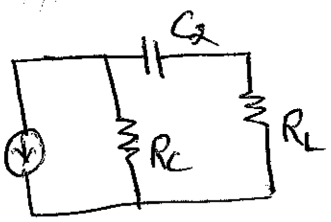
where $R_i' = R_1||R_2||R_i$

$R_i = h_{ie}$ for an ideal emitter bypass capacitor

$R_i \approx h_{ie} + (1+h_{fe})R_{CE}$ if capacitor's series resistance is taken into account.

Output Coupling Capacitor:





The critical frequency of this RC network is,

$$f_L = \frac{1}{2\pi(R_C+R_L)C_2}$$

Prob: For the CE amplifier calculate mid frequency voltage gain and lower 3dB po[int]. The circuit parameters are

The h-parameters are $h_{fe}=400$, $h_{ie}=10K\Omega$, the circuit parameters are $V_{CC}=12V$, $R_1=15K\Omega$, $R_2=2.2K\Omega$ & $C_E=50\mu$[F]
$R_S=600\Omega$, $R_C=5K\Omega$, $R_E=1K\Omega$,

Soln:

$$A_{V(MF)} = \frac{-h_{fe}R_C}{R_S + h_{ie} + \frac{h_{fe}R_S}{R_B}} = \frac{-400\times5\times10^3}{600+10\times10^3+\frac{400\times600}{15\times10^3\times2.2\times10^3}\times(15\times10^3+\ldots)}$$

$$A_{V(MF)} = -\cancel{186}.\cancel{47}$$

$$f_L = \frac{1+h_{fe}}{(R_s+h_{ie})2\pi C_E} = \frac{1+400}{(600+10\times10^3)\times2\pi\times50\times10^{-6}} = 120\,Hz.$$

prob②: Calculate the Coupling Capacitor C_c required to provide a low frequency 3dB point at 125Hz if $R_s = 600\Omega$, $h_{ie} = 1k\Omega$, $h_{fe} = 60$, $R_1 = 5k\Omega$ and $R_2 = 1.25k\Omega$ for ⓐ an ideal bypass Capacitor C_E ⓑ a practical bypass Capacitor with $R_{CE} = 25$

soln:

$$f_L = \frac{1}{2\pi (R_s + R_i')C_c}$$

ⓐ $R_i' = R_1 || R_2 || h_{ie} = 5\times10^3 || 1.25\times10^3 || 1\times10^3 = 500\Omega$

$$\therefore \quad C_c = \frac{1}{2\pi f_L (R_s + R_i')} = \frac{1}{2\pi \times 125 \times (600 + 500)} = 1.15\mu F$$

ⓑ $R_i' = R_1 || R_2 || [h_{ie} + (1 + h_{fe}) R_{CE}]$

$R_i' = 5K || 1.25K || [1K + (1 + 60) \times 25] = 716.31$

$$\therefore C_c = \frac{1}{2\pi f_L (R_s + R_i')} = \frac{1}{2\pi \times 125 \times (600 + 716.31)} = 0.97\mu F$$

Frequency Response at High Frequencies:

→ At low frequencies the response of transistor to changes of input Voltage & Current is instantaneous and hence we have neglected the effect of shunt Capacitances in the transistor. But this is not in case of high frequencies.

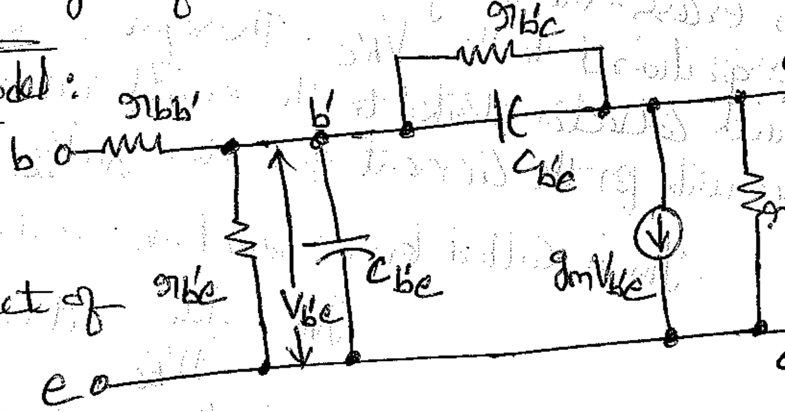
→ At low frequencies we analyze transistor using h-parameters. But for high frequency analysis the h-parameter model is not suitable for following reasons,

① The Values of h-parameters are not Constant at high frequencies. Therefore it is necessary to analyse transistor at each and every frequency, which is impracticable.

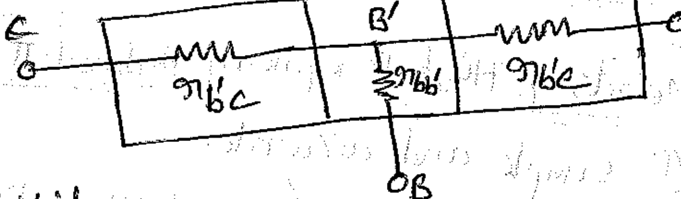
② At high frequency h-parameters become Complex in nature.

→ Due to above reasons hybrid π-model is used for high frequency analysis of the transistor. This model gives a reasonable Compromise between accuracy and simplicity to do high frequency analysis of the transistor.

Hybrid-π CE TransConductance Model:



① $C_{b'e}$: Forward biased PN junction exhibits a Capacitive effect Called the diffusion Capacitance. This Capacitive effect of normally forward biased base-emitter junction of the transistor is represented by $C_{b'e}$ or C_e in the hybrid-π model. Thus the diffusion Capacitance 'C_e' Connected between B' and E represents the excess minority Carrier storage in the base.



② $C_{b'c}$: The reverse bias PN junction exhibits a Capacitive effect Called the transition Capacitance. This Capacitive effect of normally reverse biased Collector base junction of the transistor is represented by $C_{b'c}$ or C_c in the hybrid π-model.

(3) $r_{bb'}$: The internal node b' is physically not accessible, bulk node B' represents external base terminal. The bulk resistance between external base terminal and internal node B' is represented as $r_{bb'}$. This resistance is called as base spreading resistance.

(4) $r_{b'e}$: The resistance $r_{b'e}$ is that portion of the base emitter which may be thought of as being "in series with" the collector junction. This establishes a virtual base B' for the junction capacitances to be connected to instead of b.

(5) $r_{b'c}$: Due to Early effect, the varying voltages across the collector to emitter junction results in base-width modulation. A change in the effective base width causes the emitter current to change. This feedback effect between output and input is taken into account by connecting $g_{b'c}$ or $r_{b'c}$ between b' and c.

(6) g_m : Due to small changes in voltage $V_{b'e}$ across the emitter junction, there is excess-minority carrier concentration injected into the base which is proportional to the $V_{b'e}$. Therefore, resulting small signal collector current with collector shorted to the emitter is also proportional to the $V_{b'e}$. This effect accounts for the current generator $g_m V_{b'e}$.

g_m is called transconductance and it is given as,

$$g_m = \frac{\Delta I_c}{\Delta V_{b'e}} \text{ at a constant } V_{CE}$$

(7) r_{ce} : The r_{ce} is the output resistance. It is also the result of early effect.

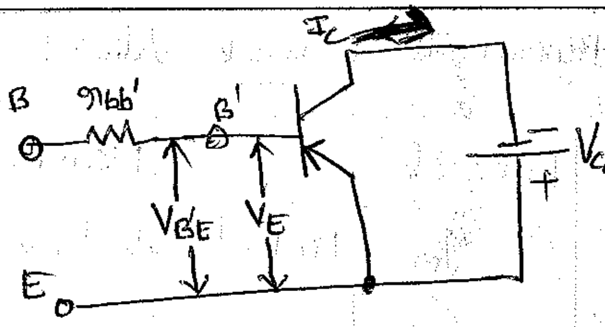
Merits of High Frequency Hybrid-π Model :

(1) Simple and accurate
(2) All parameters (resistances as well as capacitances) in the model are almost frequency invarient.
(3) The resistive components in the model may be derived from the low frequency h-parameters.

Hybrid-π parameter Values:

Parameter	Meaning	Value
① g_m	Mutual Conductance of transistor	50 mA/V
② $r_{bb'}$	Base spreading resistance	100 Ω
③ $r_{b'e}$ (or)	Resistance between B' and E	1 KΩ
$g_{b'e}$	Conductance between B' and E	1m mho
④ $r_{b'c}$	Resistance of reverse biased PN-junction between base and collector	4 MΩ
(or) $g_{b'c}$	Conductance of reverse biased PN-junction between base and collector	0.25×10^{-6} mho
⑤ r_{ce} (or)	output resistance between C and E	80 KΩ
g_{ce}	Conductance between C and E	12.5×10^{-6} mho
⑥ $C_{b'e}$ (or) C_e	Junction Capacitance between B and E	100 PF
⑦ $C_{b'c}$ (or) C_c	Junction Capacitance between base and collector	3 PF

Transistor Transconductance 'g_m':



$$g_m = \frac{\partial I_C}{\partial V_{B'E}}\bigg|_{V_{CE}} \quad \text{———} (1)$$

But $I_C = I_{CO} + \alpha I_E$

$\therefore \partial I_C = \alpha \partial I_E \quad \{\because I_{CO} = \text{Constant}\}$

$$(1) \Rightarrow g_m = \frac{\alpha \partial I_E}{\partial V_{B'E}} = \alpha \frac{\partial I_E}{\partial V_E} \quad \{\because V_E = V_{B'E}\} \quad \text{———} (2)$$

The emitter diode resistance r_e is given as,

$$r_e = \frac{\partial V_E}{\partial I_E} \rightarrow \frac{1}{r_e} = \frac{\partial I_E}{\partial V_E}$$

$$(2) \Rightarrow \quad g_m = \frac{\alpha}{r_e} \quad \text{———} (3)$$

Emitter diode is a forward biased diode and its dynamic resistance is,

$$r_e = V_T / I_E \quad \text{———} (4)$$

where $V_T = \frac{KT}{q}$ is Volt equivalent of temperature

'K' is Boltzmann Constant $(K = 1.38 \times 10^{-23}\ J/^\circ K)$

$q = 1.6 \times 10^{-19} C$ is electronic charge.

'T' is temperature in degree Kelvin

$$(3) \Rightarrow g_m = \frac{\alpha I_E}{V_T} = \frac{I_{CO} - I_C}{V_T}$$

For pnp transistor I_C is negative, for an npn transistor I_C is positive, but foregoing analysis (with $V_E = +V_{B'E}$) leads to $g_m = (I_C - I_{CO})/V_T$.

Hence for either type of transistor, g_m is positive.

$$\therefore g_m = \frac{I_C - I_{CO}}{V_T} \quad \text{———} (5)$$

$I_C \gg I_{CO}$,

$$\therefore g_m = \frac{I_C q}{KT} = \frac{I_C \times 1.6 \times 10^{-19}}{1.38 \times 10^{-23} T} = \frac{11{,}600\, I_C}{T} \quad \text{———} (6)$$

From equation (6) we can say that transconductance 'g_m' is directly proportional to collector current and inversely proportional to temperature.

At room temperature $T = 300^\circ K$

$$g_m = \frac{11600\, I_c}{300} = \frac{I_c}{26\times10^{-3}} = \frac{I_c\ mA}{26m} \quad \text{—— (7)}$$

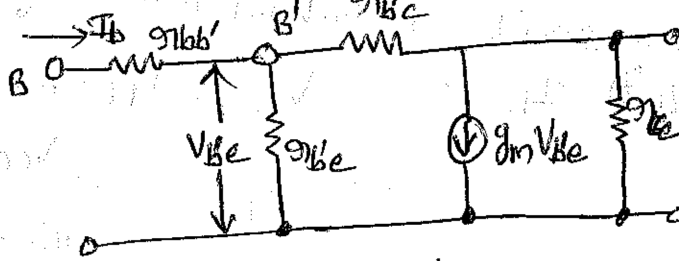


Fig (a) Hybrid π-model for CE configuration at low frequency

The Input Conductance $g_{b'e}$:

Consider the h-parameter model in fig (b).
Applying KCL to the output we get,

$$I_c = h_{fe} I_b + h_{oe}\cdot V_{ce}$$

Making $V_{ce} = 0$, i.e output short circuit, the short circuit current gain 'h_{fe}' is defined as,

$$h_{fe} = \frac{I_c}{I_b} \quad \text{—— (8)}$$

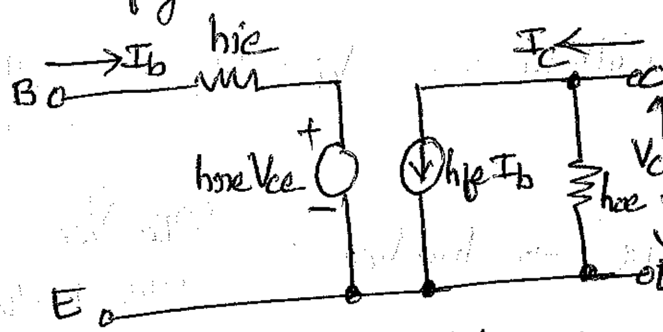


Fig (b) h-parameter model for CE configuration at low frequency

Now consider the hybrid-π model in fig (a).
As $r_{b'c} = 4M\Omega \gg r_{b'e}$ we get,

$V_{b'e} \approx I_b r_{b'e}$ and

$I_c = g_m V_{b'e}$

$$I_c = g_m I_b r_{b'e} \Rightarrow \frac{I_c}{I_b} = g_m r_{b'e} \quad \text{—— (9)}$$

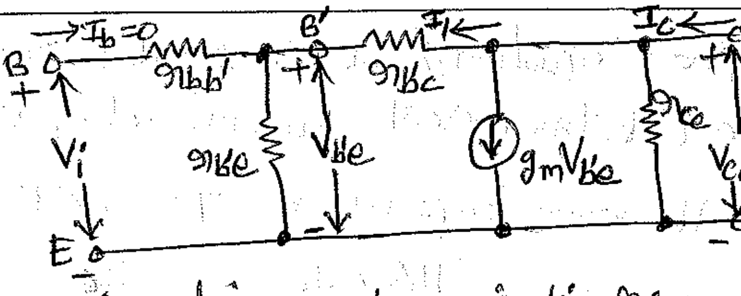
$\therefore$ (8) $\Rightarrow h_{fe} = g_m r_{b'e}$

$$\Rightarrow r_{b'e} = \frac{h_{fe}}{g_m} \quad (\text{or}) \quad g_{b'e} = \frac{g_m}{h_{fe}} \quad \text{—— (10)}$$

From eq (5) we know that $g_m = I_c / V_T$

$$\therefore r_{b'e} = \frac{h_{fe} V_T}{|I_c|} \quad (\text{or}) \quad g_{b'e} = \frac{|I_c|}{h_{fe} V_T} \quad \text{—— (11)}$$

The Feedback Conductance $g_{b'c}$:



Consider h-parameter model for CE Configuration with input open circuit i.e $I_b = 0$ So we get,

$$V_i = h_{re} V_{ce} \quad \text{—— (12)}$$

Now Consider the hybrid π-model for CE Configuration as shown in figure.

with $I_b = 0$, $V_{ce} = I_1 (r_{b'c} + r_{b'e})$

$$\Rightarrow I_1 = \frac{V_{ce}}{r_{b'c} + r_{b'e}} \quad \text{—— (13)}$$

Then, $V_{b'e} = I_1 r_{b'e} = r_{b'e} \cdot \dfrac{V_{ce}}{r_{b'c} + r_{b'e}}$ —— (14)

with $I_b = 0$, $V_i = V_{b'e} = \dfrac{r_{b'e} V_{ce}}{r_{b'c} + r_{b'e}}$

$$(12) \Rightarrow h_{re} V_{ce} = \frac{r_{b'e} V_{ce}}{r_{b'c} + r_{b'e}}$$

$$\Rightarrow h_{re} = \frac{r_{b'e}}{r_{b'c} + r_{b'e}}$$

$$\Rightarrow r_{b'e} = h_{re} r_{b'c} + h_{re} r_{b'e}$$

$$\Rightarrow (1 - h_{re}) r_{b'e} = h_{re} r_{b'c}$$

$$\therefore r_{b'c} = \left(\frac{1 - h_{re}}{h_{re}}\right) r_{b'e} \approx \frac{r_{b'e}}{h_{re}} \quad \text{—— (15)} \quad \{\because 1 - h_{re} \approx 1\}$$

$$\therefore g_{b'c} = \frac{h_{re}}{r_{b'e}} = h_{re}\, g_{b'e}$$

$$(11) \Rightarrow r_{b'c} = \frac{h_{fe} V_T}{|I_c|\, h_{re}} \quad (8) \quad g_{b'c} = \frac{|I_c|\, h_{re}}{h_{fe} V_T} \quad \text{—— (16)}$$

The Base Spreading Resistance $r_{bb'}$:

Consider h-parameter model for CE Configuration, with output shorted i.e V_{ce} input resistance is hie.

Consider hybrid-π model, with output shorted the input resistance is $r_{bb'} + r_{b'e}$.

$$\therefore h_{ie} = r_{bb'} + r_{b'e}$$

$$\Rightarrow r_{bb'} = h_{ie} - r_{b'e} \quad \text{---} \quad (17)$$

$$(11) \Rightarrow \quad r_{bb'} = h_{ie} - \frac{h_{fe} V_T}{I_C} \quad \text{---} \quad (18)$$

The output Resistance r_{ce}: the output Conductance is given as, using h-parameters

$$h_{oe} = \frac{I_c}{V_{ce}} \quad \text{---} \quad (19)$$

Now Consider hybrid-π model for CE Configuration.
Applying KCL to the output Circuit we get,

$$I_c = \frac{V_{ce}}{r_{ce}} + g_m V_{b'e} + I_1$$

$$(13) \Rightarrow \quad I_c = \frac{V_{ce}}{r_{ce}} + g_m V_{b'e} + \frac{V_{ce}}{r_{b'c} + r_{b'e}}$$

$$(14) \Rightarrow \quad I_c = \frac{V_{ce}}{r_{ce}} + g_m \frac{r_{b'e} V_{ce}}{r_{b'c} + r_{b'e}} + \frac{V_{ce}}{r_{b'c} + r_{b'e}}$$

$$\Rightarrow \frac{I_c}{V_{ce}} = \frac{1}{r_{ce}} + \frac{g_m r_{b'e} + 1}{r_{b'c} + r_{b'e}}$$

$$\frac{I_c}{V_{ce}} = \frac{1}{r_{ce}} + \frac{h_{fe} + 1}{r_{b'c} + r_{b'e}} \quad \text{---} \quad (20) \quad \{\because \text{eq} (10) \; h_{fe} = g_m r_{b'e}\}$$

$$\frac{I_c}{V_{ce}} \approx \frac{1}{r_{ce}} + \frac{h_{fe}}{r_{b'c} + r_{b'e}} \quad \{\because h_{fe} >> 1\} \quad \text{---} \quad (21)$$

$$(19) \Rightarrow \quad h_{oe} = \frac{1}{r_{ce}} + \frac{h_{fe}}{r_{b'c} + r_{b'e}} \quad \text{---} \quad (22)$$

$$\therefore h_{oe} = \frac{1}{r_{ce}} + \frac{h_{fe}}{r_{b'c}} \quad \left\{ \because r_{b'c} \gg r_{b'e} \right\} \quad \text{--- (23)}$$

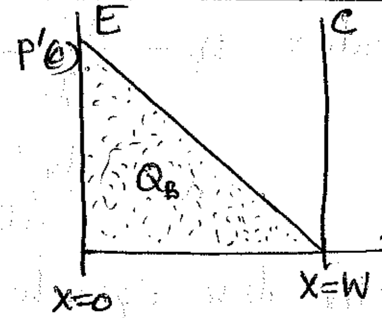
$$\therefore h_{oe} = g_{ce} + g_{b'c} h_{fe}$$

$$\therefore \frac{1}{r_{ce}} = g_{ce} = h_{oe} - g_{b'c} h_{fe} \quad \text{--- (24)}$$

Relation between hybrid-π and h-parameters :

S.NO	Parameter relation
1	$g_m = \frac{I_c}{V_T}$
2	$r_{b'e} = \frac{h_{fe}}{g_m}$
3	$r_{bb'} = h_{ie} - r_{b'e}$
4	$r_{b'c} = \frac{r_{b'e}}{h_{re}}$
5	$g_{ce} = \frac{1}{r_{ce}} = h_{oe} - g_{b'c} h_{fe}$

Hybrid π - Capacitances:



→ The transition capacitance $C_{b'c}$ or C_c is measured as a CB output capacitance with input open $I_E = 0$ and is usually specified by manufacturers as C_{ob}.

→ The diffusion capacitance is represented by $C_{b'e}$ or C_e is the summation of the emitter junction capacitance C_{Te} and the emitter diffusion capacitance C_{De}.

→ For a forward biased emitter junction, C_{De} is usually much larger than C_{Te}

$$\therefore \; C_e = C_{De} + C_{Te} \approx C_{De}.$$

The above figure shows the minority carriers charge distribution in the base region. It gives the injected hole concentration versus distance in the base region of a pnp transistor.

→ The base width 'W' is assumed to be small compared with the diffusion length L_B of the minority carriers. Since the collector junction is reverse biased, the injected charge concentration p' at the collector junction is zero.

→ If $W \ll L_B$, the p' varies almost linearly from the value $P'(0)$ at the emitter to zero at the collector.

The stored base charge Q_B can be given as, $Q_B = \frac{1}{2} P'(0) AWq$ — ①

where $\frac{1}{2} P'(0)$ is the average concentration

'A' is the base cross sectional area

WA is the volume of the base

q is the electronic charge

D_B is diffusion constant $= \mu_p V_T$
where μ_p is mobility of charge carriers (i.e holes in this case) and $V_T = \frac{T}{11600}$

$\frac{dp'}{dx}$ is carriers concentration gradient

$$\frac{dp'}{dx} = \frac{0 - P'(0)}{W - 0} = -\frac{P'(0)}{W}$$

The diffusion current is given by,

$$I = -Aq D_B \frac{dp'}{dx} \approx Aq D_B \frac{P'(0)}{W} \quad \text{— ②}$$

$$① \Rightarrow Q_B = \frac{1}{2} P'(0) AWq = \frac{\cancel{A}W\cancel{q}}{2} \times \frac{IW}{\cancel{Aq} D_B} = \frac{IW^2}{2D_B} \quad \text{— ③}$$

The static emitter diffusion capacitance C_{De} is defined as the rate of change of Q_B with respect to emitter voltage 'V'.

$$\therefore C_{De} = \frac{dQ_B}{dV} = \frac{W^2}{2D_B} \times \frac{dI}{dV} = \frac{W^2}{2D_B} \cdot \frac{1}{r_e} \quad \text{— ④}$$

where $r_e = \frac{dV}{dI} = \frac{V_T}{I_E}$ is the emitter junction incremental resistance.

$$C_{De} = \frac{W^2}{2D_B} \cdot \frac{I_E}{V_T} = g_m \frac{W^2}{2D_B} \quad \text{—— (5)}$$

The above equation indicates that the diffusion capacitance is proportional to the emitter bias current I_E.

Experimentally C_e is determined from a measurement of f_T, the frequency at which the CE-short circuit current gain drops to unity

i.e $C_e \approx \frac{g_m}{2\pi f_T}$.

Variation of Hybrid-π parameters with I_c, V_{CE} and temperature:

SNO	Parameter	$\lvert I_c \rvert$	$\lvert V_{CE} \rvert$	Temperature 'T'
1.	g_m	Increases, proportional to $\lvert I_c \rvert$.	Independent	Decreases, inversely proportional to 'T'.
2.	$r_{bb'}$	Decreases due to conductivity modulation of the base.		Increases due to decrease in conductivity as a result of decrease in mobility of majority & minority carriers
3.	$r_{b'e}$	Decreases, inversely proportional to $\lvert I_c \rvert$.	Increases	Increases
4.	$C_{b'e}$ (or) C_e	Increases, proportional to $\lvert I_c \rvert$	Decreases.	
5.	$C_{b'c}$ (or) C_c	Independent	Decreases	Independent
6.	h_{fe} r_{bc}	Increases for smaller values of $\lvert I_c \rvert$ and decreases with higher values of $\lvert I_c \rvert$	Increases due to increase of transistor 'α' as a result of decrease of the base width and the reduction in recombination	Increases.
7.	h_{ie} & r_{ce}	Decreases, inversely proportional to $\lvert I_c \rvert$.	Increases	Increases.

CE short Circuit Current Gain:

Consider a single stage CE transistor amplifier with load resistor R_L as shown in figure ⓐ.

For the analysis of short circuit current gain we have to assume $R_L = 0$. with $R_L = 0$ i.e output short circuited r_{ce} becomes zero, $r_{b'e}$, C_e and C_c appear in parallel. As $r_{b'c} \gg r_{b'e}$, $r_{b'c}$ is neglected.

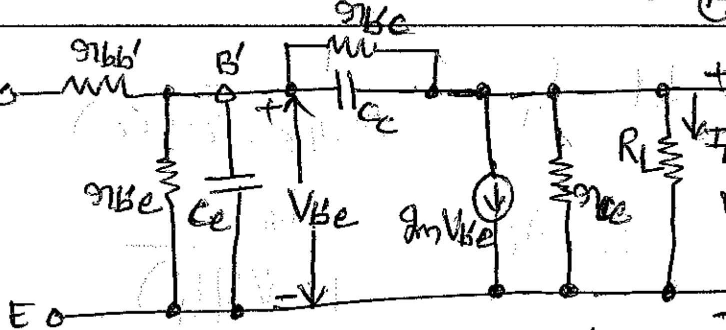


Fig ⓐ Hybrid-π Circuit for a single transistor with a resistive load R_L.

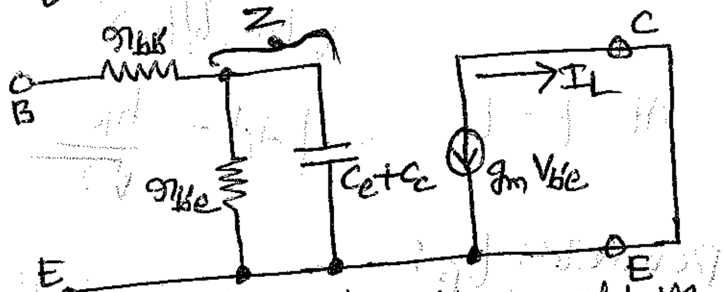


Fig ⓑ simplified hybrid π-model for short circuit CE transistor.

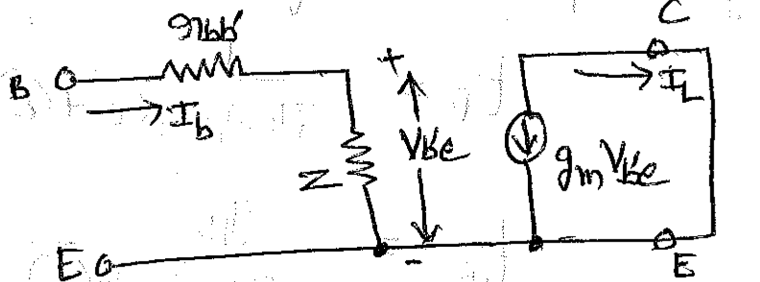


Fig ⓒ Further simplified hybrid-π model.

$$Z = r_{b'e} \parallel \frac{1}{j\omega(C_e+C_c)}$$

$$Z = \frac{r_{b'e} \times \frac{1}{j\omega(C_e+C_c)}}{r_{b'e} + \frac{1}{j\omega(C_e+C_c)}}$$

$$Z = \frac{r_{b'e}}{1 + j\omega r_{b'e}(C_e+C_c)}$$

$$\therefore V_{b'e} = I_b Z$$

$$\Rightarrow Z = \frac{V_{b'e}}{I_b}$$

$$A_i = \frac{I_L}{I_b} = \frac{-g_m V_{b'e}}{I_b} \quad \left\{ \because I_L = -g_m V_{b'e} \right\}$$

$$A_i = -g_m Z = \frac{-g_m r_{b'e}}{1 + j\omega r_{b'e}(C_e+C_c)}$$

$$A_i = \frac{-h_{fe}}{1 + j\omega r_{b'e}(C_e+C_c)} \quad \left\{ \because h_{fe} = g_m r_{b'e} \right\}$$

The above equation signifies that current is not constant as it depends on frequency. when frequency is small, $j\omega r_{b'e}(C_e+C_c) \ll 1$ and hence $A_i = -h_{fe}$. But as frequency increases A_i reduces as shown in figure ⓓ

Let $f_\beta = \dfrac{1}{2\pi r_{b'e}(C_e + C_c)}$

$$\therefore A_i = \frac{-h_{fe}}{1 + j(f/f_\beta)}$$

$$|A_i| = \frac{h_{fe}}{\sqrt{1 + (f/f_\beta)^2}}$$

At $f = f_\beta$, $|A_i| = \dfrac{h_{fe}}{\sqrt{2}}$

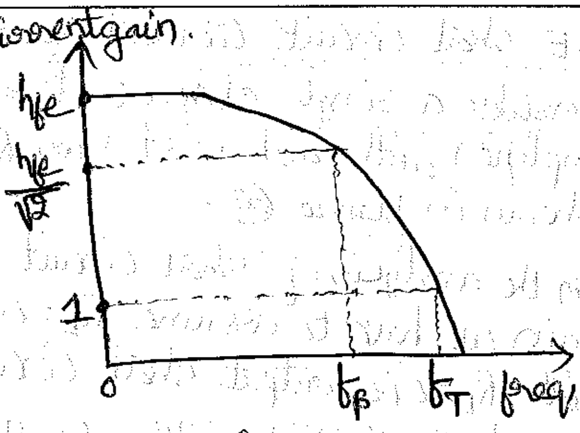


Figure ①.

Parameter f_β:

→ It is the frequency at which the transistors short circuit CE current gain drops by 3dB or $\frac{1}{\sqrt{2}}$ times from its value at low frequency.

$$f_\beta = \frac{1}{2\pi r_{b'e}(C_e + C_c)}$$

$$f_\beta = \frac{g_{b'e}}{2\pi (C_e + C_c)}$$

$$\boxed{f_\beta = \frac{g_m}{2\pi h_{fe}(C_e + C_c)}} \qquad \left\{ \because g_{b'e} = \frac{1}{r_{b'e}} = \frac{g_m}{h_{fe}} \right\}$$

Parameter f_α:

→ It is the frequency at which the transistor's short circuit CB current gain drops by 3dB or $\frac{1}{\sqrt{2}}$ times from its value at low frequency.

The current gain for CB configuration is,

$$A_i = \frac{-h_{fb}}{1+j(f/f_\alpha)}$$

where,
$$f_\alpha = \frac{1}{2\pi r_{b'e}(1+h_{fb})C_e}$$

$$f_\alpha = \frac{1+h_{fe}}{2\pi r_{b'e}C_e} \qquad \left\{\because 1+h_{fb} = \frac{1}{1+h_{fe}}\right\}$$

$$\boxed{f_\alpha \approx \frac{h_{fe}}{2\pi r_{b'e}C_e} \approx \frac{g_m}{2\pi C_e}} \qquad \left\{\because r_{b'e} = \frac{h_{fe}}{g_m}\right\}$$

At $f = f_\alpha$, $|A_i| = h_{fb}/\sqrt{2}$.

Parameter f_T:

It is the frequency at which short circuit CE current gain becomes unity.

$$|A_i| = \frac{h_{fe}}{\sqrt{1+(f/f_\beta)^2}}$$

At $f = f_T$ $|A_i| = 1$

$$\therefore 1 = \frac{h_{fe}}{\sqrt{1+(f_T/f_\beta)^2}} \qquad \{\because f_T/f_\beta \gg 1\}$$

$$\Rightarrow 1 = h_{fe}/(f_T/f_\beta)$$

$$\Rightarrow \boxed{f_T = h_{fe}f_\beta}$$

$$\therefore f_T = h_{fe} \times \frac{g_m}{2\pi h_{fe}(C_e + C_c)}$$

$$\boxed{f_T = \frac{g_m}{2\pi(C_e + C_c)}}$$

Since $C_e >> C_c$

$$\therefore \boxed{f_T \approx \frac{g_m}{2\pi C_e}}$$

prob: At $I_c = 1\,mA$ and $V_{CE} = 10V$ a certain transistor data shows $C_c = C_{b'c} = 3pF$, $h_{fe} = 200$ and $\omega_T = 500\,M\,rad/sec$. Calculate g_m, $r_{b'e}$, $C_e = C_{b'e}$ and ω_β. Assume room temperature.

soln: $g_m = \frac{I_c}{V_T} = \frac{I_c\,mA}{26m} = \frac{1 \times 10^{-3}}{26 \times 10^{-3}} = 38.46\,m\,A/V$

$$r_{b'e} = \frac{h_{fe}}{g_m} = \frac{200}{38.46 \times 10^{-3}} = 5.2K\Omega$$

$$C_e + C_c = \frac{g_m}{2\pi f_T} = \frac{g_m}{\omega_T} = \frac{38.46 \times 10^{-3}}{500 \times 10^{6}} = 76.92\,pF$$

$$\therefore C_e = 76.92 \times 10^{-12} - 3 \times 10^{-12} = 73.92\,pF$$

$$f_T = h_{fe} f_\beta$$

$$2\pi f_T = h_{fe} \times 2\pi f_\beta$$

$$\Rightarrow \omega_T = h_{fe}\,\omega_\beta$$

$$\Rightarrow \omega_\beta = \frac{\omega_T}{h_{fe}} = \frac{500 \times 10^{6}}{200} = 2.5\,M\,rad/sec.$$

Current Gain with Resistive Load:

Consider a single stage CE transistor amplifier with load resistance R_L as shown in fig (a).

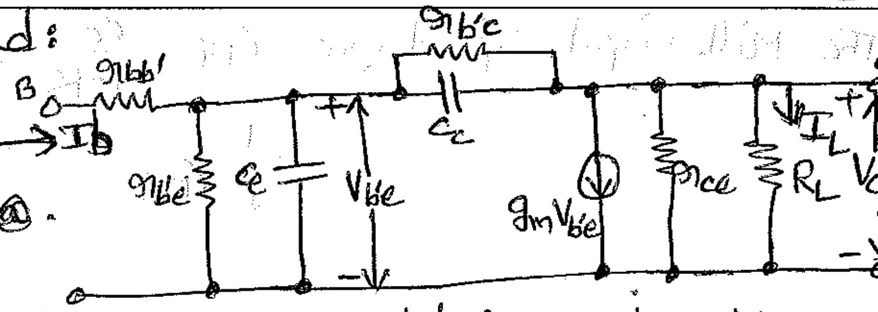


Fig (a) Hybrid π-model for a CE transistor with resistive load.

In the output circuit r_{ce} is in parallel with R_L, for high frequency amplifiers R_L is small as compared to r_{ce} and hence we can neglect r_{ce}. Using Miller's theorem, we can split $r_{b'c}$ and C_c to simplify the analysis. Fig (b) shows the simplified hybrid-π model for a single transistor with resistive load.

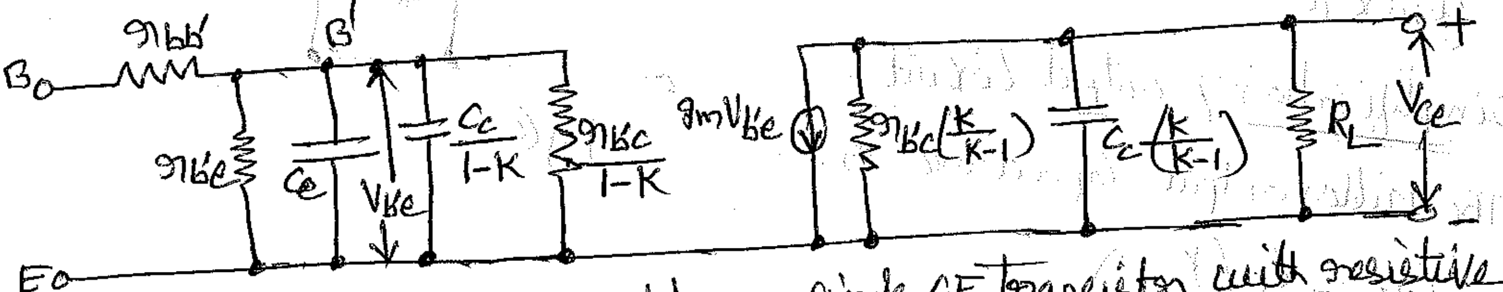


Fig (b) Simplified Hybrid-π model for a single CE transistor with resistive load.

Simplification of Input Circuit:

Amplifier's gain K is given as, $K = \frac{V_o}{V_{b'e}}$

But $V_o = -g_m V_{b'e} R_L$

$\therefore K = -g_m R_L$

Let $R_L = 2K\Omega$ and $g_m = 50mA/V$ then we get $K = -100$

and $\frac{r_{b'c}}{1-K} = \frac{4M\Omega}{1-(-100)} \approx 40K\Omega$

$\therefore$ The value of $\frac{r_{b'c}}{1-K} \gg r_{b'e}\,(1K\Omega)$ and hence $\frac{r_{b'c}}{1-K}$ which is in parallel with $r_{b'e}$ can be neglected.

The Miller input capacitance $C_{Mi} = \frac{C_c}{1-K} =$

$$\frac{1}{j\omega C_{Mi}} = \frac{\frac{1}{j\omega C_c}}{1+g_m R_L} \qquad \left\{\because K = -g_m R_L\right\}$$

$$\Rightarrow C_{Mi} = \frac{C_c}{1-K} = C_c(1+g_m R_L)$$

As C_e and C_{Mi} are in parallel, the total equivalent capacitance is,

$$C_{eq} = C_e + C_{Mi} = C_e + C_c(1+g_m R_L)$$

With these approximations the input circuit becomes as shown in figure ©.

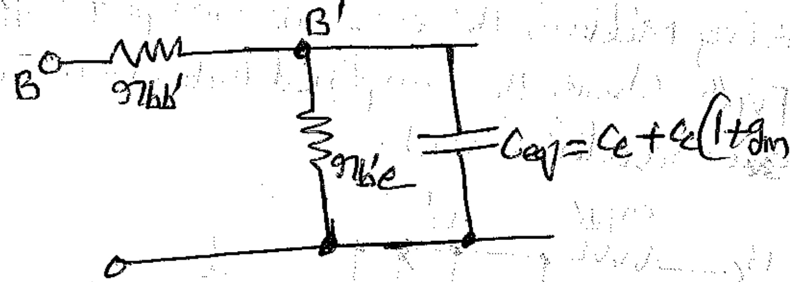


Fig ©.

Simplification of output circuit:

The Miller output capacitance is,

$$C_{Mo} = C_c\left(\frac{K}{K-1}\right)$$

$$\frac{1}{j\omega C_{Mo}} = \frac{1}{j\omega C_c} \times \left(\frac{K}{K-1}\right)$$

As $K = -100$ then $\frac{K}{K-1} \approx 1$

$$\therefore C_{Mo} \approx C_c$$

Looking at figure ⓐ we can say that there are two independent time constants one associated with the input circuit and one associated with the output circuit. As input capacitance $[C_e + C_c(1+g_m R_L)]$ is very high in comparision with output capacitance C_c. As a result, output time constant is negligible in comparision with the input time constant and may be ignored.

$$r_{b'c}\left(\frac{K}{K-1}\right) \approx r_{b'c} \approx 4M\Omega$$

This value of $r_{b'c}$ is very high in comparision with load resistance R_L which is parallel with $r_{b'c}$. Hence $r_{b'c}$ can be neglected.

Figure (d) shows further simplified hybrid-π model of single transistor in CE configuration with load resistance.

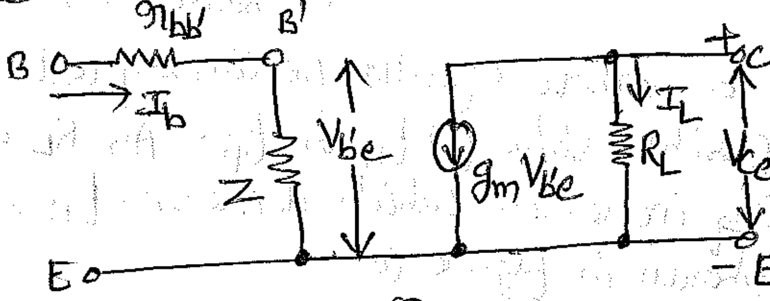


Fig (d)

where, $Z = r_{b'e} \| X_{C_{eq}}$.

$$Z = \frac{r_{b'e} \times \frac{1}{j\omega C_{eq}}}{r_{b'e} + \frac{1}{j\omega C_{eq}}}$$

$$Z = \frac{r_{b'e}}{1 + j\omega r_{b'e} C_{eq}}$$

Now, $V_{b'e} = I_b Z \Rightarrow Z = \frac{V_{b'e}}{I_b}$

Current gain, $A_i = \frac{I_L}{I_b} = \frac{-g_m V_{b'e}}{I_b}$ $\quad \left\{\because I_L = -g_m V_{b'e}\right\}$

$$A_i = -g_m Z \quad \left\{\because Z = \frac{V_{b'e}}{I_b}\right\}$$

$$\therefore A_i = \frac{-g_m r_{b'e}}{1 + j\omega r_{b'e} C_{eq}} = \frac{-h_{fe}}{1 + j 2\pi f r_{b'e} C_{eq}} \quad \left\{\because h_{fe} = g_m r_{b'e}\right\}$$

Let $f_H = \frac{1}{2\pi r_{b'e} C_{eq}}$

$$\therefore A_i = \frac{-h_{fe}}{1 + j(f/f_H)} \Rightarrow |A_i| = \frac{h_{fe}}{\sqrt{1 + (f/f_H)^2}}$$

At $f = f_H$, $|A_i| = \frac{h_{fe}}{\sqrt{2}}$

Therefore f_H is the frequency at which the transistors gain drops by 3dB or $\frac{1}{\sqrt{2}}$ times from its value at low frequency.

$$\therefore f_H = \frac{1}{2\pi r_{b'e} C_{eq}} = \frac{1}{2\pi r_{b'e}\left[C_e + C_c(1 + g_m R_L)\right]}$$

At $R_L = 0$, $f_H = \frac{1}{2\pi r_{b'e}(C_e + C_c)} = \frac{1}{f_\beta}$

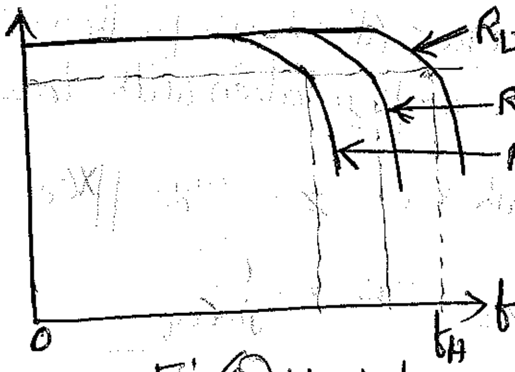


Fig (e) Variation of f_H with R_L.

From above equation we can say that maximum possible value for f_H is f_β. As R_L increases C_{eq} increases which decreases f_H as shown in figure (e).

Current Gain Including Source Resistance:

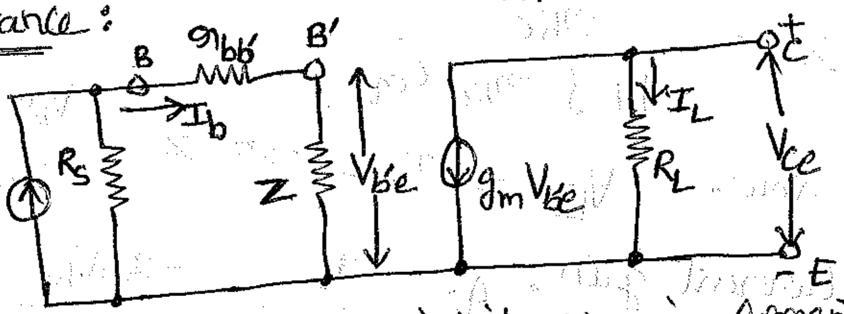


Fig (a) Equivalent circuit assuming current source

$$A_{IS} = \frac{I_L}{I_S} = \frac{I_L}{I_b} \cdot \frac{I_b}{I_S}$$

where $\frac{I_b}{I_S} = \frac{R_S}{R_S + r_{bb'} + Z}$

$$\therefore A_{is} = \frac{-g_m Z R_S}{R_S + r_{bb'} + Z} \quad \left\{ \because \frac{I_L}{I_b} = -g_m Z \right\}$$

where $Z = \frac{r_{b'e}}{1 + j\omega r_{b'e} C_{eq}}$

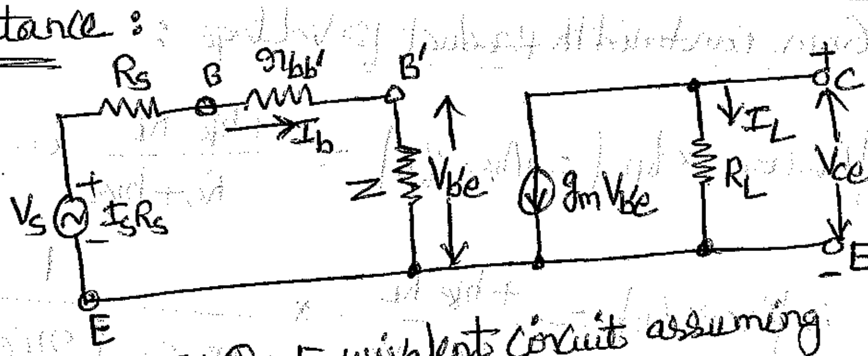
At low frequency we can neglect the capacitance and hence 'Z' is given as,

$$Z = r_{b'e}$$

$$\therefore A_{is(low)} = \frac{-g_m r_{b'e} R_S}{R_S + r_{bb'} + r_{b'e}} = \frac{-h_{fe} R_S}{R_S + r_{bb'} + r_{b'e}} \quad \{ \because h_{fe} = g_m r_{b'e} \}$$

$$A_{is(low)} = \frac{-h_{fe} R_S}{R_S + h_{ie}} \quad \{ \because h_{ie} = r_{bb'} + r_{b'e} \}$$

Voltage Gain Including Source Resistance :



Fig(b): Equivalent Circuit assuming Voltage Source

$$A_{Vs} = \frac{V_o}{V_s} = \frac{I_L R_L}{I_s R_s}$$

But $\frac{I_L}{I_s} = \frac{-g_m Z R_s}{R_s + r_{bb'} + Z}$

$$\therefore A_{Vs} = \frac{-g_m Z R_s}{R_s + r_{bb'} + Z} \times \frac{R_L}{R_s}$$

$$A_{Vs} = \frac{-g_m Z R_L}{R_s + r_{bb'} + Z}$$

At low frequency we can neglect the capacitance and hence $Z = r_{b'e}$

$$\therefore A_{Vs}(low) = \frac{-g_m r_{b'e} R_L}{R_s + r_{bb'} + r_{b'e}}$$

$$\therefore A_{Vs}(low) = \frac{-h_{fe} R_L}{R_s + h_{ie}} \qquad \left\{ \because h_{fe} = g_m r_{b'e},\; h_{ie} = r_{bb'} + r_{b'e} \right\}$$

The Cut-off frequency Including Source Resistance :

$$f_H = \frac{1}{2\pi R_{eq} \cdot C_{eq}}$$ where $R_{eq} = r_{b'e} \| (r_{bb'} + R_s)$

$C_{eq} = C_e + C_c(1 + g_m R_L)$

f_H increases as the load resistance is decreased because C_{eq} is proportional to R_L.

For $R_L = 0$,

$$f_H = \frac{1}{2\pi R_{eq}(C_e + C_c)}$$

$$f_H = \frac{f_T}{g_m R_{eq}} \qquad \left\{ \because f_T = \frac{g_m}{2\pi(C_e + C_c)} \right\}$$

$$f_H = \frac{h_{fe} f_\beta}{g_m R_{eq}} \qquad \left\{ \because f_T = h_{fe} f_\beta \right\}$$

$$f_H = \frac{f_\beta}{g_{b'e} R_{eq}} \qquad \left\{ \because g_{b'e} = \frac{1}{r_{b'e}} = \frac{g_m}{h_{fe}} \right\}$$

Gain Bandwidth product for Voltage :

$$|A_{vs(low)} \times f_H| = |A_{vso} \times f_H| = \frac{+h_{fe} R_L}{R_s + h_{ie}} \times \frac{1}{2\pi R_{eq} C_{eq}}$$

$$\therefore |A_{vso} \times f_H| = \frac{+h_{fe} R_L}{R_s + h_{ie}} \times \frac{1}{2\pi C_{eq} \left[\frac{r_{b'e}(r_{bb'} + R_s)}{r_{b'e} + r_{bb'} + R_s}\right]} \quad \left\{\because R_{eq} = r_{b'e} \| R_s + r_{bb'}\right.$$

$$= \frac{h_{fe} R_L}{R_s + h_{ie}} \times \frac{R_s + h_{ie}}{2\pi C_{eq} r_{b'e}(r_{bb'} + R_s)} \quad \left\{\because r_{b'e} + r_{bb'} = h_{ie}\right.$$

$$= \frac{g_m \cancel{r_{b'e}} R_L}{2\pi C_{eq} \cancel{r_{b'e}}(r_{bb'} + R_s)} \quad \left\{\because h_{fe} = g_m r_{b'e}\right\}$$

$$= \frac{g_m R_L}{2\pi C_{eq}(r_{bb'} + R_s)}$$

$$= \frac{g_m R_L}{R_s + r_{bb'}} \times \frac{1}{2\pi[C_e + C_c(1 + g_m R_L)]}$$

$$= \frac{g_m R_L}{R_s + r_{bb'}} \times \frac{1}{2\pi[C_e + C_c \cdot g_m R_L]} \quad \left\{\because g_m R_L \gg 1\right\}$$

$$= \frac{R_L}{R_s + r_{bb'}} \times \frac{2\pi f_T C_e}{2\pi[C_e + C_c \cdot 2\pi f_T C_e R_L]} \quad \left\{\because g_m = 2\pi f_T C_e\right.$$

$$|A_{vso} \times f_H| = \frac{R_L}{R_s + r_{bb'}} \times \frac{f_T}{1 + 2\pi f_T C_c R_L}$$

Gain Bandwidth product for Current:

$$|A_{i}(low) \times f_H| = |A_{iso} \times f_H| = \frac{h_{fe} R_s}{R_s + h_{ie}} \times \frac{1}{2\pi R_{eq} C_{eq}}$$

$$\Rightarrow |A_{iso} \times f_H| = \frac{R_s}{R_s + r_{bb'}} \times \frac{f_T}{1 + 2\pi f_T C_c R_L} \approx \frac{g_m R_s}{2\pi C_{eq}(R_s + r_{bb'})}$$

→ The quantities f_H, A_{iso} and A_{vso} which characterize the transistor stage depend on both R_L and R_s.

→ For any R_L the bandwidth is highest for lowest R_s.

→ The Voltage gain bandwidth product increases with increasing R_L and decreases with increasing R_s.

→ Therefore we can say that the gain bandwidth product is not Constant but it depends on Values of R_L and R_s.

prob ①: A high frequency amplifier uses a transistor which is driven from a source with $R_s = 1K$. Calculate Value of f_H, A_{vso} and A_{iso} if $R_L = 0$ and $R_L = 1K\Omega$. Assume $r_{b'e} = 1K\Omega$, $r_{bb'} = 100\Omega$, $C_e = 100pF$, $C_c = 3pF$ and $g_m = 50\,mA/V$.

Soln:

ⓐ For $R_L = 0$, $\quad f_H = \frac{1}{2\pi R_{eq}(C_e + C_c)}$

$$R_{eq} = r_{b'e} \| (r_{bb'} + R_s) = 1K \| (100 + 1K) = 523.8\,\Omega$$

$$\therefore f_H = \frac{1}{2\pi \times 523.8 \times (100 \times 10^{-12} + 3 \times 10^{-12})} = 2.95\,MHz$$

$$A_{vso} = \frac{-h_{fe} R_L}{R_s + h_{ie}} = 0 \quad \{\because R_L = 0\}$$

$$A_{iso} = \frac{-h_{fe} R_s}{R_s + h_{ie}} = \frac{-g_m r_{b'e} R_s}{R_s + r_{b'e} + r_{bb'}} = \frac{-50 \times 10^{-3} \times 10^3 \times 10^3}{10^3 + 10^3 + 100}$$

$$A_{iso} = -23.8$$

(b) For $R_L = 1K\Omega$

$$f_H = \frac{1}{2\pi R_{eq} C_{eq}}$$

$$R_{eq} = r_{b'e} \| (r_{bb'} + R_S) = 523.8\,\Omega$$

$$C_{eq} = C_e + C_c(1 + g_m R_L)$$

$$= 100\times10^{-12} + 3\times10^{-12}(1 + 50\times10^{-3}\times10^{3})$$

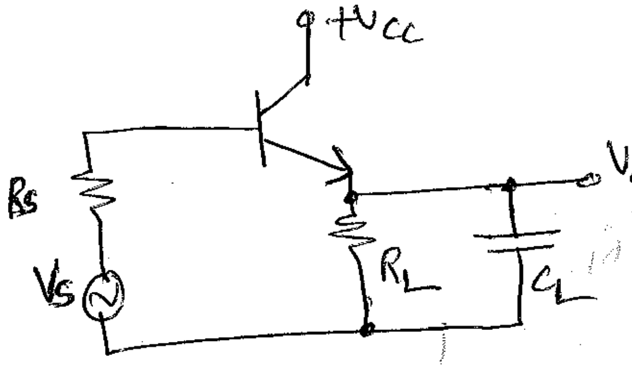
$$C_{eq} = 0.253\,nF$$

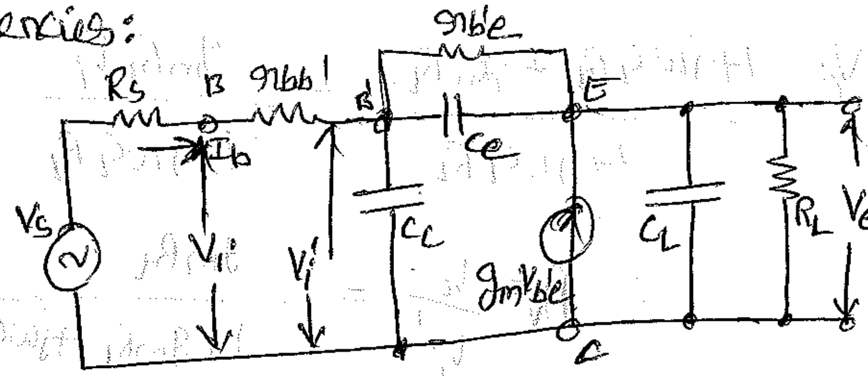
$$\therefore f_H = \frac{1}{2\pi R_{eq}\cdot C_{eq}} = \frac{1}{2\pi\times 523.8\times 0.253\times10^{-9}} = 1.2\,MHz$$

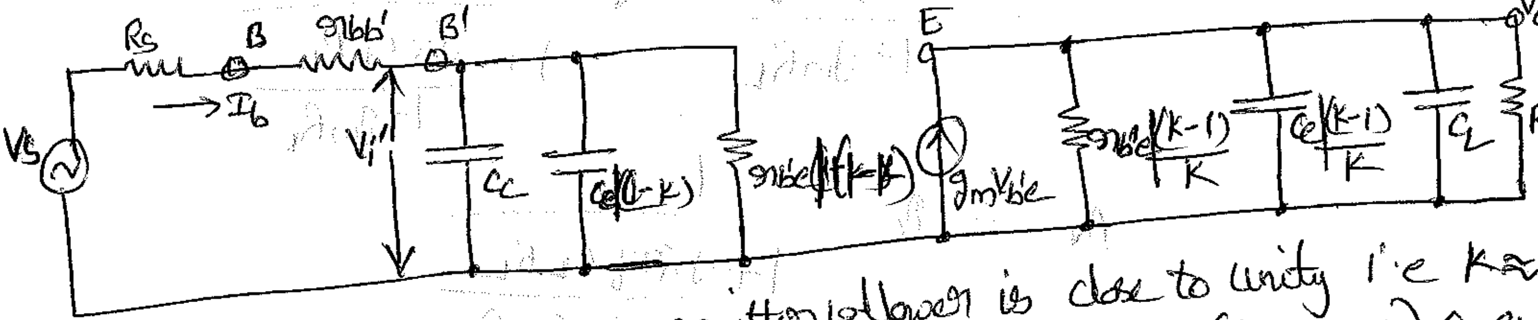
$$A_{Vso} = \frac{-h_{fe} R_L}{R_S + h_{ie}} = \frac{-g_m r_{b'e} R_L}{R_S + r_{bb'} + r_{b'e}} = -23.8$$

$$A_{iso} = \frac{-h_{fe} R_S}{R_S + h_{ie}} = \frac{-g_m r_{b'e} R_S}{R_S + r_{bb'} + r_{b'e}} = -23.8$$

Emitter Follower at High Frequencies:







The low frequency gain of an emitter follower is close to unity i.e $K \approx$ 1 and hence $1-K=0$. Therefore input time constant $\tau_i \approx (R_S + r_{bb'}) C_c$ and the output time constant is proportional to C_L. Since load is highly capacitive $\tau_0 >> \tau_i$ and hence we can determine the upper 3dB frequency considering only output circuit.

$$V_e = g_m V_{b'e} \times \left(R_L \| \frac{1}{j\omega C_L}\right)$$

$$V_e = \frac{g_m V_{b'e} R_L}{1 + j\omega C_L R_L}$$

$$= \frac{g_m (V_i' - V_e) R_L}{1 + j\omega C_L R_L}$$

$$V_e = \frac{g_m R_L V_i'}{1 + j\omega C_L R_L} - \frac{g_m R_L V_e}{1 + j\omega C_L R_L}$$

$$V_e \left[1 + \frac{g_m R_L}{1 + j\omega C_L R_L}\right] = \frac{g_m R_L V_i'}{1 + j\omega C_L R_L}$$

$$V_o \frac{1+j\omega C_L R_L + g_m R_L}{1+j\omega C_L R_L} = \frac{g_m R_L V_i'}{1+j\omega C_L R_L}$$

$$\therefore A_V = \frac{V_o}{V_i'} = \frac{g_m R_L}{1+g_m R_L + j\omega C_L R_L}$$

$$= \frac{g_m R_L}{1+g_m R_L} * \frac{1}{1+\frac{j\omega C_L R_L}{1+g_m R_L}}$$

$$A_V = A_0 \cdot \frac{1}{1+j\frac{2\pi f C_L R_L}{1+g_m R_L}}$$

where $A_0 = \frac{g_m R_L}{1+g_m R_L} \approx 1$

$$\therefore A_V = A_0 \cdot \frac{1}{1+j(f/f_H)}$$

where $f_H = \frac{1+g_m R_L}{2\pi C_L R_L} \approx \frac{g_m R_L}{2\pi C_L R_L} \approx \frac{g_m}{2\pi C_L} \approx \frac{f_T C_e}{C_L}$

$$\therefore f_T = \frac{g_m}{2\pi C_e}$$

$$\therefore f_H = \frac{1}{2\pi \tau_0}$$ where $\tau_0 = C_L / g_m$.

prob①: For a BJT amplifier the following values are known,
$T = 300^\circ K$, $I_{CQ} = 2mA$, $r_{bb'} = 100\Omega$, $r_{b'e} = 1000\Omega$, $r_{b'c} = 2M\Omega$, $r_{ce} = 80K\Omega$
$C_{b'e} = 200pF$, $C_{b'c} = 3pF$, $f_T = 50MHz$. obtain the h-parameters if
$K = 1.381 \times 10^{-23} J/^\circ K$ and $q = 1.6 \times 10^{-19} C$.

1) $g_m = |I_c| / V_T$
2) $r_{b'e} = h_{fe} / g_m$
3) $r_{bb'} = h_{ie} - r_{b'e}$
4) $r_{b'c} = r_{b'e} / h_{re}$
5) $g_{ce} = h_{oe} - g_{b'c} h_{fe}$

Soln: $g_m = \frac{|I_c|}{V_T}$ where $V_T = \frac{KT}{q} = 26m$

$g_m = \frac{2 \times 10^{-3}}{26 \times 10^{-3}} = 77 \; mA/V$

$h_{fe} = r_{b'e} g_m = 1000 \times 77 \times 10^{-3} = 77$

$h_{ie} = r_{bb'} + r_{b'e} = 100 + 1000 = 1.1K\Omega$

$h_{re} = \frac{r_{b'e}}{r_{b'c}}$ $\left\{ \because r_{b'c} = \frac{r_{b'e}}{h_{re}} \right\}$

$h_{re} = \frac{1000}{2 \times 10^{6}} = 5 \times 10^{-4}$

$h_{oe} = g_{ce} + (h_{fe}) g_{b'c} = \frac{1}{80 \times 10^3} + \frac{(77)}{2 \times 10^6} = 51 \times 10^{-6} \; A/V$

prob②: A BJT has the following parameters measured at $I_c = 1mA$, $h_{ie} = 3K\Omega$
$h_{fe} = 100$, $f_T = 4MHz$, $C_c = 2pF$ and $C_e = 18pF$. Find $r_{b'e}$, $r_{bb'}$, g_m and f_H
for $R_L = 1K\Omega$.

Soln: $g_m = \frac{|I_c|}{V_T} = \frac{1 \times 10^{-3}}{26 \times 10^{-3}} = 38.46 \; mA/V$

$g_m r_{b'e} = h_{fe} \Rightarrow r_{b'e} = \frac{h_{fe}}{g_m} = \frac{100}{38.46 \times 10^{-3}} = 2.6K\Omega$

$r_{bb'} + r_{b'e} = h_{ie} \Rightarrow r_{bb'} = h_{ie} - r_{b'e}$

$r_{bb'} = 3 \times 10^3 - 2.6 \times 10^3 = 400\Omega$

$f_H = \frac{1}{2\pi R_{eq} C_{eq}}$

$R_{eq} = r_{b'e}$ $\left\{ \because R_s = 0 \text{. If } R_s \text{ is finite then } R_{eq} = r_{b'e} \| (R_s + r_{bb'}) \right.$

$C_{eq} = C_e + C_c(1 + g_m R_L)$

$= 18 \times 10^{-12} + 2 \times 10^{-12} [1 + 38.46 \times 10^{-3} \times 10^3]$

$C_{eq} = 96.92 pF$

$\therefore f_H = 637.64 KHz$

prob③: For a single stage CE amplifier whose hybrid-π parameters are $g_m = 50\,mA/V$, $r_{bb'} = 100\,\Omega$, $r_{b'e} = 1K\Omega$, $C_c = 3\,pF$, $C_e = 100\,pF$, what value of R_s will give 3dB freq. f_H which is half the value obtained with $R_s = 0$.

Soln:
$$f_H' = \frac{f_H}{2} \Rightarrow \frac{1}{2\pi R_{eq}' C_{eq}} = \frac{1}{2 \times 2\pi R_{eq} \cdot C_{eq}}$$

$$\Rightarrow R_{eq}' = 2 R_{eq}.$$

$R_{eq}' = r_{b'e} \,\|\, (r_{bb'} + R_s)$, but $R_s = 0$ $R_{eq} = r_{b'e} \,\|\, r_{bb'}$

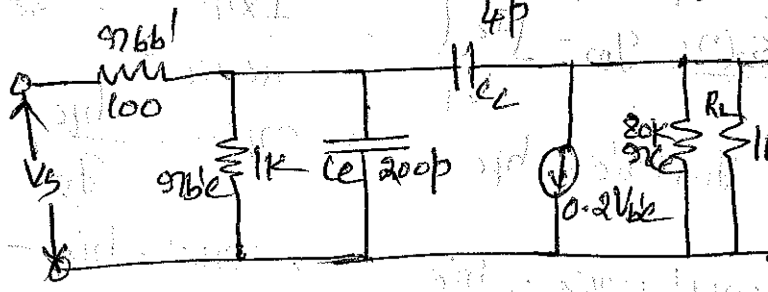
$$\frac{\cancel{r_{b'e}} \times (r_{bb'} + R_s)}{r_{b'e} + r_{bb'} + R_s} = 2 \times \frac{\cancel{r_{b'e}} \times r_{bb'}}{r_{b'e} + r_{bb'}}$$

$$\frac{100 + R_s}{10^3 + 100 + R_s} = \frac{2 \times 100}{10^3 + 100} = 0.1818$$

$$100 + R_s = 181.8 + 18.18 + 0.1818 R_s$$

$$\Rightarrow R_s = 122.2\,\Omega$$

prob④: A CE amplifier's hybrid-π parameters are, $g_m = 0.2\,A/V$, $r_{bb'} = 100\,\Omega$, $r_{b'e} = 1K\Omega$, $C_e = 200\,pF$, $C_c = 4\,pF$ and $r_{ce} = 80K\Omega$, $r_{b'c} = \infty$. Draw the hybrid-π model and calculate A_{VSO}, f_β & f_T with $R_L = 1K\Omega$ & $R_s = 900\,\Omega$.



Soln:
$$A_{VM} = \frac{V_o}{V_s} = \frac{-h_{fe} R_L}{R_s + h_{ie}}$$

$h_{fe} = g_m r_{b'e} = 0.2 \times 10^3 = 200.$

$h_{ie} = r_{bb'} + r_{b'e} = 100 + 10^3 = 1.1K\Omega$

$$\therefore A_{VM} = \frac{-200 \times 10^3}{900 + 1.1 \times 10^3} = -100$$

$$f_\beta = \frac{1}{2\pi r_{b'e}(C_e + C_c)} = \frac{1}{2\pi \times 10^3 (200+4) \times 10^{-12}} = 780.17\,KHz$$

$$f_T = h_{fe} \cdot f_\beta = 200 \times 780.17 \times 10^3 = 156\,MHz$$

Prob: Given the following transistor measurements made at $I_C = 5mA$, $V_{CE} = 1$ at $T = 300°K$, $h_{fe} = 100$, $h_{ie} = 600\Omega$, $A_i = 10$ at $10MHz$, $C_c = 3pF$.
Find f_β, f_T, C_e, $r_{b'e}$ & $r_{bb'}$.

Sol^n:

$$|A_i| = \frac{h_{fe}}{\sqrt{1+(f/f_\beta)^2}}$$

$$10 = \frac{100}{\sqrt{1+(f/f_\beta)^2}}$$

$$\Rightarrow \sqrt{1+(f/f_\beta)^2} = 10$$

$$1+(f/f_\beta)^2 = 100$$

$$(f/f_\beta)^2 = 99$$

$$\Rightarrow \frac{f}{f_\beta} = 9.95 \Rightarrow \frac{10\times10^6}{9.95} = f_\beta = 1.005MHz.$$

$$f_T = h_{fe} f_\beta = 100\times1.005\times10^6 = 100.5MHz.$$

$$C_c + C_e = \frac{g_m}{2\pi f_T} = \frac{|I_C|}{V_T}\times\frac{1}{2\pi f_T}$$

$$= \frac{5\times10^{-3}}{26\times10^{-3}} \times \frac{1}{2\pi\times100.5\times10^6}$$

$$C_c + C_e = 304.5pF \Rightarrow C_e = 301.5pF.$$

$$r_{b'e} = \frac{h_{fe}}{g_m} = \frac{100}{\left(\frac{5\times10^{-3}}{26\times10^{-3}}\right)} = 520\Omega$$

$$r_{bb'} = h_{ie} - r_{b'e} = 600 - 520 = 80\Omega$$

Prob: For a BJT amplifier, the following values are known,
$T = 300°K$, $I_C = 4mA$, $r_{bb'} = 100\Omega$, $r_{b'e} = 1.1K\Omega$, $r_{b'c} = 4M\Omega$,
$r_{ce} = 80K\Omega$, $C_e = 100pF$, $C_c = 2pF$. obtain h-parameters.

Soln:

$$g_m = \frac{I_C}{V_T} = \frac{4m}{26m} = 0.153\ A/V$$

$$h_{fe} = r_{b'e} \cdot g_m = 169.2$$

$$h_{ie} = r_{bb'} + r_{b'e} = 1.2K\Omega$$

$$h_{re} = \frac{r_{b'e}}{r_{b'c}} = 2.75 \times 10^{-4}$$

$$h_{oe} = \frac{1}{r_{ce}} + \frac{(1+h_{fe})}{r_{b'c}} = 0.5\mu A/V$$

Prob: At $I_C = 1mA$ and $V_{CE} = 10V$ a certain transistor data shows $C_c = C_{b'c} = 3pF$
$h_{fe} = 200$, $\omega_T = 500M$ rad/sec. Calculate g_m, $r_{b'e}$, $C_e = C_{b'e}$ and ω_β. ($T = 300$

Soln: $g_m = \frac{I_C}{V_T} = \frac{1m}{26m} = 38.46m\ A/V$

$$r_{b'e} = \frac{h_{fe}}{g_m} = \frac{200}{38.46 \times 10^{-3}} = 5.2K\Omega$$

$$f_T = \frac{g_m}{2\pi(C_e + C_c)} \Rightarrow C_e + C_c = \frac{g_m}{2\pi f_T} = \frac{g_m}{\omega_T} = \frac{38.46 \times 10^{-3}}{500 \times 10^6} = 76.92$$

$$\Rightarrow C_e = 76.92 \times 10^{-12} - 3 \times 10^{-12} = 73.92\ pF$$

$$f_T = h_{fe} f_\beta$$

$$\Rightarrow \omega_T = h_{fe}\, \omega_\beta$$

$$\Rightarrow \omega_\beta = \frac{\omega_T}{h_{fe}} = \frac{500 \times 10^6}{200} = 2.5M\ rad/sec.$$

UNIT – IV MOS AMPLIFIERS. 4-(

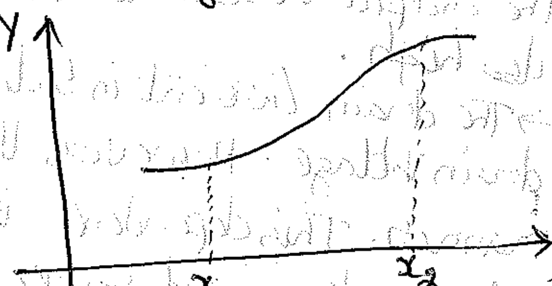
→ The amplification process is a very essential function in most of the analog Circuits. An Analog or digital signal needs amplification,

(i) when the load to be driven is large

(ii) when a large amount of noise of a subsequent stage is needed to be overcome

(iii) when needed to provide a right logical level of signal to the next Circuit.

→ Amplification process plays an important role in the feedback system als



Fig@ Input/output charac. of a nonlinear system

Basic Concepts:

→ The input-output characteristic of an amplifier is normally a non-linear function.

It can be approximated as a polynomial over a finite signal range as given by,

$$y(t) \approx \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \cdots + \alpha_n x^n(t), \quad x_1 \le x \le x_2$$

The input and output signals may be Voltage or Current. • Assuming a sufficiently narrower band of Values of x,

$$y(t) \approx \alpha_0 + \alpha_1 x(t)$$

here α_0 is the operating point or the bias point and α_1 is the small-signal gai

As long as the Value $\alpha_1 x(t) << \alpha_0$, the Variation in the bias point is negligibl higher order terms are insignificant provided a reasonable approximation and which indicates a linear relationship betwee

→ In otherwords, $\Delta y = \alpha_1 \Delta x$, the increments at the input and the corresponding output.

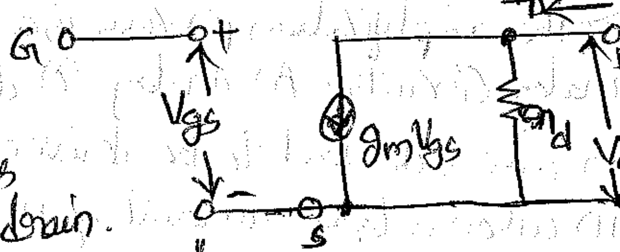
→ As the signal $x(t)$ increases in its magnitude, higher order terms introduce themselves. This leads to increased non-linearity, necessitating large-signal analysis in the process.

→ The slope of the incremental gain characteristics changes with the signal and here the system can be considered to be non-linear.

→ The important performance characteristics of an amplifier are gain, Spe Power dissipation, supply Voltage, linearity, noise and maximum Voltag swings.

→ Additionally, the input and output impedances determine how the Circuit Connects with the previous and Subsequent stage. In practice most of these Parameters are traded-off with each other which makes the design process a multi-dimensional optimization problem.

MOS Small signal model:



→ The FET behaves as a Voltage Controlled Current Source. It receives a signal V_{gs} applied between its gate and source terminals and provides a current of value $g_m V_{gs}$ at the drain.

→ The input resistance is very high or ideally infinity.
The output resistance which is the resistance looking into the drain is also high.

→ The drain current in saturation is assumed to be independent of the drain voltage. However, the drain current depends on V_{ds} in a linear manner. This dependence is modelled by the finite resistance r_d between drain and source.

Transconductance g_m:

Transconductance of MOSFET is given by,

$$g_m = \frac{\partial I_D}{\partial V_{gs}}\bigg|_{V_{ds}}$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_t)^2 = \frac{1}{2}K_n\frac{W}{L}(V_{gs}-V_t)^2$$

$$\boxed{\therefore\ g_m = K_n\frac{W}{L}(V_{gs}-V_t)}$$

→ It indicates that g_m is proportional to the process transconductance parameter $K_n = \mu_n C_{ox}$ and the device size (W/L) ratio of MOS device. Thus a relatively large transconductance device can be obtained with a short and wide transistor.

→ The transconductance of a device is proportional to the overdrive voltage. The bias voltage V_{gs} exceeds the threshold voltage V_t.

→ However increasing g_m by biasing the device with a large V_{gs} reduces the allowable voltage swing at the drain.

→ The parameter g_m can be obtained by substituting for $(V_{gs}-V_t)$ from the drain current equation as,

$$g_m = K_n \frac{W}{L} \cdot \sqrt{\frac{2I_D}{K_n \frac{W}{L}}} \quad \left\{ \because I_D = \frac{1}{2} K_n \frac{W}{L} (V_{gs}-V_t)^2 \right\}$$

$$\boxed{g_m = \sqrt{2 I_D K_n \frac{W}{L}}}$$

→ From above equation it is clear that,

(i) for a given MOSFET g_m is proportional to the square root of the dc bias current.

(ii) at a particular bias current g_m is proportional to size ratio $\left(\frac{W}{L}\right)$

→ on the other hand, the transconductance of the BJT is proportional to the bias current and is independent of the physical size and geometry of the device.

→ Substituting for $K_n\left(\frac{W}{L}\right)$ from drain current equation as,

$$g_m = K_n \frac{W}{L}(V_{gs}-V_t)$$

$$= \frac{2I_D}{(V_{gs}-V_t)^2} \cdot (V_{gs}-V_t)$$

$$\boxed{g_m = \frac{2I_D}{(V_{gs}-V_t)}}$$

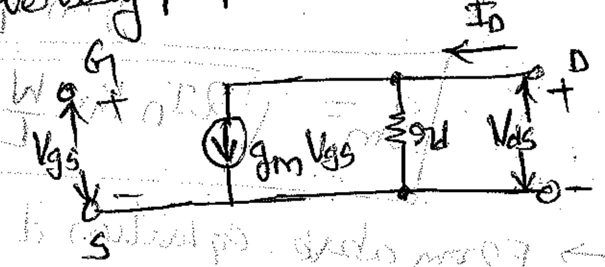
→ Among the three design parameters $\left(\frac{W}{L}\right)$, $(V_{gs}-V_t)$ and I_D any of the two can be choosen independently.

→ To operate the MOSFET a certain overdrive voltage $(V_{gs}-V_t)$ and a current I_D may be chosen. Then $\frac{W}{L}$ ratio may be selected accordingly and finally g_m can be determined.

output Conductance g_d:

$$g_d = \frac{\partial I_D}{\partial V_{ds}}\bigg|_{V_{gs}} = \lambda I_D = \frac{1}{r_d}$$

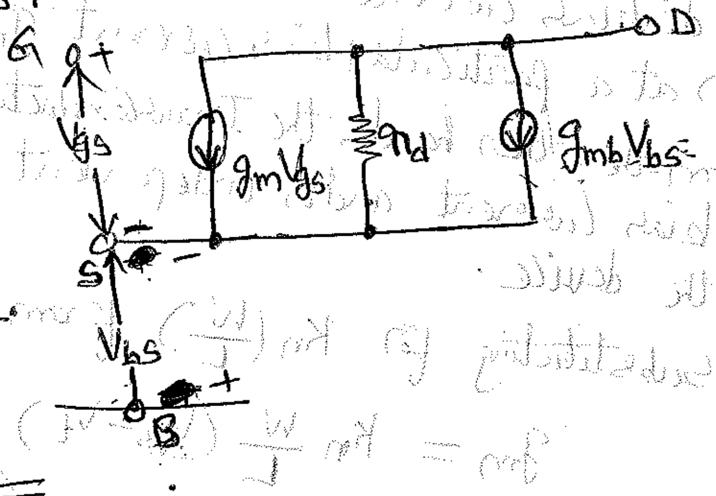
Here 'λ' is the MOSFET parameter that is inversely proportional to the MOSFET channel length.



$$\boxed{\therefore\ I_D = g_m V_{gs} + \frac{V_{ds}}{r_d}}$$

Back Gate TransConductance g_{mb}:

The drain Current also change due to change in the back gate bias. This dependence is represented by another Current Source $g_{mb} V_{bs}$ connected between drain and Source.

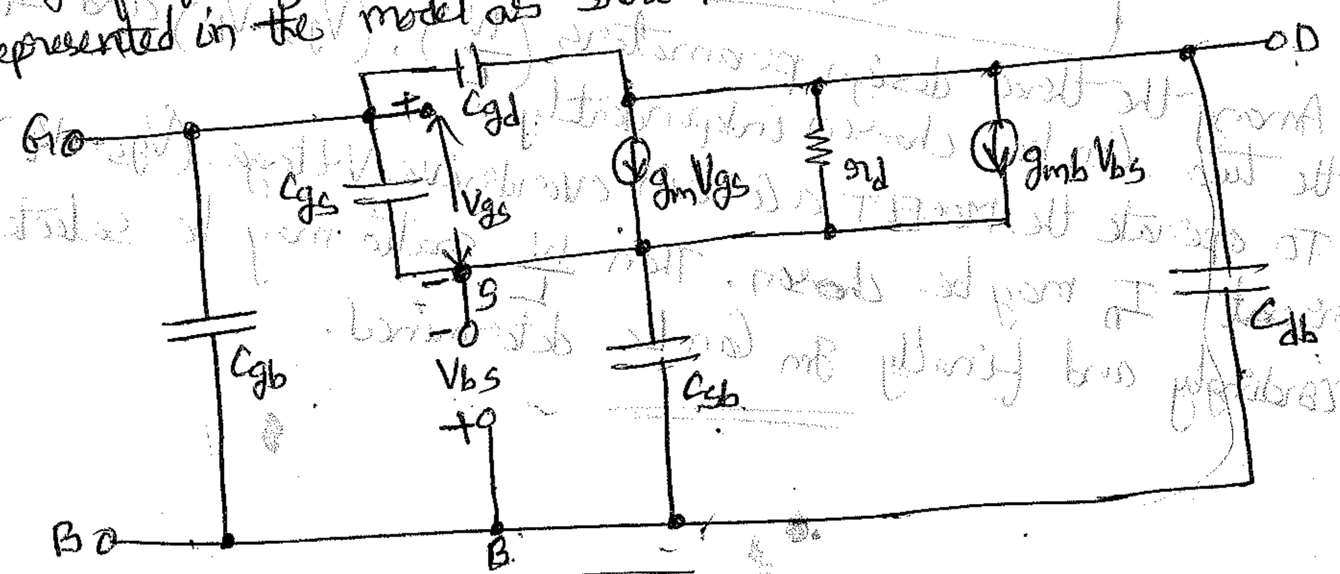


In saturation g_{mb} is,

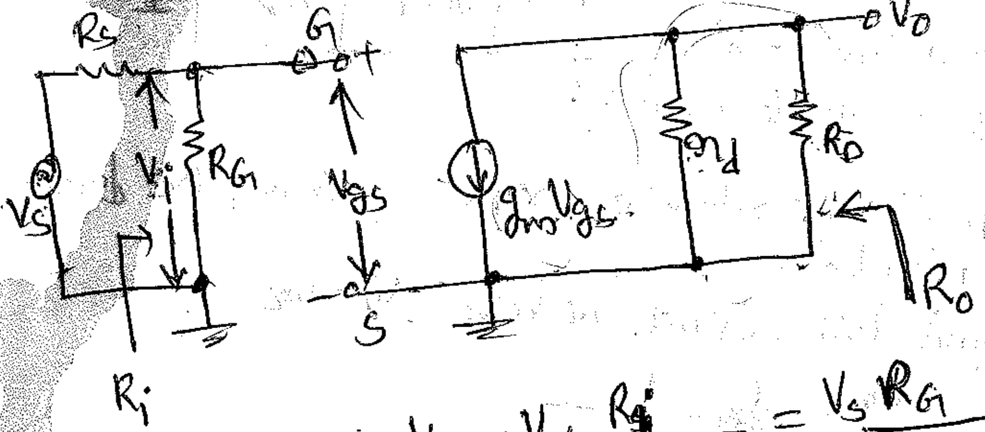
$$g_{mb} = \frac{\partial I_D}{\partial V_{bs}} = g_m \frac{V}{2\sqrt{2\phi_F + V_{SB}}}$$

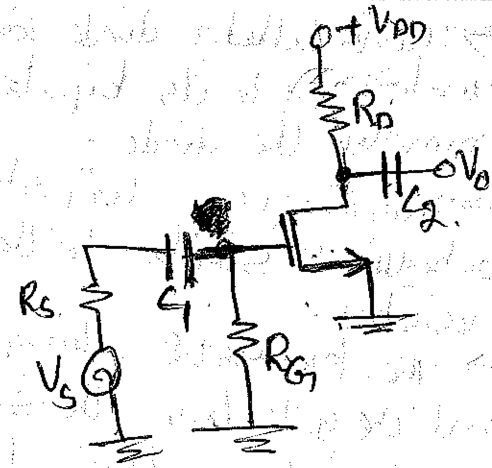
$$g_{mb} = \eta g_m$$

→ At high frequency device Capacitance have their own significance and they are represented in the model as shown.



Common Source (CS) Amplifier with Resistive Load:





$R_i = R_G \quad \therefore V_i = V_s \dfrac{R_i}{R_s + R_i} = \dfrac{V_s R_G}{R_s + R_G}$

But $R_G \gg R_s \quad \therefore V_i \approx V_s$

$\therefore V_{gs} \approx V_i \approx V_s$

$V_o = -g_m V_{gs} (r_d || R_D)$

$\Rightarrow A_V = -g_m (r_d || R_D) = -g_m \dfrac{r_d R_D}{r_d + R_D} \approx -g_m R_D \quad \{\because r_d \gg R_D\}$

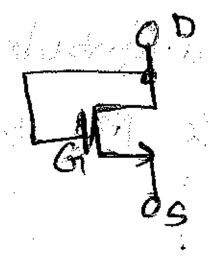
$R_o = r_d || R_D$

Since r_o appears between the drain and source terminals, it is practically connected in parallel with R_D.

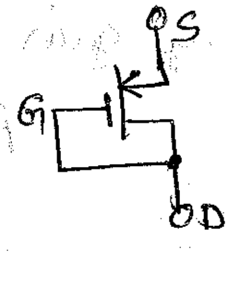
→ Normally $r_d \gg R_D$ thus the effect of r_d is slight reduction in the voltage gain and output resistance R_o.

→ Hence the CS amplifier has a very high input resistance, a moderately high voltage gain and a relatively high output resistance.

Common Source Amplifier with Diode-Connected Load:

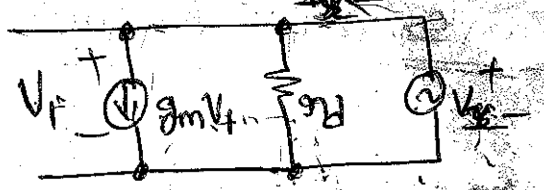


→ In the normal CMOS technologies it is often found difficult to fabricate accurate values of resistors with a reasonable physical size. Hence, it becomes practical to replace R_D with a MOS transistor.



→ The MOSFET can operate as a small-signal resistor when its gate and drain are shorted as shown in figure.

→ This is called a diode connected device analogous to its bipolar counterpart namely the diode.



→ This configuration shows a small-signal behaviour similar to that of a two-terminal resistor.

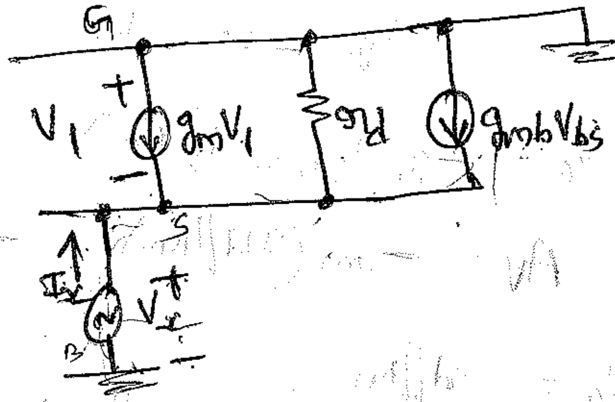
→ The transistor always operates in saturation region, because the drain and the gate have the same potential.

→ Using the small signal equivalent circuit we have $V_1 = V_x$

$$I_x = \frac{V_x}{r_d} + g_m V_x \Rightarrow \frac{V_x}{I_x} = \frac{1}{g_m + \frac{1}{r_d}}$$

$$\therefore R_o = \frac{V_x}{I_x} \approx \frac{1}{g_m} \quad \left\{\because r_d \text{ is very large}\right\}$$

when the body effect is considered,



then $R_o = \frac{V_x}{I_x}$

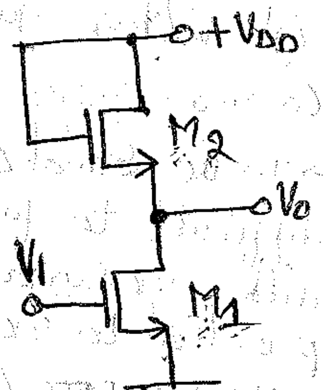
$$I_x = -g_m V_1 - g_{mb} V_{bs} - \frac{V_1}{r_d}$$

But $V_1 = -V_x$ & $V_{bs} = -V_x$

$$\therefore I_x = g_m V_x + g_{mb} V_x + \frac{V_x}{r_d} = V_x\left(g_m + g_{mb} + \frac{1}{r_d}\right)$$

$$\therefore R_o = \frac{V_x}{I_x} = \frac{1}{g_m + g_{mb} + \frac{1}{r_d}} \approx \frac{1}{g_m + g_{mb}}.$$

Now consider CS amplifier with diode-connected loads



Since M_2 is used as a load resistor then,

$$R_o = \frac{1}{g_{m2} + g_{mb2}}$$

Voltage gain for CS-amplifier is,

$$A_V = -g_m (r_d \| R_o)$$

$$\Rightarrow A_V = -g_m R_D \quad \{\because r_d >> R_D\}.$$

For M_1 transconductance is g_{m_1}.

$$\therefore A_V = -g_{m_1} \cdot \frac{1}{g_{m_2} + g_{mb_2}}$$

$$= \frac{-g_{m_1}}{g_{m_2}} \cdot \frac{1}{1 + \left(\frac{g_{mb_2}}{g_{m_2}}\right)}$$

$$\boxed{A_V = \frac{-g_{m_1}}{g_{m_2}} \cdot \frac{1}{1+\eta}} \quad \text{where } \eta = \frac{g_{mb_2}}{g_{m_2}}$$

But $g_m = \sqrt{2 I_D \mu_n C_{ox} \frac{W}{L}}$

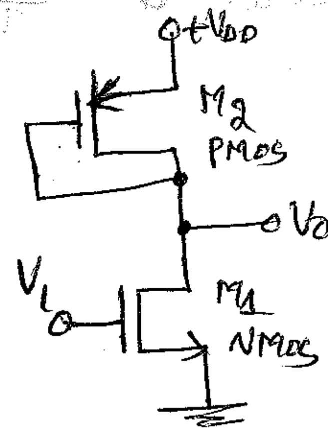
$$\therefore A_V = -\frac{\sqrt{2 I_{D_1} \mu_n C_{ox} (W_1/L_1)}}{\sqrt{2 I_{D_2} \mu_n C_{ox} (W_2/L_2)}} \cdot \frac{1}{1+\eta}$$

since $I_{D_1} = I_{D_2}$ we get,

$$A_V = -\sqrt{\frac{W_1/L_1}{W_2/L_2}} \cdot \frac{1}{1+\eta}$$

→ when the variation of 'η' due to output Voltage is neglected, the gain is independent of the bias currents and Voltages.

→ As the input and output signal levels change, the gain remains relatively constant denoting that the input - output characteristic is relatively linear.

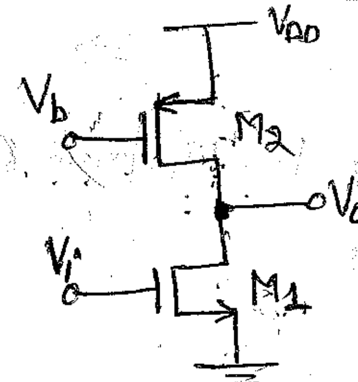


→ when CS stage with diode Connected load is implemented with PMOS device and if the Circuit is free from body effect then,

$$A_V = -\sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_2}} \quad (8)$$

$$A_V = \frac{-g_{m_1}}{g_{m_2}} = \frac{\mu_n C_{ox} (W/L)_1 \; (V_{GS_1} - V_{Th1})}{\mu_p C_{ox} (W/L)_2 \; (V_{GS_2} - V_{Th2})}$$

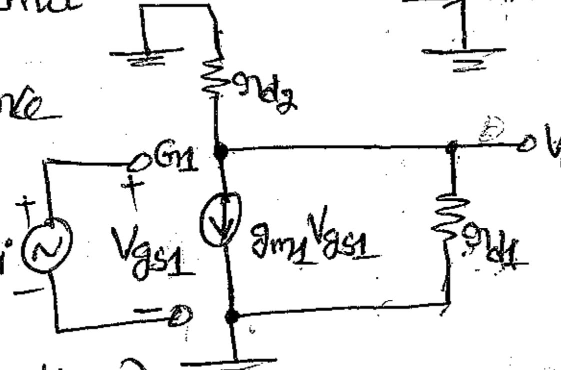
CS Amplifier with Current Source Load:



→ When a large voltage gain is to be realized in a single stage, the relationship $A_1 = -g_m R_o$ compels to have large load impedance.

→ However with a resistor or diode connected load increasing the load resistance value will limit the output voltage swing.

→ The load can be replaced with a current source as shown in figure. Here both the MOSFETs operate in saturation,



→ The total impedance seen at the output node is equal to $(r_{d1} \| r_{d2})$.

∴ The gain is given by, $A_V = -g_{m1}(r_{d1} \| r_{d2})$

→ Usually r_d of a MOSFET is much larger than a resistance R_o that can be placed as load. As a result a saturated PMOS load results in much higher voltage gains.

→ The intrinsic gain of the transistor is given by,

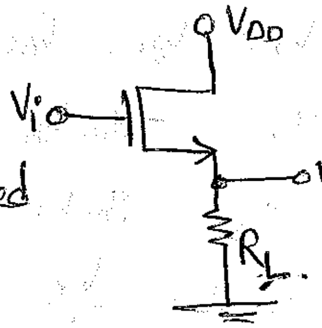
$$g_{m1} \cdot r_{d1} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_1 I_D} \times \frac{1}{\lambda I_D}$$

This shows that the gain increases with L, since λ depends on L than g_m when I_D increases, $g_{m1} r_{d1}$ decreases.

→ When L_2 is increased keeping W_2 constant r_{d2} also increases and hence the voltage gain increases.

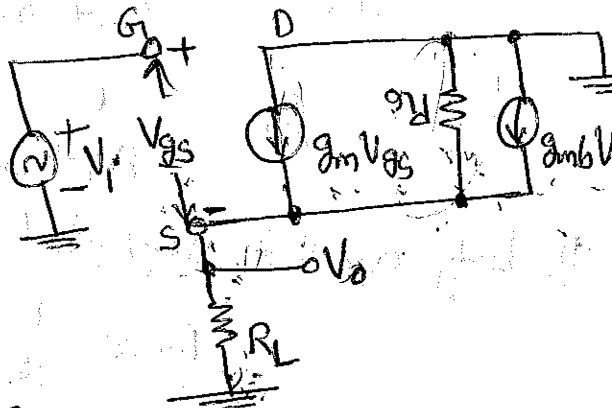
Since $r_d \propto \frac{L}{I_D}$

Source Follower:



→ In CS stage load impedance should be high to get high Voltage gain. Such a stage is not preferable to drive low impedance load because maximum power is transferred when impedances are matched.

→ In such cases buffer amplifier is used to drive the load with negligible loss of signal. A Common drain amplifier circuit shown in figure is used as a buffer also called as source follower.



$$V_o = V_i - V_{gs} = V_i - V_1 \quad \{\because V_1 = V_{gs}\}$$

$$V_{bs} = -V_o$$

$$V_o = I_o R_L = \left[g_m V_{gs} + g_{mb} V_{bs} + \frac{V_{gs}}{r_d}\right] R_L$$

$\{\because r_d$ is very large$\}$

$$\frac{V_o}{R_L} \approx g_m V_{gs} + g_{mb} V_{bs}$$

$\left\{\because \begin{array}{l} V_o = V_i - V_{gs} \\ V_{bs} = -V_o \end{array}\right\}$

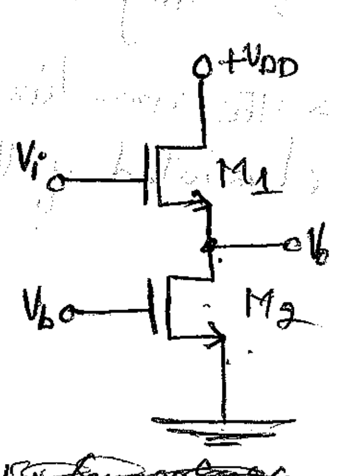
$$= g_m (V_i - V_o) - g_{mb} V_o$$

$$\frac{V_o}{R_L} = g_m V_i - (g_m + g_{mb}) V_o$$

$$V_o \left(\frac{1}{R_L} + g_m + g_{mb}\right) = g_m V_i$$

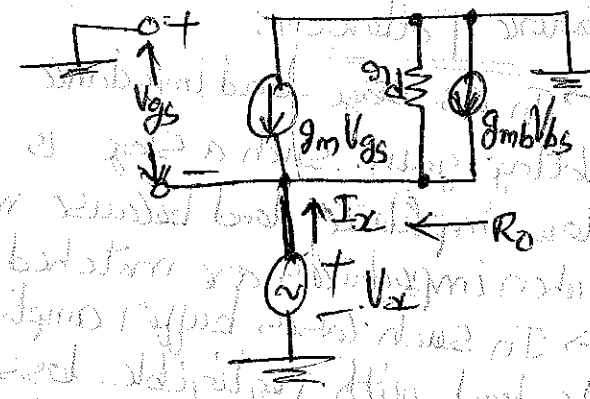
$$\therefore A_V = \frac{V_o}{V_i} = \frac{g_m}{g_m + g_{mb} + \frac{1}{R_L}}$$

$$\boxed{A_V = \frac{g_m R_L}{1 + (g_m + g_{mb}) R_L}}$$



~~Fig: Common Source~~

→ Figure shows the source follower in which resistor 'R_L' is replaced by Current source implemented by MOSFET.



$V_x = -V_{gs}, \quad V_{bs} = -V_x$

$$I_x = -g_m V_{gs} - g_{mb} V_{bs} - \frac{V_{gs}}{r_d}$$

$$I_x = g_m V_x + g_{mb} V_x + \frac{V_x}{r_d}$$

$$\therefore R_o = \frac{V_x}{I_x} = \frac{1}{g_m + g_{mb} + \frac{1}{r_d}}$$

$$R_o = \frac{1}{g_m + g_{mb}} \quad \{\because r_d \text{ is very large}\}$$

If body effect is neglected then,

$$R_o \simeq \frac{1}{g_m}.$$

Advantages:

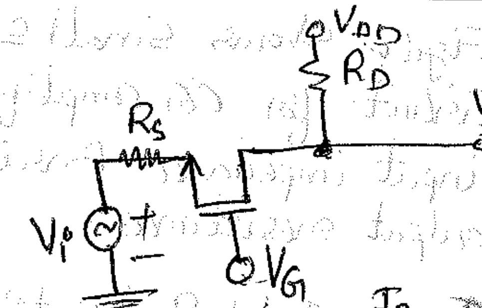
1) They provide high input impedance
2) They provide moderate output impedance
3) used for impedance matching at the output stage of multistage amplifiers
4) used as unity gain Voltage buffer amplifiers.

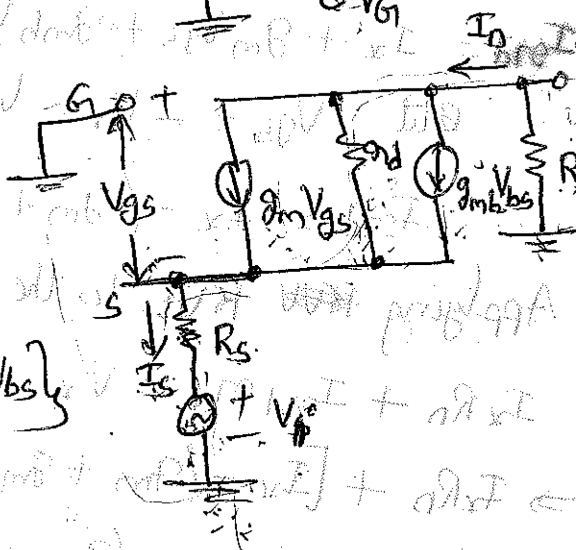
Disadvantages:

1) Suffers from non-linearity due to body effect.
2) They shift the dc level of the signal by V_{gs} thereby Consuming Voltage headroom and limiting the Voltage swings.
3) They have poor driving Capability.

→ The non-linearity of source follower due to body effect can be eliminated if the bulk (body) is tied to the source.

Common Gate stage :





Applying KVL to the input loop,

$$V_{gs} + I_S R_S + V_i = 0$$

But $I_S = I_D = -\frac{V_o}{R_D}$

$$\therefore\ V_{gs} - \frac{V_o}{R_D} R_S + V_i = 0$$

$$\Rightarrow\ V_{gs} = \frac{V_o}{R_D} R_S - V_i$$

$$I_{rd} = I_D - \left(g_m V_{gs} + g_{mb} V_{bs}\right)$$

$$I_{rd} = -\frac{V_o}{R_D} - g_m V_{gs} - g_{mb} V_{gs} \quad \{\because V_{gs} = +V_{bs}\}$$

Applying KVL to output loop,

$$V_o - I_{rd} r_d - I_S R_S - V_i = 0$$

$$\Rightarrow V_o = I_{rd} r_d + I_S R_S + V_i$$

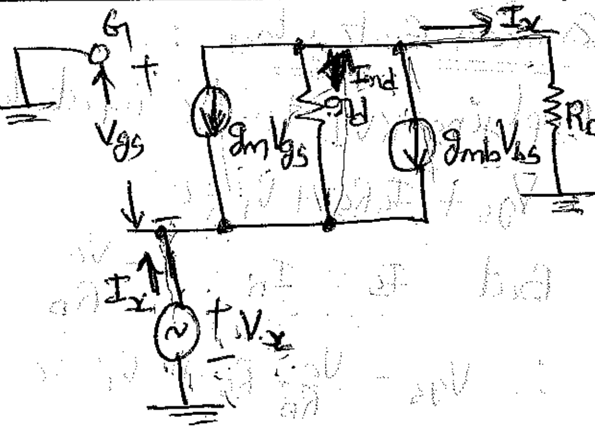
$$V_o = \left[-\frac{V_o}{R_D} - g_m V_{gs} - g_{mb} V_{gs}\right] r_d - \frac{V_o}{R_D} R_S + V_i$$

$$V_o = \left[-\frac{V_o}{R_D} - (g_m + g_{mb})\left(\frac{V_o}{R_D} R_S - V_i\right)\right] r_d - \frac{V_o}{R_D} R_S + V_i$$

$$V_o = -V_o\left[\frac{r_d}{R_D} + \frac{(g_m + g_{mb}) R_S r_d}{R_D} + \frac{R_S}{R_D}\right] + V_i\left[1 + (g_m + g_{mb}) r_d\right]$$

$$A_V = \frac{V_o}{V_i} = \frac{1 + (g_m + g_{mb}) r_d}{1 + \frac{r_d + R_S + (g_m + g_{mb}) R_S r_d}{R_D}}$$

Figure shows small signal equivalent circuit for CG amplifier to determine input impedance considering finite output resistance.



$I_{rd} = I_x + g_m V_{gs} + g_{mb} V_{bs}$

But $V_{gs} = -V_x = V_{bs}$

$\therefore \; I_{rd} = I_x - (g_m + g_{mb}) V_x$

Applying KVL to the output-loop we have,

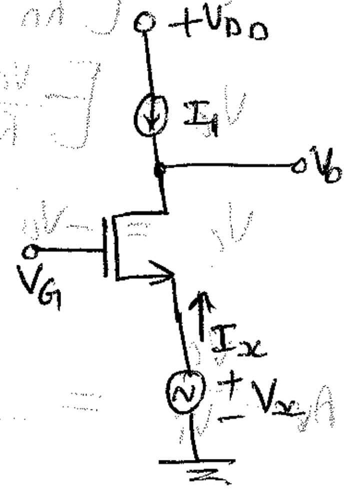
$I_x R_D + I_{rd} r_d - V_x = 0.$

$\Rightarrow I_x R_D + [I_x - (g_m + g_{mb}) V_x] r_d - V_x = 0.$

$(R_D + r_d) I_x - (g_m + g_{mb}) r_d V_x - V_x = 0.$

$$\Rightarrow \frac{V_x}{I_x} = \frac{r_d + R_D}{1 + (g_m + g_{mb}) r_d}$$

$$R_i \approx \frac{r_d + R_D}{(g_m + g_{mb}) r_d} \qquad \{\because (g_m + g_{mb}) r_d \gg 1\}$$



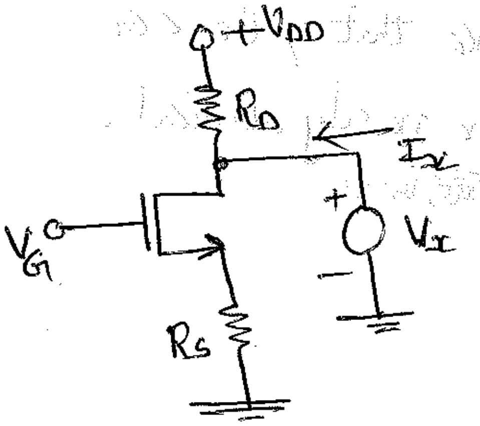
If R_D is replaced by an ideal current source as shown in figure, the input impedance approaches infinity. Here, the current through the MOSFET is fixed and equal to I_1, a change in the source potential does not change I_D and hence $I_x = 0$.

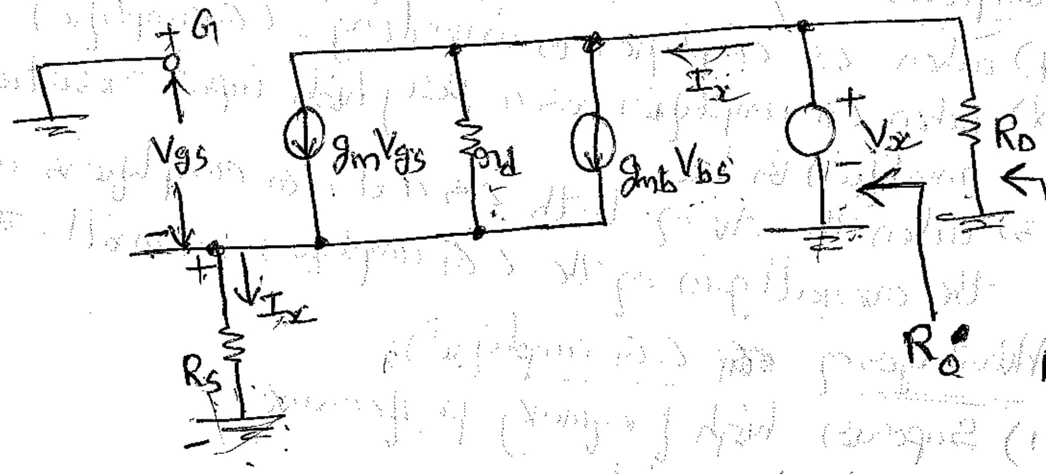
$$\therefore R_i = \frac{V_x}{0} = \infty$$

when R_D approaches to ∞ we have,

$$A_V = 1 + (g_m + g_{mb}) r_d$$

Figure shows equivalent circuit of CG amplifier for calculating output resistance.





$V_{gs} = -I_x R_s$ and

$I_{rd} = I_x - (g_m + g_{mb}) V_{gs}$ $\{\because V_{gs} = V_{bs}\}$

$= I_x + (g_m + g_{mb}) I_x R_s$

$I_{rd} = I_x [1 + (g_m + g_{mb}) R_s]$

Applying KVL to the output loop we have,

$V_x - r_d [I_x + (g_m + g_{mb}) I_x R_s] - I_x R_s = 0$

$\Rightarrow V_x = I_x [1 + (g_m + g_{mb}) R_s] r_d + R_s I_x$

$$\frac{V_x}{I_x} = [1 + (g_m + g_{mb}) R_s] r_d + R_s$$

$$R_o = [1 + (g_m + g_{mb}) r_d] R_s + r_d$$

$$R_o \approx (g_m + g_{mb}) r_d R_s + r_d$$

$$R_o \approx [1 + (g_m + g_{mb}) R_s] r_d$$

Considering R_D we have,

$$R_o' = \{[1 + (g_m + g_{mb}) R_s] r_d\} || R_D$$

~~Cascode Amplifiers~~

Comparision of CS & CG Amplifiers:

1) when CS amplifier is inverting, CG amplifier is non-inverting.
2) when CS amplifier has a very high input resistance that of the CG amplifier is low.
3) when the A_V of both CS and CG amplifiers are nearly identical, the overall gain of the CG amplifier is small.

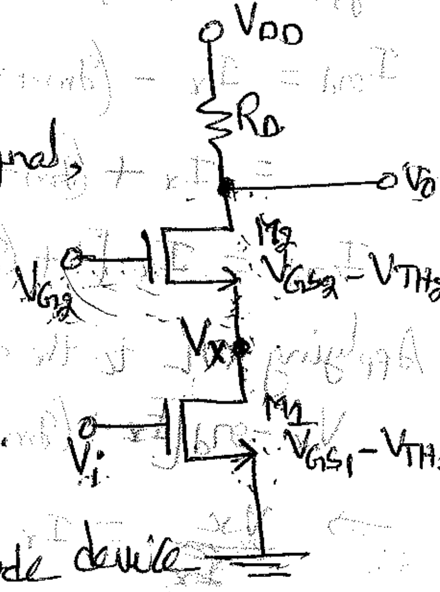
Advantages of CG amplifier:

1) Superior high frequency performance
2) Low input resistance
3) used in high frequency applications eg: transmission line.

Cascode Amplifier:

→ The input signal of a CG amplifier is a current signal, the transistor in CS amplifier converts voltage signal into current.

→ The cascode of CS and CG amplifiers is called cascode structure as shown in figure.



→ M_1 generates small signal current proportional to V_i and M_2 guides this current to R_D and M_2 is identified as the cascode device. M_1 is called input device and M_2 is identified as the cascode device and M_1 and M_2 carry equal currents.

→ Looking at the biasing for the cascode amplifier for M_1 to operate in saturation we have, $V_x \geq V_i - V_{TH1}$

when both M_1 and M_2 are operating in saturation, V_x is determined mainly by V_{G2} and $V_x = V_{G2} - V_{GS2}$.

$$\therefore \; V_{G2} - V_{GS2} \geq V_i - V_{TH1}$$

$$\Rightarrow \; V_{G2} > V_i + V_{GS2} - V_{TH1}$$

→ To operate M_2 in saturation,

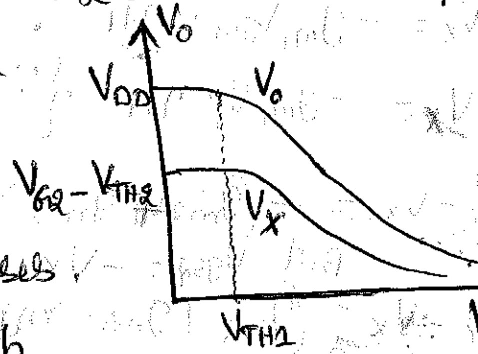
$$V_0 \geq V_{G2} - V_{TH2} \text{ (or)}$$

$$V_0 \geq V_i + V_{GS2} - V_{TH1} - V_{TH2}.$$

when V_{G2} is chosen to place M_1 at the edge of saturation.

→ As a ~~...~~ result the minimum output level for which both the transistors operate in saturation is equal to the overdrive voltage of M1 plus that of M_2.

→ The inclusion of M_2 in the circuit reduces the output voltage swing by atleast the amount of overdrive voltage of M_2 and M_2 is stacked on M_1.



→ when V_i rises from 0 to V_{DD} for $V_i \le V_{TH1}$, M_1 and M_2 remain off, also $V_0 = V_{DD}$ and $V_X \approx V_{G2} - V_{TH2}$ neglecting the subthreshold conduction factor.

→ As V_{in} exceeds V_{TH1}, M_1 tends to draw current making V_0 drop. As I_{D2} increases, V_{GS_2} also increases.

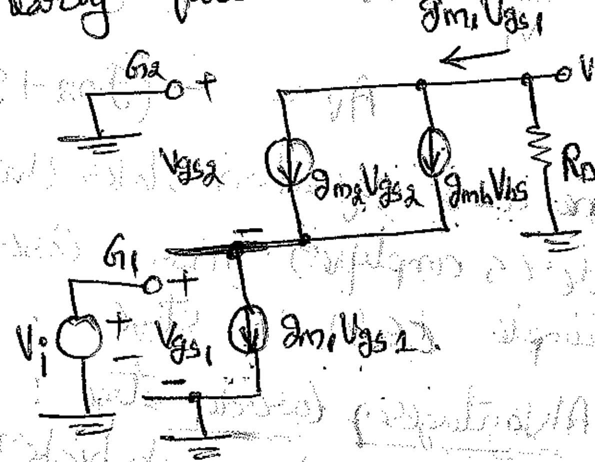
→ This causes V_X to fall. when V_i becomes very high,

(i) V_X drops below V_i by V_{TH1} pushing M_1 into triode region of operation.

(ii) V_0 goes below V_i by V_{TH2} driving M_2 into the triode region of operation.

→ Based on the device sizes and the values of R_D and V_{G2}, one supersedes the other. Thus when V_b is low, M_1 enters the triode region first. when M_1 goes into deep triode region V_X and V_0 get nearly equal.

→ Consider the small signal equivalent circuit of cascode amplifier,



$$V_0 = -g_{m_1} V_{gs_1} \cdot R_D$$

$$V_0 = -g_{m_1} V_i R_D \qquad \{\because V_{gs_1} = V_i\}$$

$$\therefore A_V = \frac{V_0}{V_i} = -g_{m_1} R_D$$

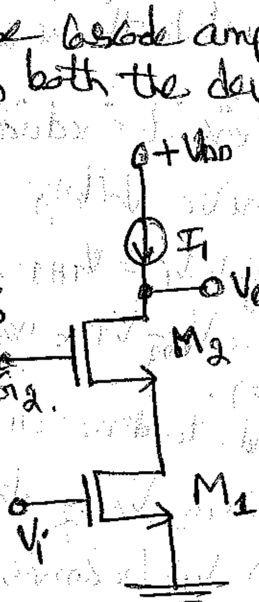
output resistance of CG amplifier is, $R_0 = [1 + (g_m + g_{mb}) r_d] R_S + r_d$

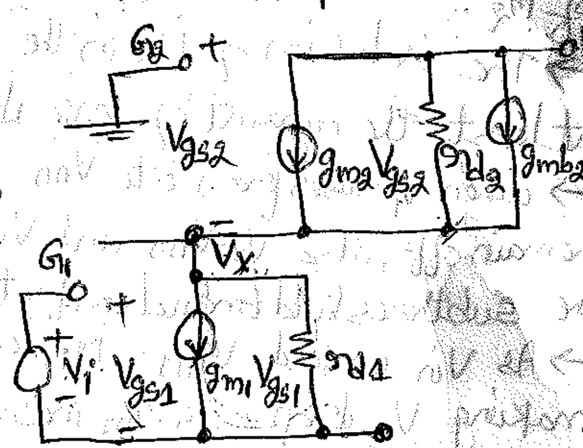
In the cascode amplifier R_S is nothing but output resistance of CS amplifier i.e $r_{d1} = R_S$

$$\therefore R_0 = [1 + (g_m + g_{mb}) r_{d_2}] r_{d_1} + r_{d_2}$$

→ Cascading can be extended to three or more stacked devices also for realizing higher output impedance values. However the required additional voltage headroom makes such configurations less attractive.

→ We know that $A_V \propto g_m R_o$, to increase the voltage gain increase R_o which results in voltage swings. So use cascode amplifier with current source load as shown in figure in which both the devices M_1 and M_2 operate in saturation.





$$V_X = -g_{m1} V_{gs1} \cdot r_{d1}$$

$$V_X = -g_{m1} V_i \cdot r_{d1} \quad \left\{ \because V_i = V_{gs1} \right\}$$

$$V_o - V_X = -(g_{m2} + g_{mb2}) r_{d2} \cdot V_{gs2}$$

But $V_{gs2} = -V_X$

$$V_o - V_X = (g_{m2} + g_{mb2}) r_{d2} V_X$$

$$V_o = \left[1 + (g_{m2} + g_{mb2}) r_{d2}\right] V_X$$

$$V_o = -\left[1 + (g_{m2} + g_{mb2}) r_{d2}\right] g_{m1} V_{gs1} \cdot r_{d1}$$

$$\frac{V_o}{V_i} = A_V = -\left[1 + (g_{m2} + g_{mb2}) r_{d2}\right] g_{m1} r_{d1}$$

$$A_V = -(g_{m2} + g_{mb2}) r_{d2} \cdot g_{m1} r_{d1}$$

The above equation states that gain of cascode amplifier is nearly square of the CS amplifier. Thus a cascode stage provides a much larger gain than a simple CS or CG stage.

Advantages of cascode stage:

1) They provide much higher gain
2) They provide high frequency response i.e. higher bandwidth.
3) They can be used to build constant current sources
4) They provide higher output impedance
5) They provide higher input impedance

Disadvantages:

1) Requires two transistors and high supply voltage
2) In cascode circuit, transistors must be biased with ample V_{DS} in operation imposing lower limit on the supply voltage.

shielding property:

→ The high output impedance of the circuit is resulted due to the fact that when the output node voltage is varied by ΔV, the effecting change at the source of the cascode device is much less.

→ In other words the cascode transistor shields the input device from voltage variations at the output. This shielding property of the cascode structure is useful in many applications.

→ The shielding property of cascodes diminishes if the cascode device enters the triode region (or) ohmic region (or) linear region.

Folded Cascode Amplifier:

→ The principle behind the cascode structure is that the input voltage is converted into a current and it is applied to a CG amplifier. However the input and the cascode devices need not be of the same type.

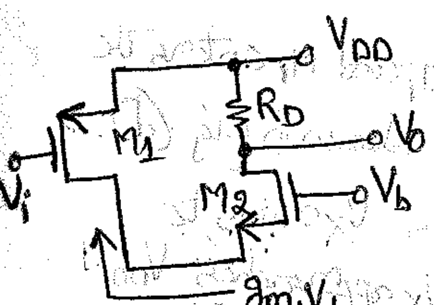


Fig (a) simple folded cascode amplifier

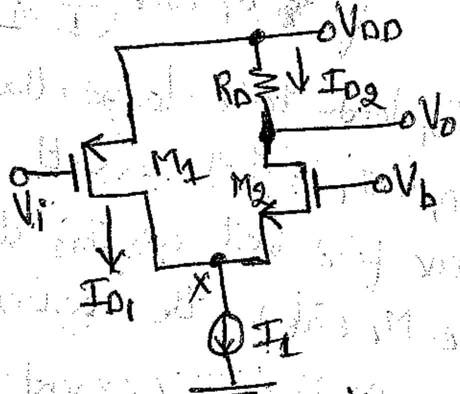


Fig (b) Folded cascode with current source biasing

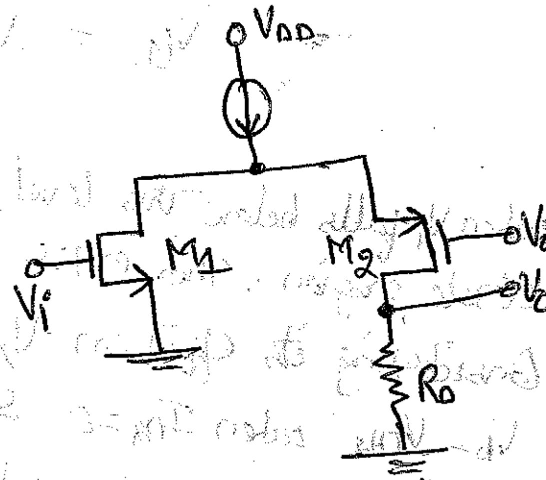


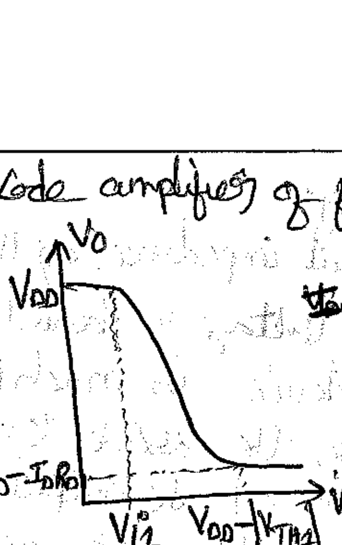
Fig (c) Folded cascode with NMOS input.

→ Fig (a) shows a simple folded cascode PMOS-NMOS pair. To bias the devices M_1 and M_2 a current source is to be added as in fig (b).

→ when V_i becomes more positive $|I_{D1}|$ falls making I_{D2} rise. This makes V_0 drop. The voltage gain and output impedance of the circuit can be found out in the same manner dealt with NMOS-NMOS cascode. Fig (c) shows NMOS-PMOS cascode.

→ The circuit configurations of fig (b) and (c) are called folded cascode amplifiers since the small-signal current is folded up as shown in fig (b) or folded down as shown in fig (c). Here the total bias current must be higher than that in ordinary cascode amplifier to achieve comparable performance.

Consider the large signal behaviour of folded cascode amplifier of fig (b) as shown in figure (d).



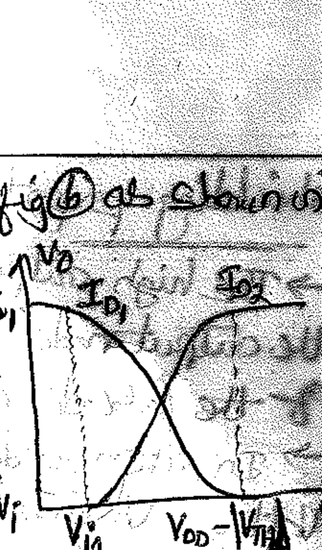


Fig (d).

Assume that V_i decreases from V_{DD} to zero.
when $V_i > V_{DD} - |V_{TH1}|$, M_1 is off and M_2 passes all of I_1. It yields $V_o = V_{DD} - I_1 R_D$.
when $V_i < V_{DD} - |V_{TH1}|$, M_1 turn on and operates in saturation, making

$$I_{D2} = I_1 - \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_1 \left[V_{DD} - V_i - |V_{TH1}|\right]^2$$

As V_i falls, I_{D2} reduces further, reaches zero when $I_{D1} = I_1$.

$$\frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_1 \left[V_{DD} - V_i - |V_{TH1}|\right]^2 = I_1$$

$$\Rightarrow V_{i1} = V_{DD} - \sqrt{\frac{2I_1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_1}} - |V_{TH1}|.$$

when V_i falls below this level, I_{D1} tends to be larger than I_1 and M_1 enters the circle region. This makes $I_{D1} = I_1$ and the result is shown in fig (d). Considering its effect on V_x, we find that as I_{D2} drops V_x rises to $V_b - V_{TH2}$ when $I_{D2} = 0$. Since M_1 enters the region, V_x approaches V_{DD}.

→ Fig (e) shows folded cascode amplifier with current source implementation using MOSFET.
The output resistance R_o for above amplifier is,

$$R_o = \left[1 + (g_{m2} + g_{mb2})r_{d2}\right](r_{d1} \| r_{d3}) + r_{d2}$$

This output impedance is lower than that of a non-folded cascode.

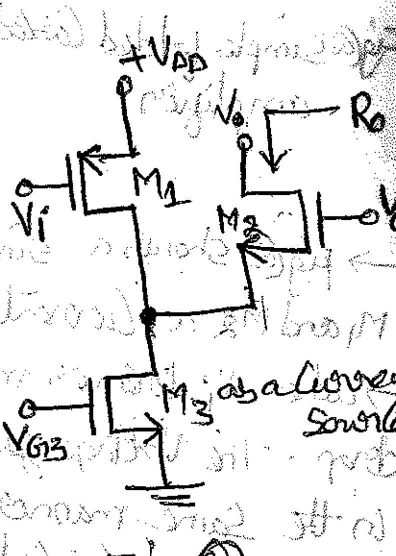
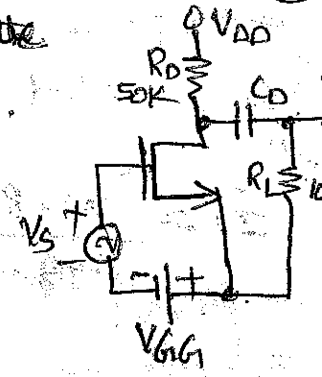
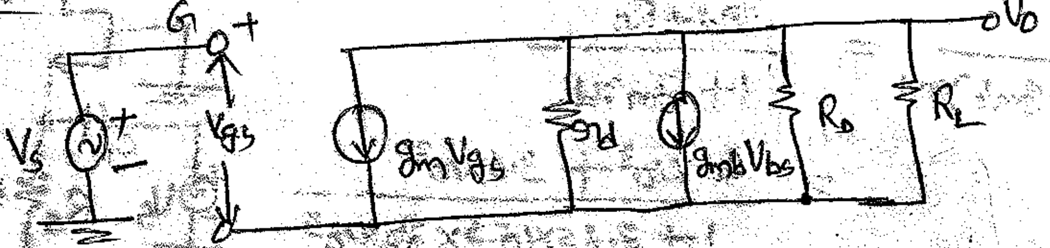


Fig: (e)

Prob 1: Calculate the voltage gain of the FET amplifier assuming the blocking capacitor to be large. $g_m = 4mA/V$ & $r_d = 5K\Omega$.



Soln:



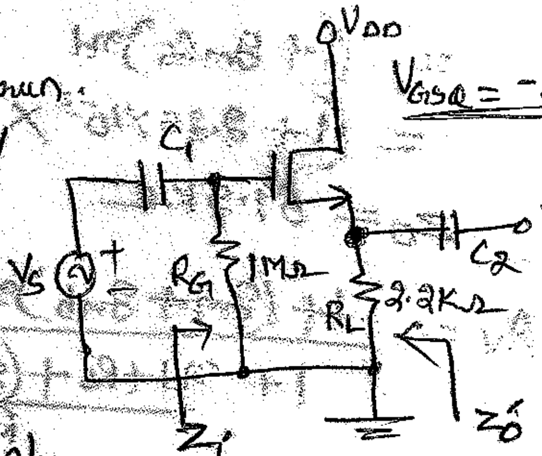
$A_V = -g_m Z_L$ where $Z_L = r_d \| R_D \| R_L$

$A_V = -g_m (r_d \| R_D \| R_L) = -4\times10^{-3} \times (5K \| 50K \| 10K)$

$A_V = -4\times10^{-3} \times (3.125\times10^{3})$

$A_V = -12.5$

Prob 2: Calculate A_v, Z_i & Z_o for FET amplifier shown. If $I_{DSS} = 16mA$, $V_p = -4V$ and $g_d = 25\mu A/V$



Soln: $r_d = \frac{1}{g_d} = \frac{1}{25\times10^{-6}} = 40K\Omega$

$g_m = g_{mo}\left(1 - \frac{V_{GSQ}}{V_P}\right)$

where $g_{mo} = \frac{2 I_{DSS}}{|V_P|} = \frac{2\times 16\times10^{-3}}{4} = 8mA/V$

$\therefore g_m = 8\times10^{-6} \times \left[1 - \left(\frac{-2.86}{-4}\right)\right] = 2.28 mA/V$

$Z_i = R_G = 1M\Omega$

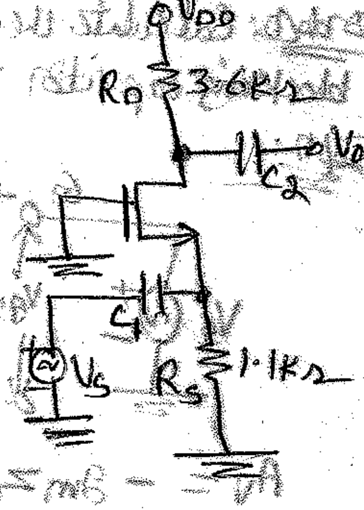
$Z_o = \frac{1}{g_m + g_{mb} + \frac{1}{r_d}} = \frac{1}{g_m + \frac{1}{r_d}} = \frac{1}{2.28\times10^{-3} + \left(\frac{1}{40\times10^{3}}\right)} = 433.8$

$Z_o' = Z_o \| R_L = 433.83 \| 2.2K = 362.39\,\Omega$

$A_V = \frac{g_m R_L}{1 + (g_m + g_{mb}) R_L} = \frac{g_m R_L}{1 + g_m R_L} = \frac{2.28\times10^{-3}\times2.2\times10^{3}}{1 + 2.28\times10^{-3}\times2.2\times10^{3}}$

$A_V = 0.83$

prob ③: For the FET amplifier shown calculate Z_i, Z_o & A_V. $g_m = 2.25\,mA/V$ and $r_d = 20K\Omega$.



Soln:

$$Z_i = \frac{r_d + R_D}{1+(g_m+g_{mb})r_d} = \frac{r_d+R_D}{1+g_m r_d}$$

$$= \frac{20\times10^3 + 3.6\times10^3}{1+2.25\times10^{-3}\times 20\times10^3}$$

$$Z_i = 513\,\Omega$$

$$Z_i' = Z_i \| R_S = 513 \| 1.1K = 349.8\,\Omega$$

$$Z_o = [1+(g_m+g_{mb})R_S]\,r_d$$

$$= (1+g_m R_S)\,r_d$$

$$= (1+2.25\times10^{-3}\times1.1\times10^3)\times 20\times10^3$$

$$Z_o = 69.5K\Omega$$

$$A_V = \frac{1+(g_m+g_{mb})r_d}{1+\frac{r_d+R_S+(g_m+g_{mb})R_S r_d}{R_D}}$$

$$A_V = \frac{(1+g_m r_d)R_D}{R_D+r_d+R_S+g_m R_S r_d}$$

$$= \frac{[1+(2.25\times10^{-3}\times20\times10^3)]\times3.6\times10^3}{3.6\times10^3+20\times10^3+1.1\times10^3+2.25\times10^{-3}\times1.1\times10^3\times20\times10^3}$$

$$A_V = 2.23$$