UNIT- V

SAMPLING GATES

Basic operating principles of sampling gates, Unidirectional diode gate, Bi-directional sampling gates using transistors, Reduction of pedestal in gate circuit, four diode sampling gate, an alternate form of four diode gate, six diode sampling gate, chopper amplifier, sampling scope.

LOGIC FAMILIES

Realization of Logic gates (OR, AND, Not) using Diodes and Transistors, DCTL, RTL, DTL, TTL, ECL, CML, CMOS logic family and comparison of logic families.

SAMPLING GATES

Introduction

Def:

"An ideal sampling gate is a transmission circuit in which the output is an exact reproduction of an input waveform during a selected time interval and is zero otherwise".

→ The time interval for transmission is selected by an externally impressed signal which is called the gating signal.

It is usually rectangular in waveshape.

The gating signal is also called as control pulse (or) selector pulse (or) Enabling pulse.

→ Sampling gates are also called as transmission gates (or) time-selection circuits (or) linear gates.

classification of sampling gates:

These are broadly classified as

1) Unidirectional sampling gates.
2) Bi-directional sampling gates.

Unidirectional sampling gate:

If the input signal consists essentially of a unidirectional pulse, the sampling gate is required to respond to an input signal of only one polarity, such sampling gate is known as unidirectional gate.

Bi-directional sampling gate:

If a sampling gate is required to handle (or transmit) the excursions of signals of both the polarities, it is known as Bi-directional sampling gate.

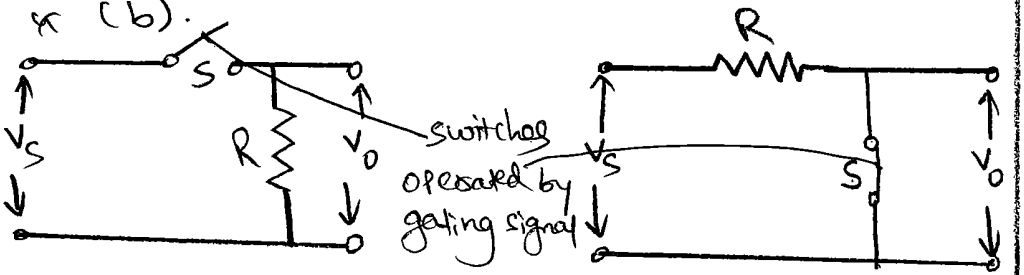
→ A sampling gate has one signal input and during the selected time interval, the output must reproduce faithfully the input waveform, be it a pulse, a sinusoid or any other waveform. Hence a sampling gate is also called as linear gate.

Comparison between Logic gate and Sampling gate

Logic gates	Sampling gates
1) In this, there can be any number of inputs.	1) In this, it has only single input.
2) A logic gate has to provide at the output a pulse (or) no pulse, depending on the pulses present at the many gate inputs and the type of the gate.	2) A sampling gate provides an output, which is an exact reproduction of the input during the selected time interval. (whatever may be the input, a pulse, a sinusoid or any other waveform).
3) Ex: AND, OR, NOT, NAND, NOR, EX-OR	3) Ex: Unidirectional and Bi-directional sampling gates.

Basic operating principles of sampling gates

The basic operating principle of a linear gate is shown in fig (a) & (b).



a) circuit using series switch b) circuit using shunt switch

→ In fig (a), switch 's' is normally open and is closed during the desired transmission interval.

→ In fig (b), switch 's' is normally closed and is opened only during the desired transmission interval.

→ Semiconductor devices such as diodes and transistors are used as switches. When they are conducting, they acts as a closed switch and when they are not conducting, they acts as an open switch.

→ Ideally, the switches should have zero resistance when closed and infinite resistance when open.

But semiconductor devices do not have infinite back resistance and their forward resistance may lie in the range of several ohms.

When such devices are used there is no generally apparent advantage in either

the series (or) shunt switch position, and the decision with respect to the circuit of choice must depend on the particular application.

→ When semiconductor devices are used as a switch the circuit of fig(a) has the following disadvantages over the circuit of fig(b) are:

a) The inevitable stray capacitance across the switch will permit some signal transmission even when the switch is open.

b) Since the signal is transmitted through 'S' there will be some attenuation and distortion introduced by the non-linearity of the device used for the switch.

Unidirectional sampling Gate:

A uni-directional sampling gate which uses a semiconductor diode as a switch is shown below:

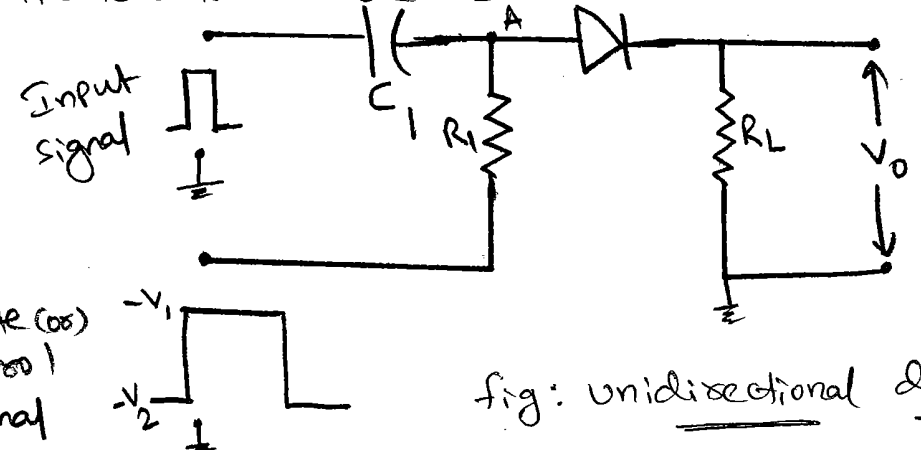


fig: unidirectional diode gate

→ The above gate is suitable for a positive going input signal.

→ The gate signal i.e; the signal which determines the gating (or) transmission period, is a rectangular wave form with voltage levels $-V_1$ and $-V_2$ is applied and voltage level $-V_1$ is more positive than $-V_2$.

→ i) when the gating signal is at $-V_2$ the diode gets reverse-biased so there is no conduction because of capacitive coupling, the signal input voltage will appear at point A with an average level $-V_2$ and hence resulting zero output.

It is assumed that the peak amplitude of the input signal is smaller than the back-biasing voltage $-V_2$.

If the peak amplitude of the input signal is greater than the voltage level $-V_2$, the diode may conduct giving undesirable output voltage.

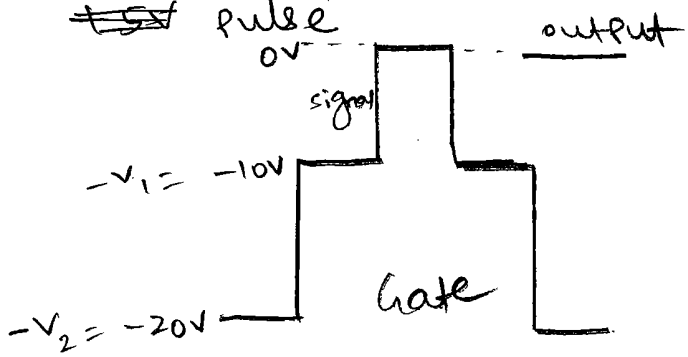
ii) → when the gate signal voltage rises abruptly from $-V_2$ to $-V_1$, the positive going input signal causes the diode to be forward biased, diode D conducts and a time-coincident signal input pulse is transmitted through the gate and an output voltage appears across R_L.

If ideal conditions are assumed, then there is neither attenuation nor distortion of the input signal. The output voltage would be an exact replica of the input signal.

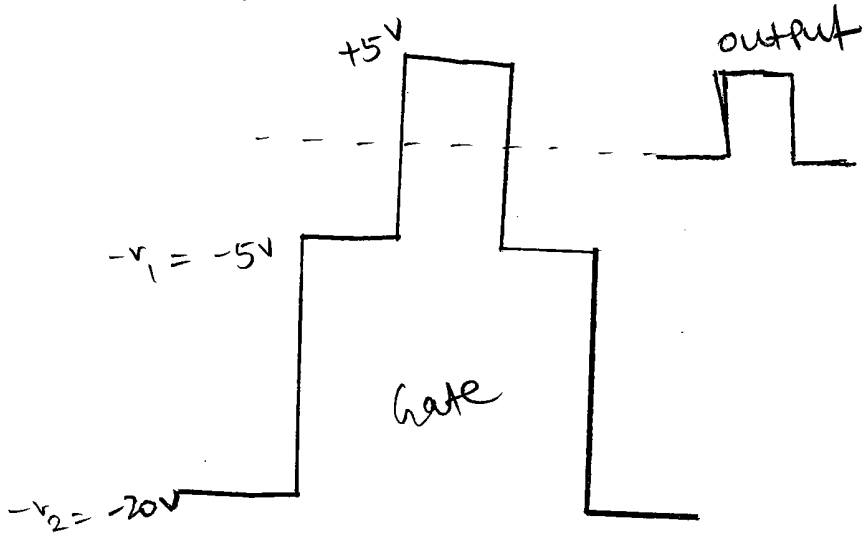
→ The effect of the higher level of the gating signal $-V_1$ on gate output is shown below.

Let the input signal is a +10V pulse.

i) when ~~zero~~ $-V_2 = -20V$, $-V_1 = -10V$, the output is a ~~5V~~ pulse



ii) when $-V_2 = 20V$, $-V_1 = -5V$, the output is a $+5V$ pulse.

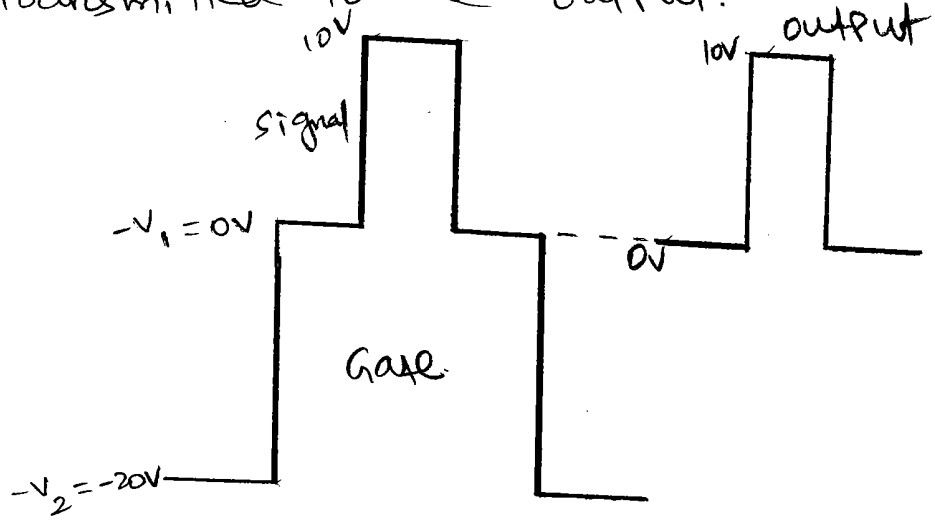


iii) Operation in this manner is often advantageous when the base line of the input signal has some noise signal superimposed.

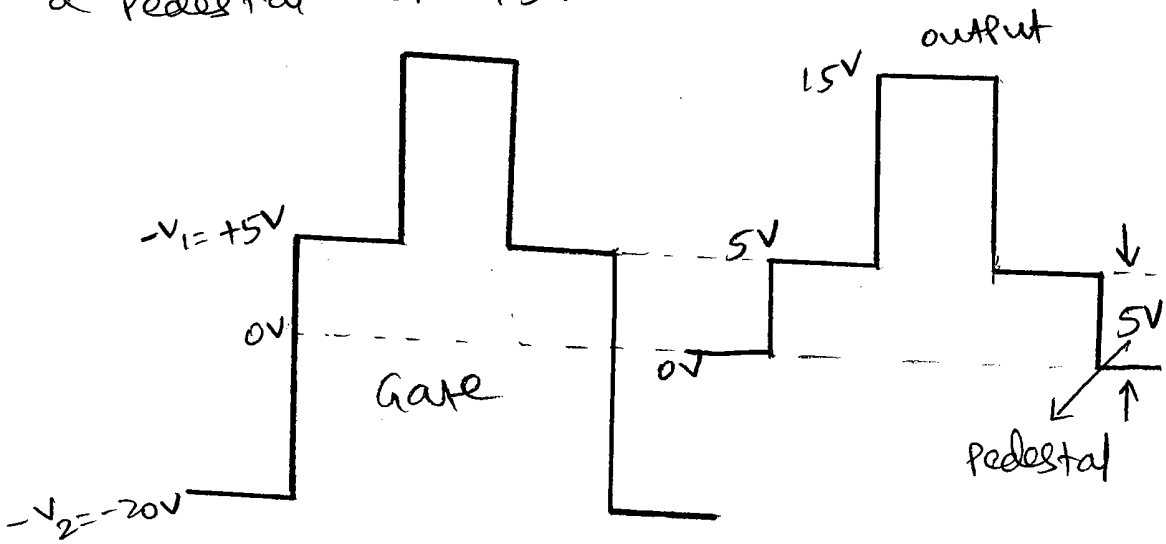
The level $-V_1$ may be adjusted so that only that part of the signal above the noise threshold appears at the output.

When used in this manner, the circuit is called as "Threshold gate".

iii) when $-V_2 = -20V$, $-V_1 = 0V$, the output is a +10V pulse i.e; the entire input pulse is transmitted to the output.



iv) when $-V_2 = -20V$ and $-V_1 = +5V$, then the output is a +10V pulse superimposed on a pedestal of +5V



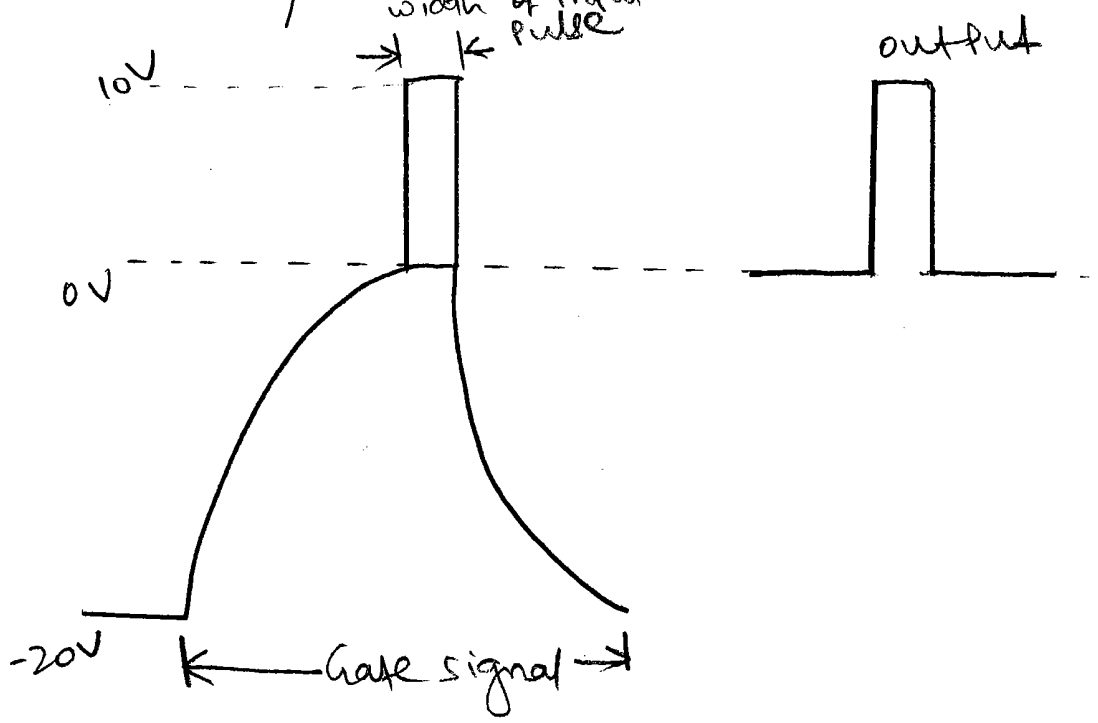
The wave forms of the above figures are not practical, because we have not considered the fact that R_1C_1 network constitutes an integrating

network for the gate waveform.

Hence the gate voltage will not appear abruptly at A as required, but rather will rise exponentially with a time constant R_1C_1 and fall at similar rate.

Hence this type of gate is not suitable for selecting a part of a continuous waveform.

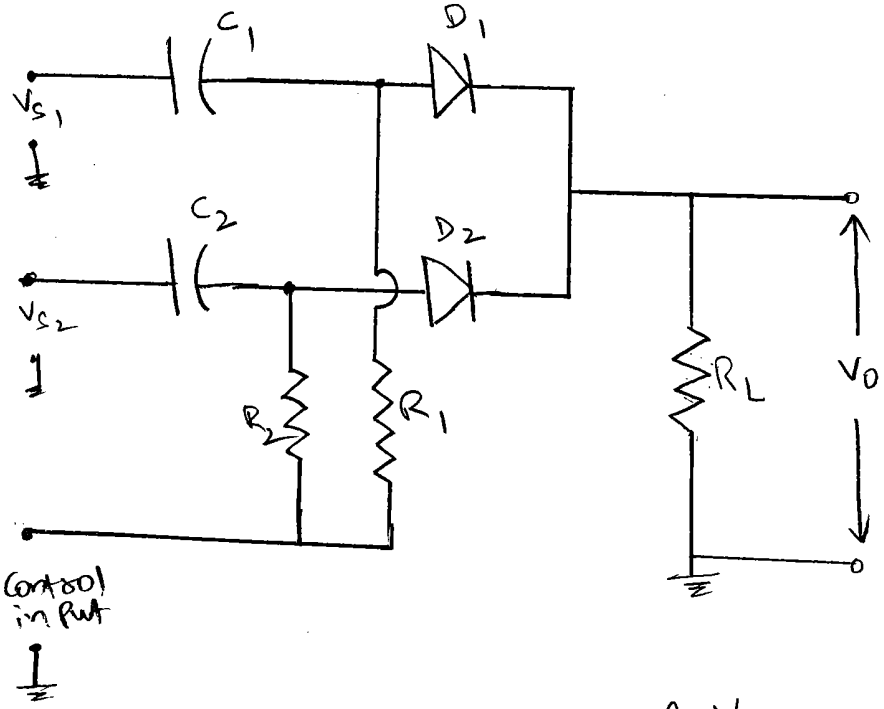
However if the input signal is a pulse whose width is very small as compared to the gate width, the input may be transmitted satisfactory at the output as is shown below:



Uni-directional diode gate for more than one input signal

The uni-directional sampling gate may be adopted to accept more than one signal input.

Uni-directional sampling gate with two input signals is shown below:



→ The two inputs are V_{s_1} and V_{s_2}.

→ The gate voltage has two levels; a higher level which is usually zero and a lower level which is negative.

→ When the gate signal is at lower level, the diodes are heavily reverse-biased and there is no conduction through them, the output voltage is zero. Hence, the negative level of the

Advantages of Uni-directional gate:

1) It is very simple gate.
2) The time delay is quite small, since the input is coupled directly to the output through C_1 and diode.
3) The gate draws no current in its quiescent condition.
4) This gate can be easily extended into a multi-input OR circuit with an INHIBITOR or NOT terminal.

Disadvantages of Uni-directional gate:

1) There is undesirable interaction between the input signal source and the gate voltage source.
2) The gate is of limited use because of the slow rise of the gate voltage at the diode.

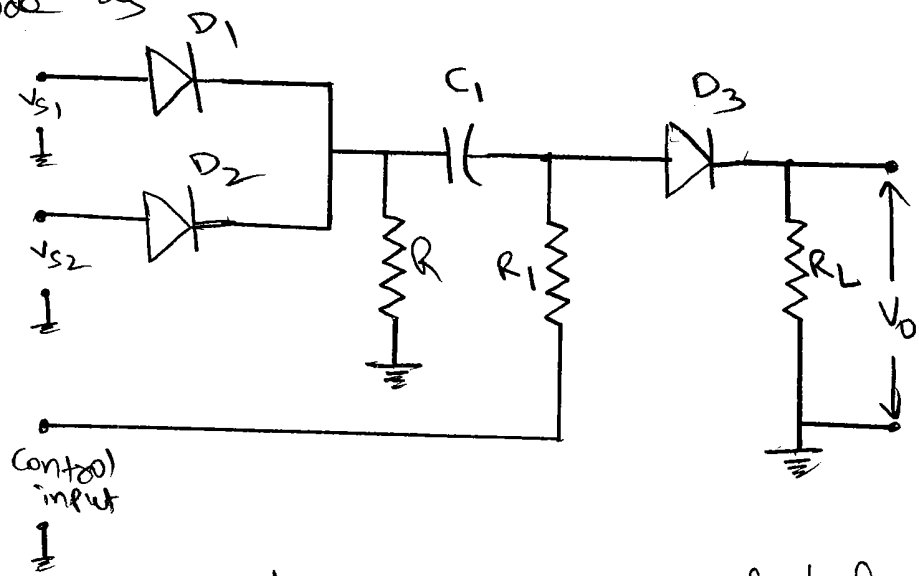
control pulse may be considered as inhibitor signal.

→ when the control signal is at its higher level (ie; 0V) the diode get forward biased (assuming the input signals to be positive pulses) and hence they conduct and the circuit is recognized as a capacitively coupled 2-input OR gate with lower level of the gate signal as an inhibitor signal.

Drawback:

As the number of inputs increases, the loading on the gate input increases heavily.

→ This difficulty can be solved by using additional diode as shown below.

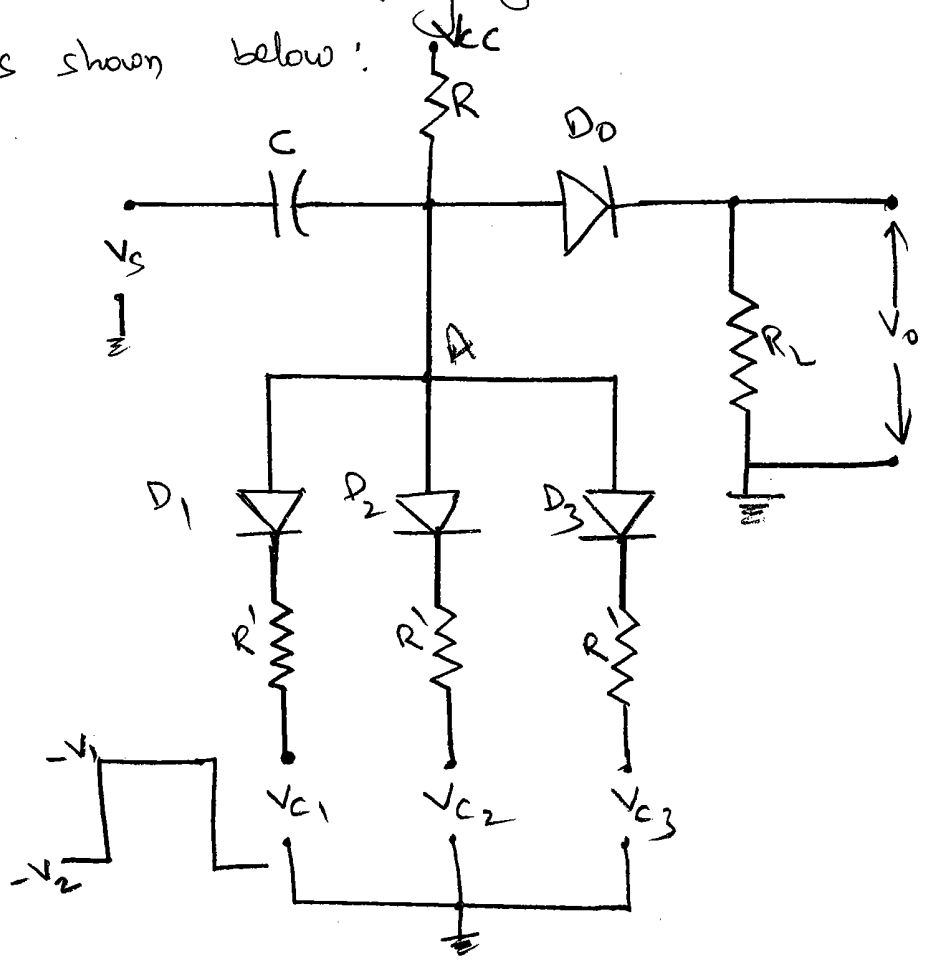


sampling gate which avoids loading of gate signal

Here, the gate input voltage does not feed into the signal sources. Therefore by using above circuit it is possible to increase the number of input signals without encountering difficulties.

Sampling gate with multiple gate signals

The diode sampling gate with multiple gate signals is shown below:



In this the input signal is transmitted to the output only when all gate inputs are at their highest voltage levels.

→ When all the gate signal inputs are at their higher voltage levels ($-V_1$), the back bias on the diode D_0 is removed and the input signal is transmitted at the output.

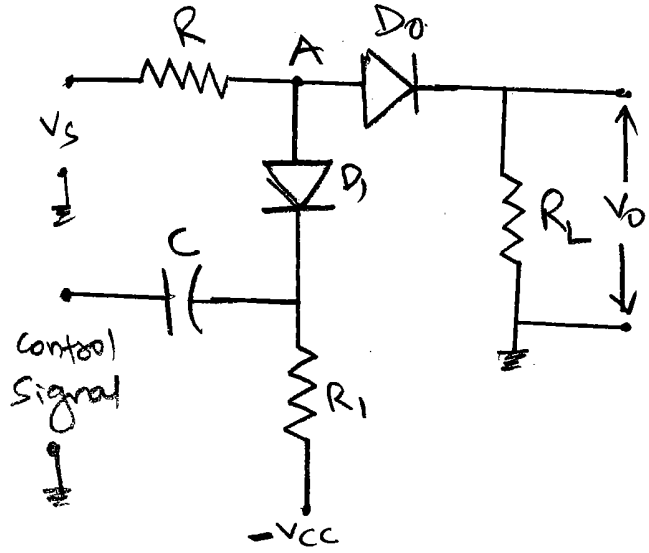
→ When any one of the gate signal V_c is at lower level ($-V_2$), the point A is negative with respect to the ground by an amount say V' and no part of the input waveform is transmitted unless the input signal is larger than this back-bias voltage (V') at point A.

→ This circuit is called as AND circuit.

Sampling gate not sensitive to the upper level of the control voltage

In earlier circuits it is observed that, if the higher level of the gate signal is not exactly zero, either there is attenuation of the input signal or the output signal gets superimposed on a pedestal.

A gate whose response is not sensitive to the upper level of the control voltage is shown below:



→ In the absence of the control signal, diode D_1 is forward-biased and hence it conducts. The current through R develops a large voltage drop across it with the result that the voltage at A is less than the cut-in voltage of D_0. Hence there is no conduction through D_0 and the output is zero.

→ If a positive going control signal is applied, it is evident that the diode D_1 gets reverse-biased and hence conduction through it stops. Diode D_0 gets forward biased and as a result the input signal gets transmitted through the circuit for the duration of the control signal.

→ For proper functioning of the gate, it is essential that the input signal is D.C Coupled (Resistor R), but the control signal may be either A.C coupled or D.C coupled.

Bi-directional sampling gates

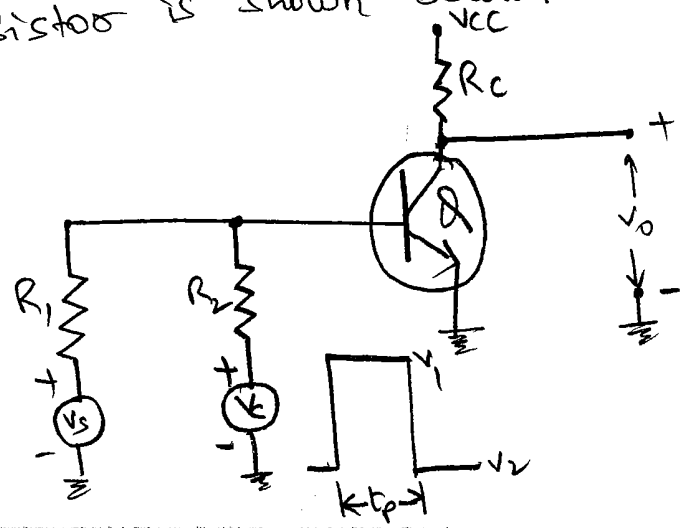
→ The Uni-directional gates have limitation that they transmit signals of only one polarity. ie; either positive signals or negative signals.

→ Bidirectional gates can pass the signal of both the polarities.

Bidirectional gates can be constructed by using transistors (or) diodes.

Bi-directional sampling gate using transistor

A linear bidirectional sampling gate using transistor is shown below:



→ The signal voltage V_s and the control voltage V_c are applied through the summing resistors R_1 and R_2 to the base of a transistor.

→ The gate signal is a pulse waveform having voltage levels V_1 and V_2 with a pulse width t_p equal to the required transmission interval duration.

→ When the gating signal V_2 is applied to the base of the transistor through resistor R_2, it biases the transistor well below cut-off. Hence there is no conduction and no transmission of input signal at the output.

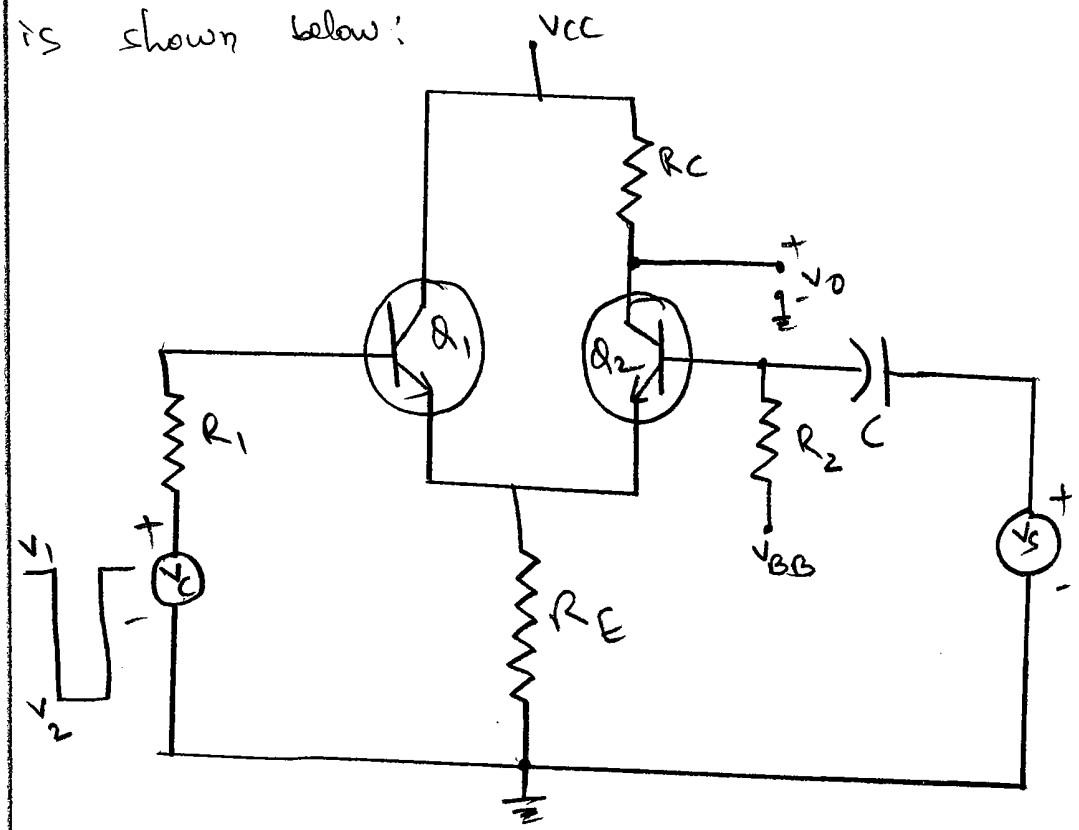
→ When the gate voltage is at its higher level V_1, the transistor is biased above the cut-off to drive the transistor in active region.

Since the transistor is in the active region, the input signal is sampled for the duration of the gate pulse, and it appears in an amplified form at the output.

→ Thus, this gate can handle the excursions of the input signal V_s in both positive and negative directions -

Bidirectional Sampling gate using two transistors

The Bidirectional sampling gate using two transistors is shown below:



→ In the previous circuit both the input signal and the control signal are applied to a common base.

This circuit provides separate bases for the two voltages.

→ The gate signal has two levels; a higher level V_1 and a lower level V_2.

→ When the control voltage V_C is at its upper level V_1, Q_1 becomes ON and the resulting emitter current through Re is large and the voltage drop across it causes the potential of the emitter of Q_2 to rise such that Q_2 becomes cut-off. Hence there is no transmission of the input signal to the output.

→ When the control voltage is at its lower level V_2, Q_1 is cut-off and Q_2 is free to operate as an amplifier. Thus it transmits the input signal in the amplified form at the output for the duration of the gating signal.

Advantages:

During sampling interval (ie; transmission of the input signal) transistor Q_1 is cut-off and hence there is no coupling between the input signal and the gating signal source. This reduces the loading effect on the signal source.

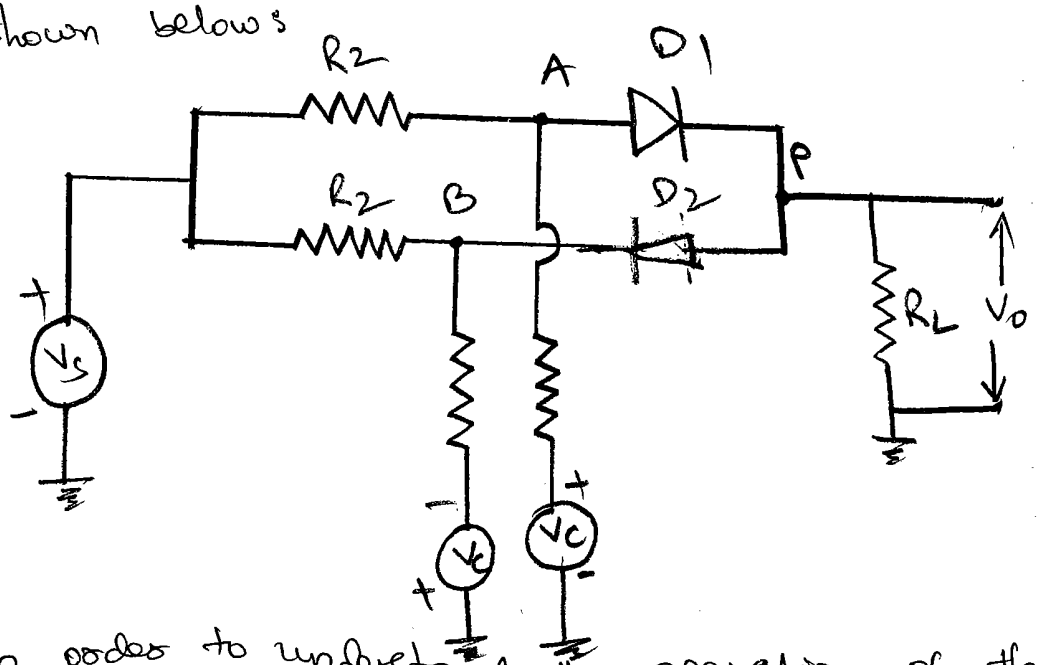
Bi-directional Diode sampling gate

A Bi-directional sampling gate may be constructed with the use of diodes instead of transistors.

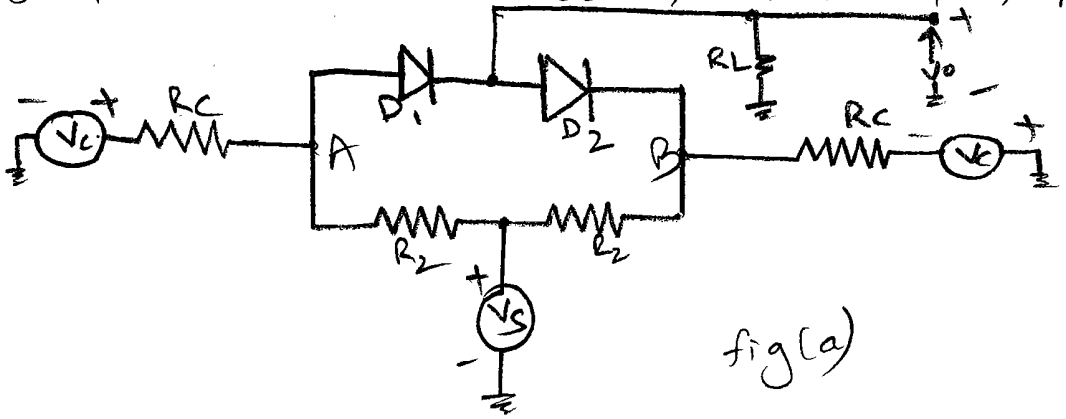
Advantages of Diode gates

1) The linearity of operation.
2) Ease of adjustment to get zero pedestal.

A Bi-directional two-diode sampling gate is shown below:



In order to understand the operation of the sampling gate, the circuit is redrawn in the form of a bridge



fig(a)

→ The circuit consists of two symmetrical gate signals $+V_G$ and $-V_G$.

→ i) when the gate voltage levels are such that the voltage at point A is negative ($-V_G$) and at point B is positive ($+V_G$) then both the diodes D_1 and D_2 are reverse biased and hence there is no transmission of signals V_S.

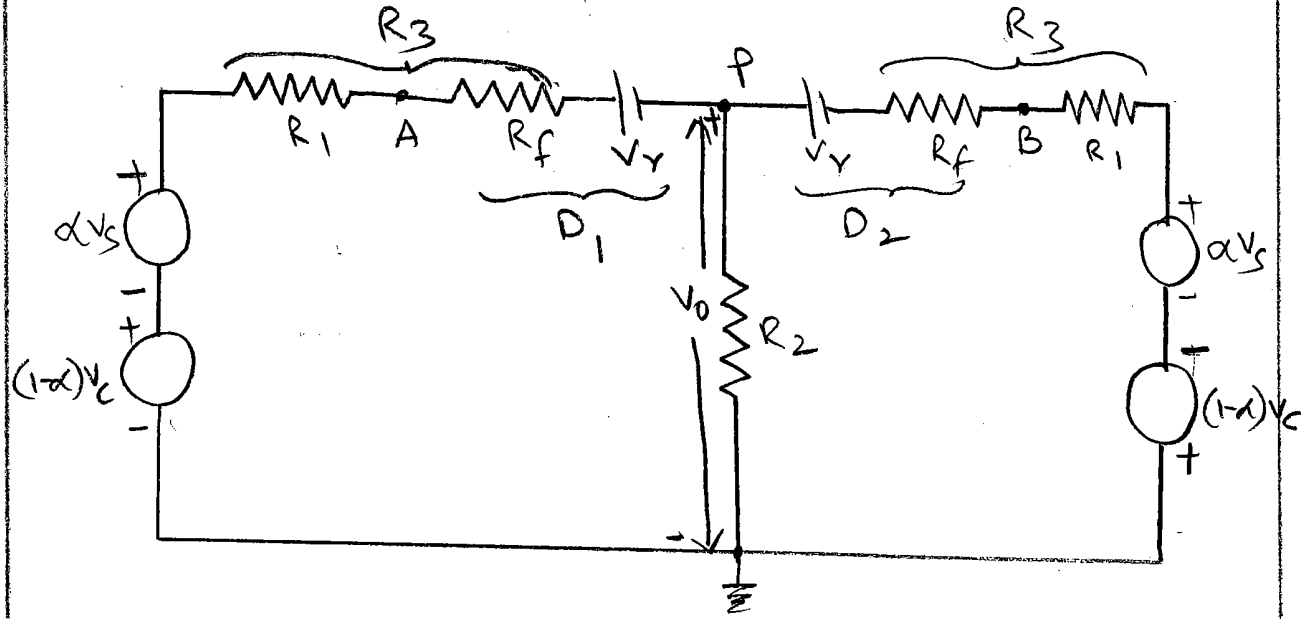
→ ii) when the gate voltages are such that the voltage at point A is positive ($+V_G$) and the voltage at point B is negative ($-V_G$), then both the diodes D_1 and D_2 are ON. As a result, there is a transmission of input signal for the duration of gate pulses.

→ It is important to note that the diodes should be identical in characteristics to maintain the complete symmetry of the circuit so that no pedestal can appear at the output in response to the gating voltages.

i) Gain of the sampling gate

"The gain of the sampling gate is defined as the ratio of $\frac{V_o}{V_s}$ during the transmission interval."

This can be easily calculated from the equivalent circuit derived from above figure by applying Thevenin's theorem at point A and B and replacing the diodes with its piecewise linear model:



R_f = forward resistance of the diode.

V_r = cut-in voltage of the diode.

$$R_1 = R_2 \| R_c = \frac{R_2 R_c}{R_2 + R_c}$$

$$R_3 = R_1 + R_f$$

$$\alpha = \text{Attenuation} = \frac{R_1}{R_2} = \frac{R_c}{R_2 + R_c}$$

$$V_A = V_C \times \frac{R_2}{R_2+R_C} + V_S \times \frac{R_C}{R_2+R_C}$$

but $\frac{R_C}{R_2+R_C} = \alpha$, $1-\alpha = 1 - \frac{R_C}{R_2+R_C}$

$$= \frac{R_2+R_C-R_C}{R_2+R_C} = \frac{R_2}{R_2+R_C}$$

$$\boxed{V_A = V_C(1-\alpha) + V_S\alpha}$$

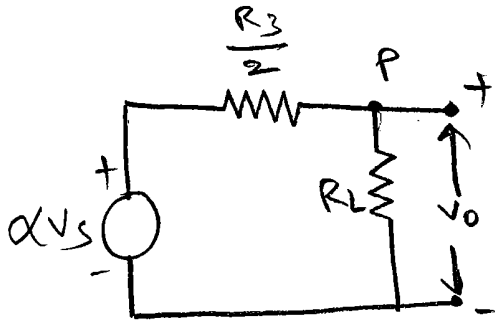
$$V_B = -V_C \times \frac{R_2}{R_2+R_C} + V_S \times \frac{R_C}{R_2+R_C}$$

$$\boxed{V_B = \alpha V_S - (1-\alpha)V_C}$$

. From the equivalent circuit of above fig, we observe that the offset voltages (V_γ) and gate voltage components $[(1-\alpha)V_C]$ sends equal currents in opposite directions through R_L.

Hence the net current R_L due to them is zero. Therefore open circuit voltage at point P with respect to ground is αV_S.

Thevenin's equivalent circuit between the point 'P' and ground is shown below:



Thevenin's equivalent circuit

The open circuit voltage from P to ground is αV_s and thevenin's resistance is $\frac{R_3}{2}$.

The output voltage $V_0 = \alpha V_s \times \frac{R_L}{R_L + \frac{R_3}{2}}$

but $\alpha = \frac{R_c}{R_2 + R_c}$

$$V_0 = \left[\frac{R_c}{R_2 + R_c}\right] V_s \left[\frac{R_L}{R_L + \frac{R_3}{2}}\right]$$

$$\therefore \boxed{\text{Gain } (A) = \frac{V_0}{V_s} = \left[\frac{R_c}{R_2 + R_c}\right]\left[\frac{R_L}{R_L + \frac{R_3}{2}}\right]}$$

ii) Gate / Control voltage V_c:

for proper operation of the sampling gate it is necessary to conduct both the diodes over the full range of the input signal and both diodes should be back biased when no sampling takes place.

These criteria's impose two restrictions on the control voltage levels:

1) minimum positive control voltage level $(V_c)_{min}$
2) Initially, in the presence of only gate voltages, Diodes D_1 and D_2 conduct equal currents, Hence the load current is zero and the pedestal is zero.
3) Assume, that V_s is a positive going signal, then the current in D_1 increases and the current in D_2 decreases, hence the difference current flows through R_L. As V_s continues to increase eventually, the current in D_2 becomes zero i.e; D_2 will be cut-off.

(a) Determination of minimum positive control voltage level $(V_c)_{min}$:

→ To maintain conduction of D_2, there is a restriction on the minimum value of the positive level of control voltage, when signal voltage attains a maximum voltage V_s.

→ To complete the required minimum positive voltage $(V_c)_{min}$, assume that diode D_2 has just stopped conducting. Then from equivalent

circuit, the voltage across R_3 associated with D_2 is zero and neglecting V_r i.e, $V_r = 0$, the output voltage is given by

$$V_0 = \alpha V_s - (1-\alpha) V_c \quad \text{---Considering right loop.}$$

Since R_3 across D_2 = zero

~~but~~

$$V_0 = \left[\alpha V_s + (1-\alpha) V_c\right] \frac{R_L}{R_L + R_3} \quad \text{---Considering left loop}$$

equating two equations for V_0

$$\left[\alpha V_s + (1-\alpha) V_c\right] \frac{R_L}{R_L+R_3} = \alpha V_s - (1-\alpha) V_c$$

$$\alpha V_s \times \frac{R_L}{R_L+R_3} + (1-\alpha) V_c \times \frac{R_L}{R_L+R_3} = \alpha V_s - (1-\alpha) V_c$$

$$(1-\alpha) V_c \left[\frac{R_L}{R_L+R_3} + 1\right] = \alpha V_s \left[1 - \frac{R_L}{R_L+R_3}\right]$$

$$(1-\alpha) V_c \left[\frac{R_L + R_3 + R_L + R_3}{R_L + R_3}\right] = \alpha V_s \left[\frac{R_L + R_3 - R_L}{R_L + R_3}\right]$$

$$(1-\alpha) V_c \left[2R_L + R_3\right] = \alpha V_s \left[R_3\right]$$

substitute $\alpha = \frac{R_C}{R_2 + R_C}$

$$\left[1 - \frac{R_C}{R_2+R_C}\right] V_c \left[2R_L + R_3\right] = \left[\frac{R_C}{R_2+R_C}\right] V_s R_3$$

$$V_c(2R_L+R_3) - \frac{R_C}{R_2+R_C} \times V_c (2R_L+R_3) = \frac{R_C V_s R_3}{R_2+R_C}$$

$$\frac{V_C(2R_L+R_3)R_2 + V_C(2R_L+R_3)R_C - V_C(2R_L+R_3)V_C}{R_2+R_C} = \frac{R_C V_S R_3}{R_2+R_C}$$

$$R_2 V_C[2R_L+R_3] = R_C R_3 V_S$$

$$\therefore \boxed{V_C = \frac{R_C}{R_2} \cdot \frac{R_3}{2R_L+R_3} V_S = (V_C)_{min}}$$

→ This is the minimum positive value of the control voltage required to ensure signal transmission over the full range of the input signal by keeping both the diodes conducting.

→ from the above equation, $(V_C)_{min}$ decreases with increasing R_L.

$$(V_C)_{min} \propto \frac{1}{R_L}$$

However we cannot increase R_L beyond certain limit, because increase in R_L increase $R_L C$ time constant where C = stray capacitance across the output terminals.

As $R_L C$ increases, more time is required to decay output voltage to zero value when the diode cut-off at the end of the gating signal.

Determination of minimum negative control voltage level $(V_{C1})_{min}$:

→ During no sampling period both the diodes should be back-biased. But if negative control voltage is not sufficient enough then at the maximum voltage of the input signal diode D_1 may be forward biased.

→ So, to ensure that both diodes are back-biased (off) when no sampling is to take place these should be minimum negative value of the control voltage.

→ when both the diodes are reverse-biased, point P in equivalent circuit is at ground potential.

∴ voltage across D_1 is

$$\alpha V_s - (1-\alpha) V_C$$

So, for D_1 to be reverse biased, this voltage must be either negative or in worst case zero.

$$\therefore \alpha V_s - (1-\alpha) V_C = 0$$

$$\alpha V_s = (1-\alpha) V_C$$

$$V_C = \frac{\alpha V_s}{1-\alpha}$$

sub $\alpha = \frac{R_C}{R_2+R_C}$

$$V_C = \frac{\frac{R_C}{R_2+R_C} V_S}{1 - \frac{R_C}{R_2+R_C}}$$

$$V_C = \frac{V_S R_C}{\frac{R_2+R_C}{R_2+R_C-R_C}}$$

$$\frac{R_2+R_C-R_C}{R_2+R_C}$$

$$\therefore \boxed{V_C = \frac{R_C}{R_2} V_S = (V_{Cn})_{min}}$$

This is the minimum negative value of the control voltage required to ensure back-biased (off) of the diode during no sampling period.

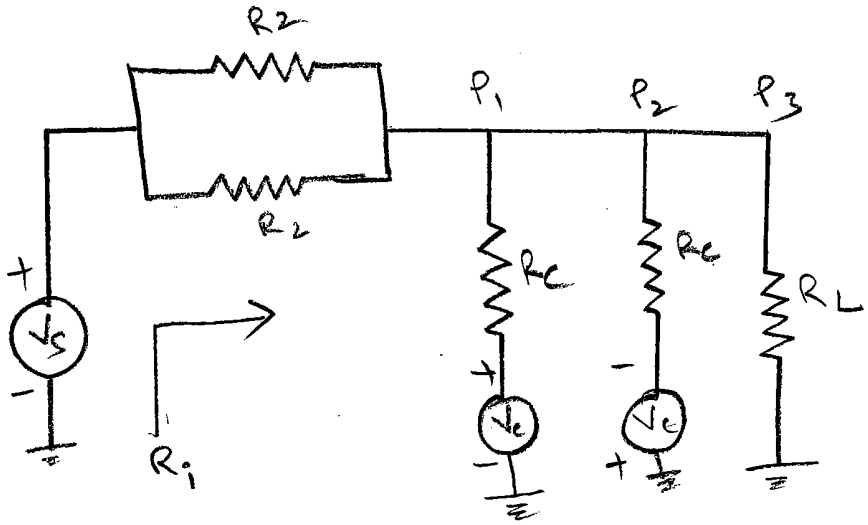
→ In practice, larger values of $(V_{Cp})_{min}$ and $(V_{Cn})_{min}$ are chosen.

→ A larger value of $(V_{Cp})_{min}$ improves linearity in addition to safety.

iii) Signal input Resistance (R_i):

Sol: Assume Ideal diodes ie; $R_f = 0$, $R_\sigma = \infty$, $V_r = 0$

I) when diodes are conducting:

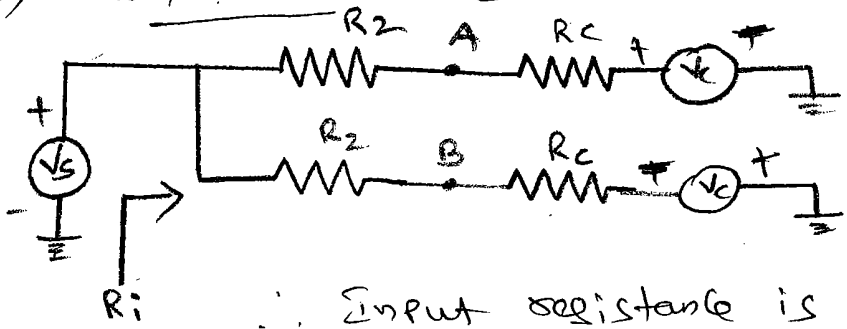


∴ Input resistance is

$$R_i = \left[\frac{R_c}{2} \,//\, R_L\right] + \frac{R_2}{2}$$

$$\boxed{R_i = \frac{R_c R_L}{R_c + 2R_L} + \frac{R_2}{2}}$$

II) when diodes are not conducting:



∴ Input resistance is

$$R_i = (R_2 + R_c) \,//\, (R_2 + R_c)$$

$$\boxed{R_i = \frac{R_2 + R_c}{2}}$$

Problem: In a bidirectional diode sampling gate, assume that $R_L = R_C = 100k\Omega$, $R_2 = 50k\Omega$ and that the signal has a peak value of 20V. Find.
a) Gain A, b) $(V_{cp})_{min}$ c) $(V_{cn})_{min}$ d) R_i and e) 3-dB frequency of the gate. (Assume total shunting capacitance of 20pf)

Sol: Assume diodes are perfect and ideal

a) $\text{Gain } (A) = \left[\frac{R_C}{R_C + R_2}\right]\left[\frac{R_L}{R_L + \frac{R_3}{2}}\right] = 0.57$

b) $(V_{cp})_{min} = \frac{R_C}{R_2}\left[\frac{R_3}{R_3 + 2R_L}\right] V_S = 5.7V$

c) $(V_{cn})_{min} = \frac{R_C}{R_2} \times V_S = 40V$

d) $R_i = \frac{R_C + R_L}{R_C + 2R_L} + \frac{R_2}{2} = 58k\Omega$ (when diodes are conducting)

$R_i = \frac{R_2 + R_C}{2} = 75k\Omega$ (when diodes are not conducting)

e) 3-dB frequency $(f_2) = \frac{1}{2\pi\tau}$

when $\tau = RC$

$\tau = \left[\frac{R_1 R_L}{R_1 + 2R_L}\right](C_0 + 2C_S)$

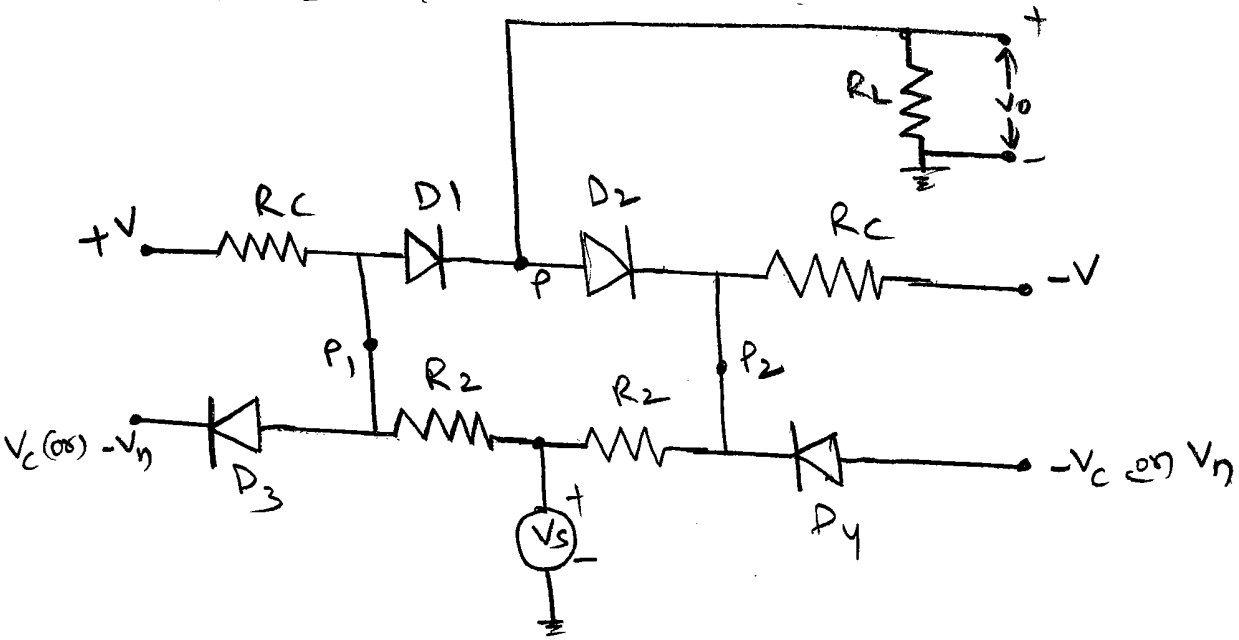
$\tau = 0.29\mu S$

$f_2 = \frac{1}{2\pi \times 0.29 \times 10^{-6}}$

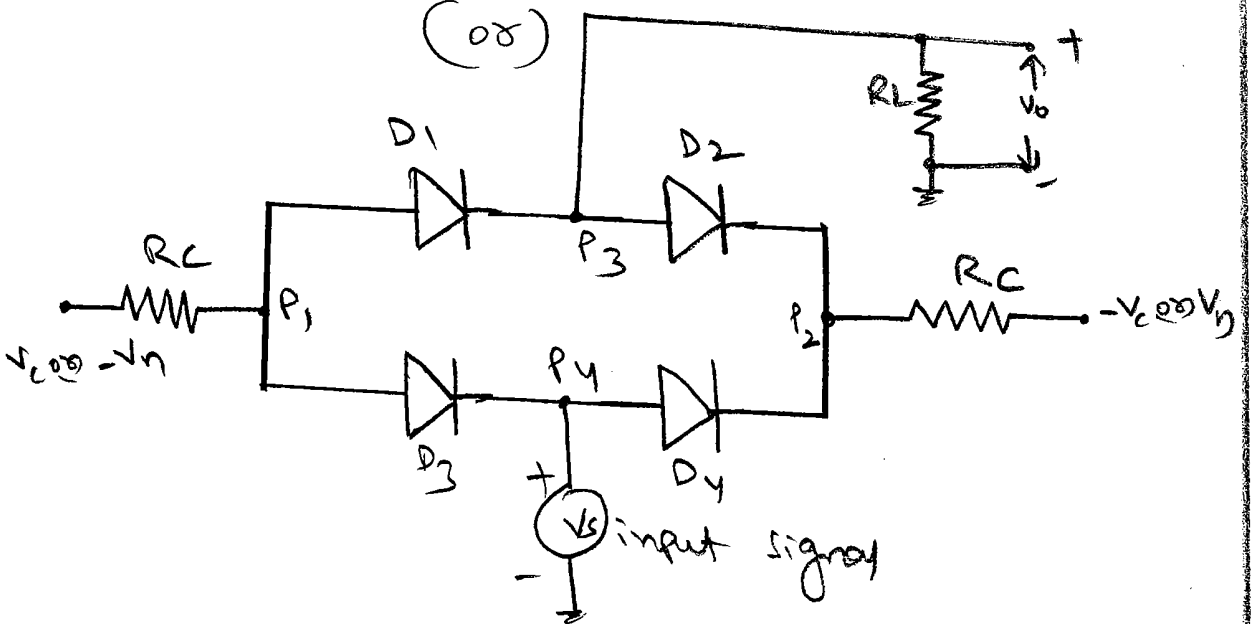
$f_2 = 0.55 MHz$

Four-Diode sampling gate

The disadvantages of two-diode sampling gate may be improved by the use of two additional diodes as shown below:



(or)



Operation :

1) When the control voltages are at levels V_C and $-V_C$, All four diodes are forward biased and so the input signal is connected through two parallel paths each consisting of two diodes in series. So, signal transmission takes place.

2) When control voltages are at levels V_h and $-V_h$, all four diodes are off, so no signal transmission takes place

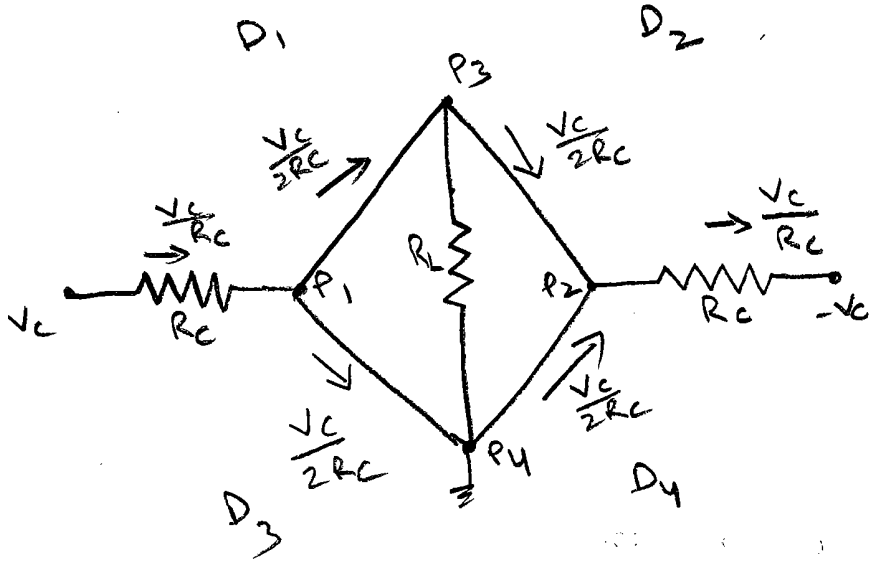
$\therefore V_o = 0$.

→ The required voltages V_C and $-V_C$ depend on the amplitude of the signal V_s and are determined by the condition that the current be in the forward direction in each of the diodes D_1, D_2, D_3 and D_4.

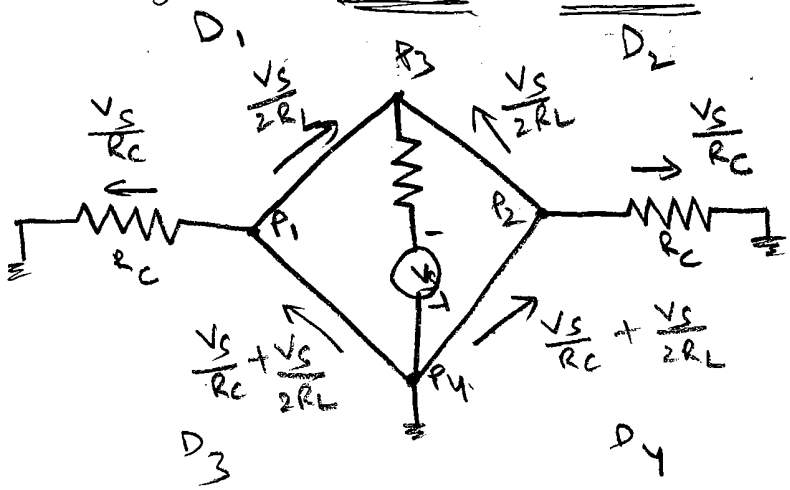
→ The current in each diode consists of two components:

1) Due to V_C as shown below fig (a).

2) Due to V_s as shown below fig (b).



fig(a): Current due to V_c



fig(b): Current due to V_s

→ The current due to V_c is $\frac{V_c}{2R_c}$ and is in the forward direction in each diode but the current due to V_s is in reverse direction in D_3 (between P_1 and P_4) and in D_2 (between P_3 and P_2).

→ The largest reverse current is in D_3 and is equal to $\frac{V_s}{R_c} + \frac{V_s}{2R_L}$. This current must be

less than $\frac{V_c}{2R_c}$ (which is due to V_c through D_3) so that D_3 conducts.

$$\therefore \frac{V_c}{2R_c} < \left(\frac{V_s}{R_c} + \frac{V_s}{2R_L}\right)$$

$$\frac{V_c}{2R_c} > V_s\left[\frac{1}{R_c} + \frac{1}{2R_L}\right]$$

$$\frac{V_c}{2R_c} > V_s\left[\frac{2R_L + R_c}{2R_cR_L}\right]$$

$$V_c > V_s \times 2R_c\left[\frac{2R_L + R_c}{2R_cR_L}\right]$$

$$V_c > V_s\left(2 + \frac{R_c}{R_L}\right)$$

∴ minimum value of V_c required to keep D_3 ON is

$$\boxed{(V_c)_{min} = V_s\left[2 + \frac{R_c}{R_L}\right]}$$

Hence it is assumed that $R_f << R_c$ or R_L.

→ If R_f and R are $<< R_c$ and R_L, gain will be very close to unity $\therefore \boxed{A \simeq 1}$

→ when the control voltages are V_n and $-V_n$ then all the diodes are reverse biased.

If the signal has a peak amplitude V_s, then the minimum voltage required at P_2 to keep D_4 off is $\boxed{(V_n)_{min} = V_s}$

problems:

(1) Assume $V_s = 20V$, $R_f = 25\Omega$, $R_L = R_C = 100K\Omega$ and $R = 100\Omega$. Find A, $(V_C)_{min}$ and $(V_n)_{min}$ for four-diode gate?

Sol: a) $(V_C)_{min} = V_s \left[2 + \frac{R_C}{R_L}\right]$

$$(V_C)_{min} = 20\left[2 + \frac{100K\Omega}{100K\Omega}\right]$$

$$= 20\left[2+1\right] = 20 \times 3$$

$$(V_C)_{min} = 60\,V$$

(or)

~~$(V_C)_{min} = \frac{R_C}{R}$~~.

b) $A \cong 1$ $\because$ R_f and $R \ll R_C$ and R_L

c) $(V_n)_{min} = V_s = 20V$

(2) In the ~~four~~ two-diode gate, Consider $R_L = R_C = 100K\Omega$ and $R_2 = 1K\Omega$. Assume $R_f = 25\Omega$, $V_s = 20V$, Compute A, $(V_n)_{min}$ and $(V_C)_{min}$?

Sol: a) $A = \frac{R_C}{R_C + R_2} \cdot \frac{R_L}{R_L + \left(\frac{R_3}{2}\right)}$

where $R_3 = R_1 + R_f = 1.96K\Omega + 25\Omega = 2.01\,K\Omega$

but $R_1 = \frac{R_2 R_C}{R_2 + R_C} = \frac{1K\Omega \times 100K\Omega}{1K\Omega + 100K\Omega} = 1.96K\Omega$

$$A = \frac{100K\Omega}{100K\Omega + 2K\Omega} \times \frac{100K\Omega}{100K\Omega + \left(\frac{2.01K\Omega}{2}\right)} = 0.97$$

b) $$(V_{cp})_{min} = \frac{R_C}{R_2}\left(\frac{R_3}{R_3 + 2R_L}\right) \cdot V_S$$

$$= \frac{100K\Omega}{2K\Omega}\left(\frac{2.01K\Omega}{2.01K\Omega + 2\times 100K\Omega}\right) \times 25$$

$$\therefore V_{cp(min)} = 12.43V$$

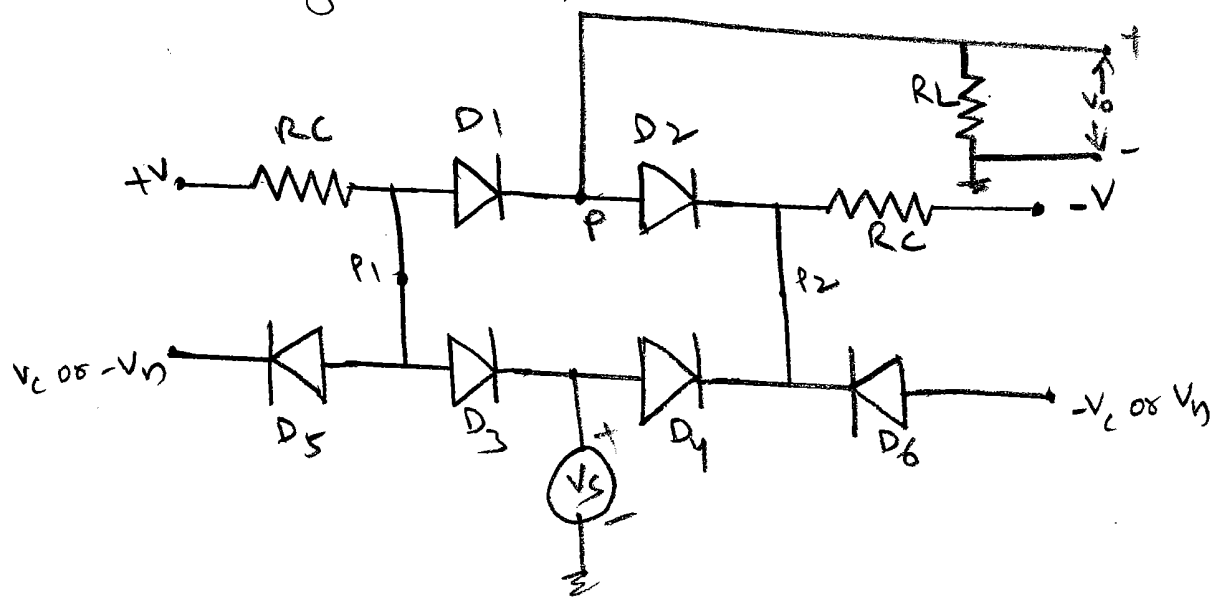
c) $$(V_{cn})_{min} = \frac{R_C}{R_2} \cdot V_S$$

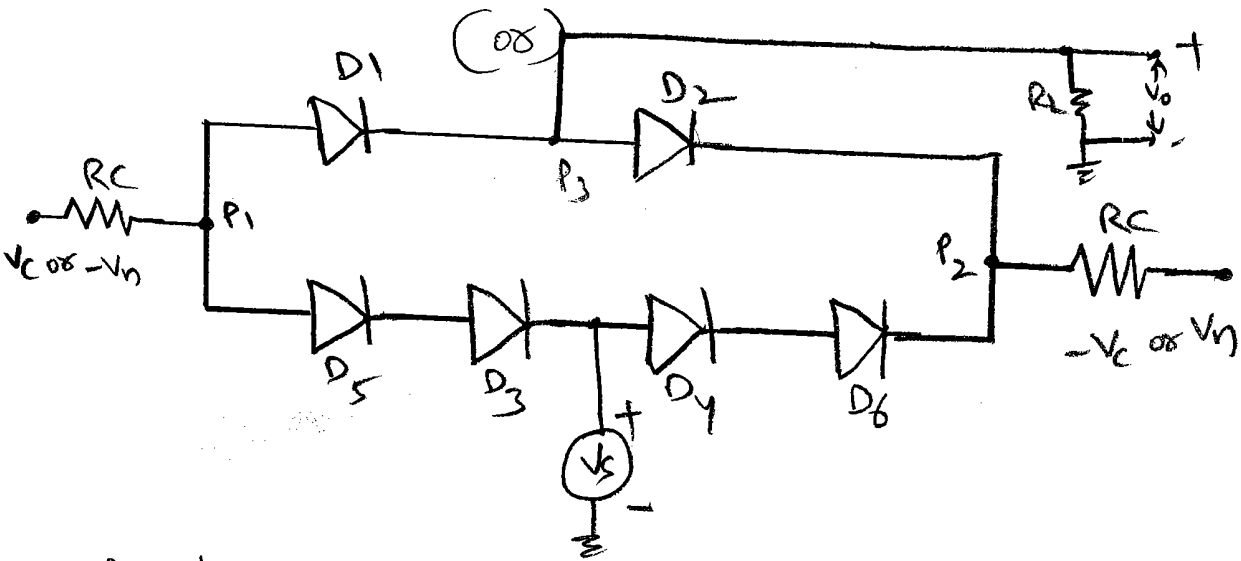
$$= \frac{100K\Omega}{2K\Omega} \times 25V$$

$$\therefore (V_{cn})_{min} = 1250V$$

Six-Diode sampling gate

This gate combines the features of two four-diode gate shown below.





Operation:

1) When control voltages are at the levels V_h and $-V_h$ then the diodes D_6 and D_5 are off and Six-diode gate becomes equivalent to four diode gate

2) When the control signals are at levels V_C and $-V_C$ diodes D_6 and D_5 conduct and the points P_2 and P_1 are clamped to these levels.

Hence D_3 and D_4 are back biased and signal transmission takes place.

$$\therefore \boxed{V_{min} = V_S \left[2 + \frac{R_C}{R_L}\right]}$$

→ $(V_C)_{min}$ for four diode gate or V_{min} for 6-diode gate may be as large as 168.75V for 25V signal.

Advantage:

Advantage of six-diode gate is that such a large voltage V_{min} needed appear only as a fixed voltage but not as a control signal as in four-diode gate.

Reduction of Pedestal in a Gate Circuit

→ In Bi-directional transistor sampling circuit, if no gating signal is applied the voltage level at the output is V_{CC}.

→ when the gating signal is applied, the transistor draws current and the output therefore establishes itself at a new lower quiescent level.

→ Now, when the signal is applied, the output signal is superimposed on this new quiescent level.

→ The appearance of the output during a gating interval is shown below, where the sampled portion of the signal is superimposed on a pedestal.

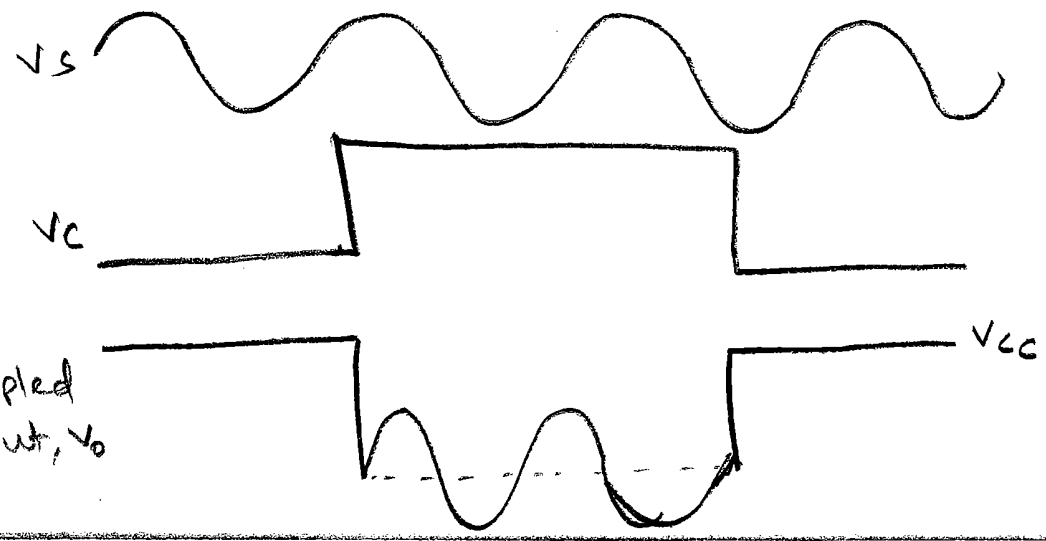
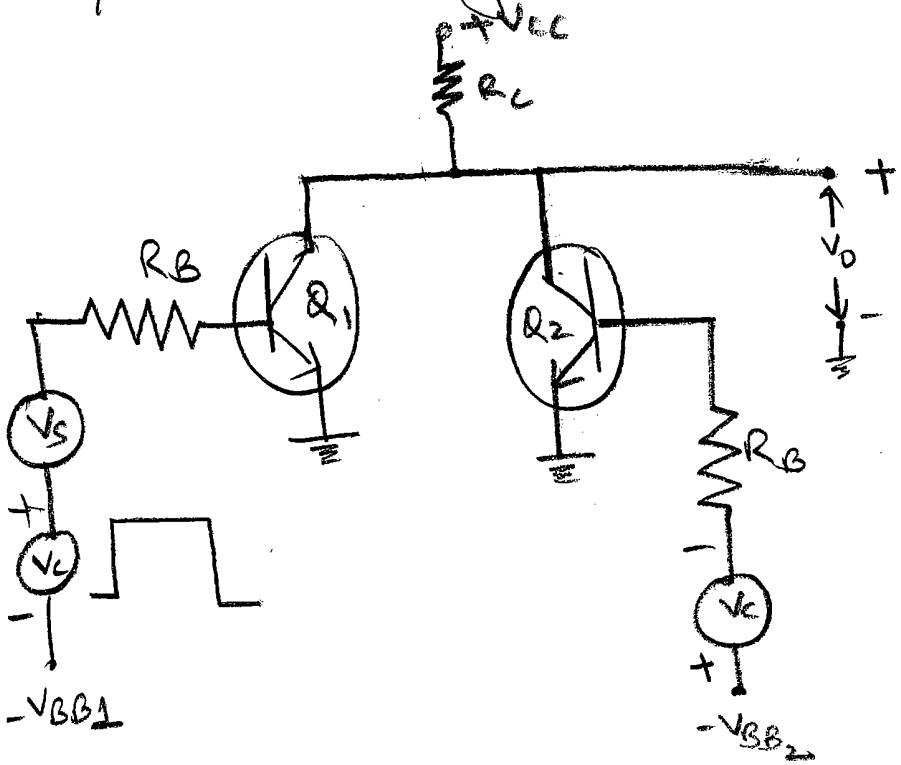


fig (a)

→ The pedestal can be largely suppressed by the symmetrical arrangement shown below:



b) A linear gate circuit with provision to cancel the pedestal.

→ In this, the gating and signal voltage have been placed directly in series.

→ A pair of transistors is used and the bases of transistors are driven by the gating signal of opposite polarity.

Q_1 = Gating transistor.

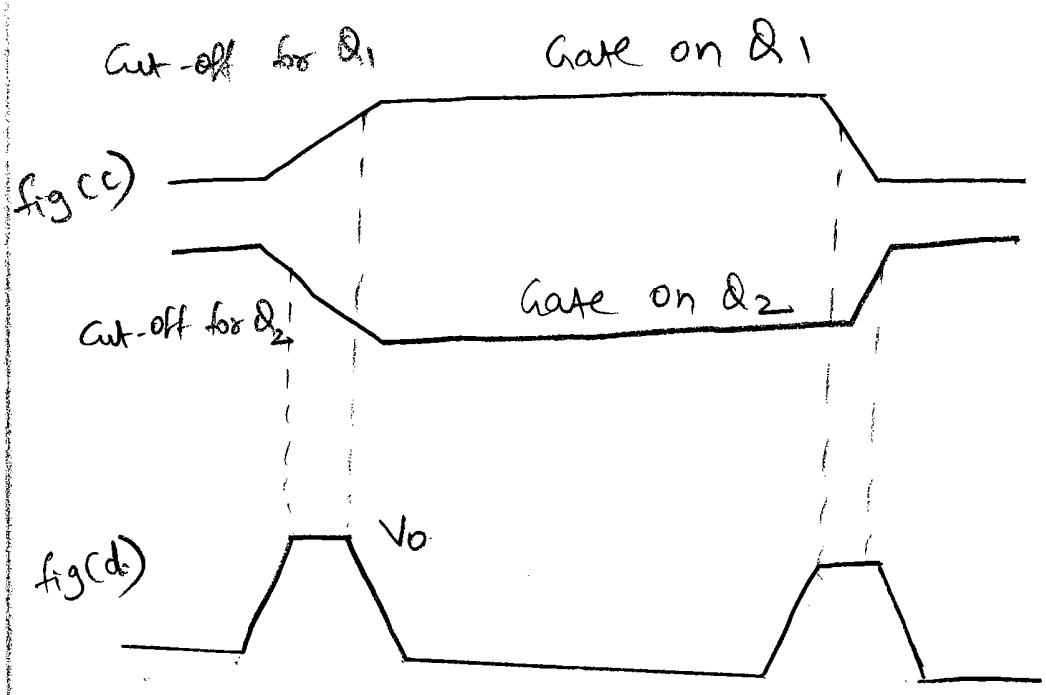
Q_2 = It is used to minimize the pedestal.

→ During the transmission time t_p i.e, when the control signal is at its upper level Q_1 conducts and Q_2 is cut-off. A current flows from V_{cc} through R_c and Q_1.

→ During no sampling time (non-transmission time) when the control signal is at its lower level, Q_1 is off and Q_2 conducts and a current flows from V_{cc} through R_c and Q_2.

The bias voltages $-V_{BB_1}$ and $-V_{BB_2}$ and the gate signal amplitudes are adjusted so that the two transistor currents are identical. As a result the quiescent output voltage level will remain constant.

→ If the gate voltage has finite rise time then the voltage spikes appear in the output. These spikes may not be objectionable if the gate waveform rise time is small in comparison with the gate duration.



fig(c): Gating waveform of fig(b) drawn with non-zero rise time

fig(d): Spikes which may occur in the output circuit of fig(b) due to gating waveform with non-zero rise time.

Drawbacks of fig(b):

1) If the gating waveform have definite rise and fall times, two sharp spikes are generated at the output.

2) There is a continuous flow of current through R_C and so it has to dissipate a lot of heat.

3) The circuit is complicated, since it requires two bias voltages i.e; $-V_{BB_1}$ & $-V_{BB_2}$ and two control signal sources which are complements of each other.

Effect of circuit Capacitance on bidirectional diode gate:

The capacitances which effect the operation of gate circuit has the following:

1) Capacitance C_o across the bidirectional sampling gate output terminals.
2) Capacitance C_d across each diode.
3) Stray capacitances C_s from each of the junctions of the resistors R_2 and R_c to ground.

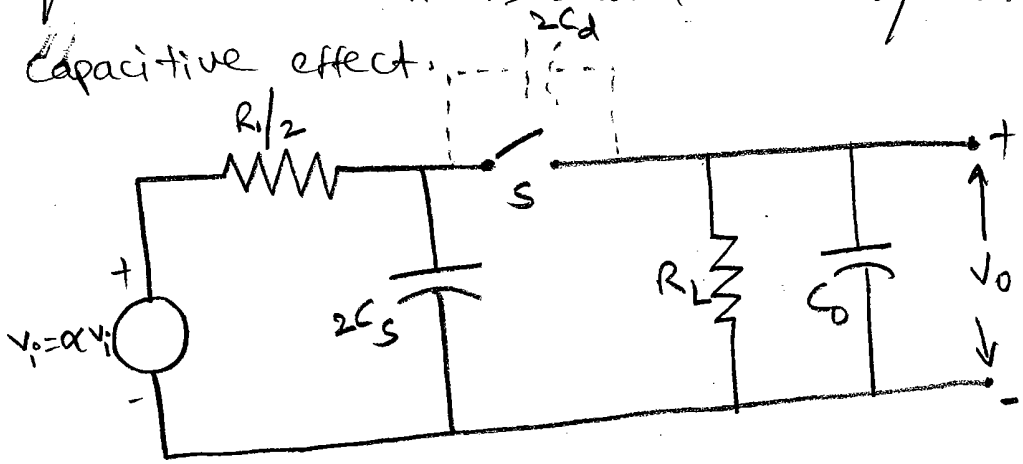
→ The capacitance C_o, has an adverse effect on the ability of the sampling gate to transmit fast waveforms due to finite rise time and fall time.

→ The capacitance C_s, not only affects the ability to transmit fast waveforms but also limits the speeds with which the gate can be opened and closed.

→ The diode capacitance C_d, provides a transmission path through the gate even when the diodes are not conducting.

→ Assuming $R_f = 0$, $R_r = \infty$ and ideal diode, when the diodes are forward biased, the

equivalent circuit is shown below by considering capacitive effect.



where $R_3 = R_1 + R_f \simeq R_1$

$$R_1 = \frac{R_2 R C}{R_2 + R C} \quad \text{and}$$

$$\alpha = \frac{R C}{R_2 + R C}$$

The circuit simply behaves as a low pass RC circuit whose time constant is RC where

$$R = \frac{R_1}{2} // R_L = \frac{\frac{R_1}{2} \times R_L}{\frac{R_1}{2} + R_L} = \frac{R_1 R_L}{R_1 + 2R_L}$$

$$C = C_0 + 2C_S \quad (\text{since switch is closed})$$

→ The residual transmission which results from the capacitance which shunts the diodes is calculated from above circuit by opening switch S and shunting across the switch a capacitance equal to the sum of the diode capacitances.

Disadvantages of two-diode gate:

1) Gain is low.
2) sensitive to control voltage imbalance.
3) There may be appreciable leakage through the diode capacitance.
4) There is a possibility that $(V_n)_{min}$ may be excessive.

Applications of sampling gate

1) Chopper Amplifier

→ One of the application of a sampling gate is chopper amplifier.

→ Need:

suppose a small signal (of the order of millivolts), v(t) having very small $\frac{dv}{dt}$ is to be amplified using

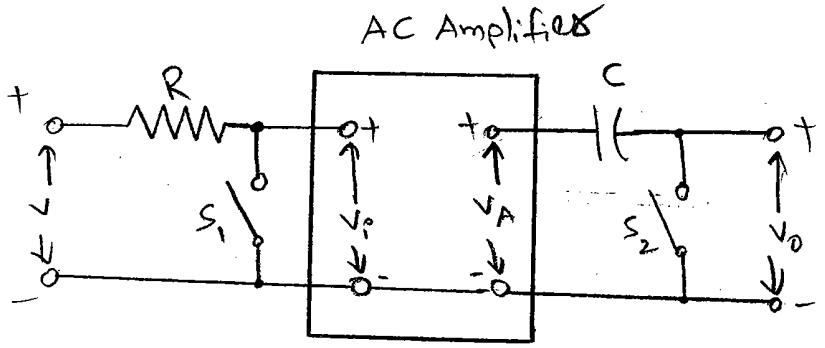
1) AC amplifier: coupling capacitors between stages would not be feasible, since these coupling capacitances would be impractically large.

2) DC amplifier: it is not possible to distinguish between a change in output voltage as the result of a change in

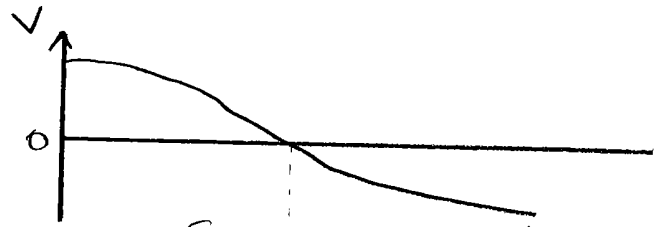
input voltage or as the result of a drift in some active device or component.

In this case a chopper amplifier can be used.

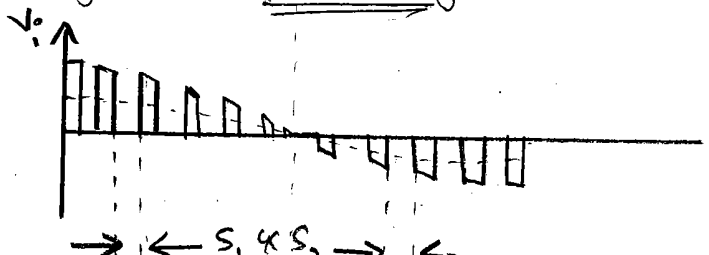
chopper stabilized amplifier is shown below fig(a).



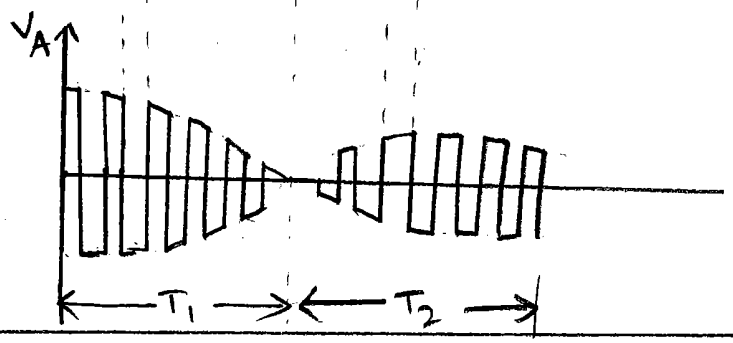
fig(a): A chopper stabilized Amplifier



fig(b): Input signal



fig(c): chopped signal



fig(d): signal-modulated square-wave

→ The low-frequency input signal $v(t)$ is shown in fig (b).

→ Assume that switch S_1 is being driven so that it is alternately open and closed. Then the signal $v_i(t)$ at the amplifier input will appear as shown in fig (c).

i.e; when S_1 = open, $v_i(t) = v(t)$

when S_1 = closed, $v_i(t) = 0$

so, the signal $v_i(t)$ is a "chopped" version of $v(t)$.

∴ The circuit consisting of R and S_1 is called <u>chopper</u>.

In fig (c), when the switch is open, the signal $v_i(t)$ reproduces the input signal $v(t)$. so, a perceptible voltage change takes place in $v(t)$ during any interval when S_1 is open. Thus, when $v(t)$ is positive, the positive extremities of the waveform $v_i(t)$ are not at a constant voltage and similarly for the negative extremities when $v(t)$ is negative. But this feature is in no way essential to the operation.

If the frequency of operation of the switch is very large (typically 100 times) in comparison with the frequency of signal v(t). Therefore no appreciable change takes place in v(t) during the interval when S_1 is open.

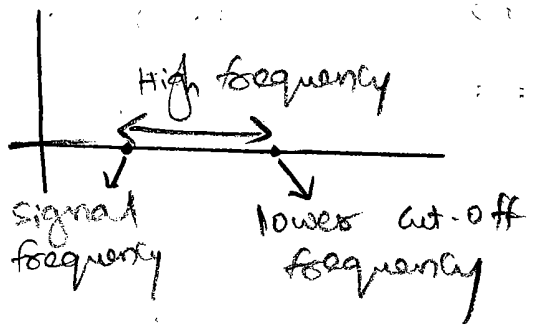
So, $V_i(t)$ may be considered as a square-wave of amplitude proportional to v(t) and having an average value (shown dashed in fig c) that is also proportional to the signal v(t). Alternatively, the signal $V_i(t)$ is a square wave at the switching frequency, amplitude-modulated by the input signal and superimposed on a signal which is proportional to the input signal v(t) itself.

→ Thus $V_i(t)$ is applied to an amplifier, if this AC amplified is designed to act as a filter to eliminate the signal itself i.e; average value from $V_i(t)$, then the chopper (or chopper together with a filter to eliminate the signal itself) is called a "modulator".

→ The output of this modulator is a modulated waveform as shown in fig (d). This is obtained by adjusting the low-frequency cut-off of AC amplified in such a way

that relatively high frequency square wave passes with small distortion while the signal frequency is well below the cut-off point so that it is rejected.

∴ At the output of the AC amplifier, only the modulated waveform as shown in fig (d) will appear.



→ The original signal is recovered through the mechanism of the capacitor 'C' and switch S_2.

Let the switch S_2 closes and opens in synchronism with S_1. Thus during the interval T_1, the negative extremity of $V_A(t)$ is restored to zero and during the interval T_2, the positive extremity is reduced to zero.

∴ Except for an increase in amplitude, the signal $v_0(t)$ across S_2 is same as the signal $v_i(t)$.

→ If this signal $V_0(t)$ is passed through a low-pass filter, it rejects the square wave (high frequency) and transmits the signal frequency.

→ At the filter output, amplified replica of the original signal is obtained.

→ If S_2 operates antisynchronously with S_1 (S_2 closed while S_1 is open and vice-versa) then at the output the signal will appear with reversed polarity.

→ In either case, the combination of the capacitor C, switch S_2 and the filter is called "Synchronous demodulator."

Note:

The amplifier is not stabilized by the choppers but rather the choppers eliminate the necessity for a direct-coupled stabilized amplifier.

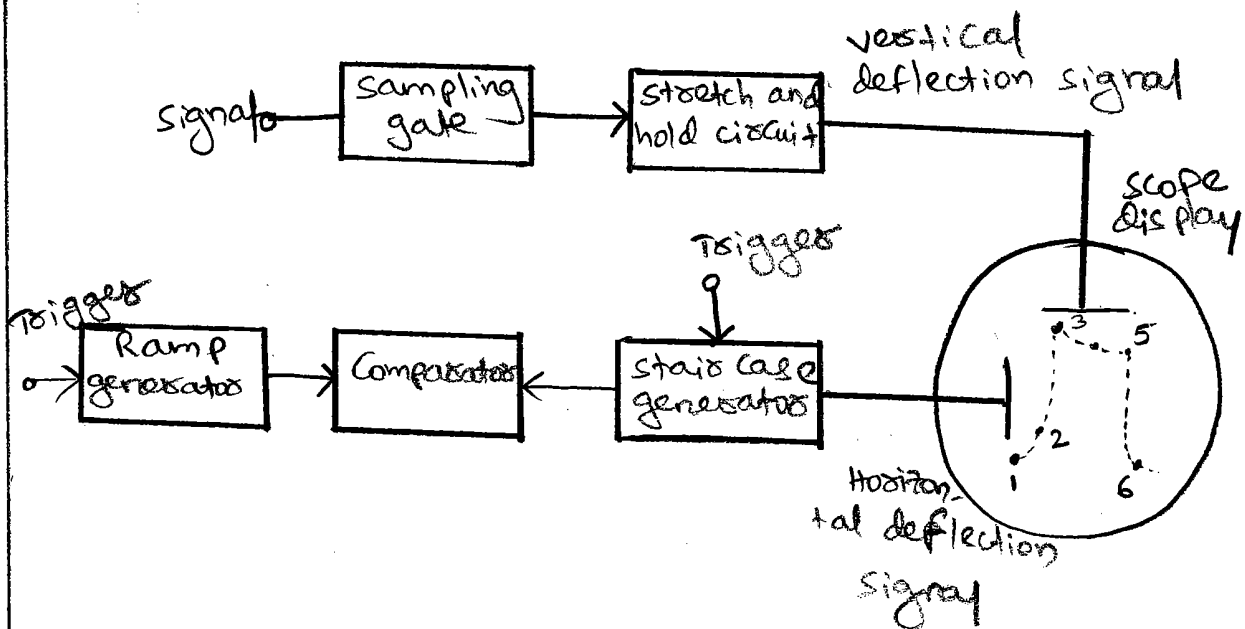
2) Sampling scope

→ An important application of a sampling gate is in sampling scopes.

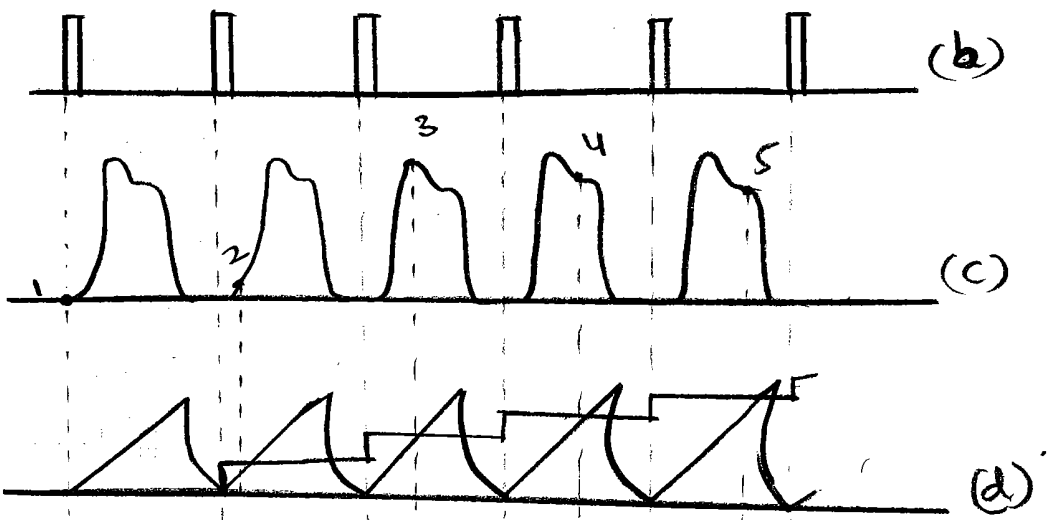
→ Basic principle of sampling scope:

In this scope, the display consists of a sequence of samples of the input waveform, each sample taken at a time progressively delayed with respect to some reference point in the waveform.

fig(a) shows the block diagram of a sampling scope:



fig(a): Block diagram of sampling-scope



b) Triggering signal

c) signal to be observed

d) The ramp and staircase signals

→ Assume that the waveform to be displayed is a pulse in the train of pulses as shown in fig (c).

→ fig (b) represents a train of triggers whose time of occurrence precedes somewhat the pulses. These triggers are used to trigger sweep and a stair step signal.

Operation:

→ The stair-step and ramp signals are applied to a comparator.

→ The stair-step serves as the reference voltage and in each cycle, whenever the ramp attains the stair-step level, the comparator produces a pulse output which is used as the control signal of the sampling gate.

→ At each such control signal, the gate produces its output a sample of the signal.

→ The sample having a duration equal to the width of the control pulse.

→ The control signal has so short a duration that during its interval no sensible change takes place in the input signal.

→ Thus the gate output, at each control signal, is a voltage equal to the signal voltage at the time of sampling.

→ The points at which samples are taken have been marked by dots 1, 2, ... as shown in fig (c).

→ It is seen that the samples are taken at a time, which is progressively delayed by equal increments.

→ The sample consist of a pulse whose duration is equal to the duration of the sampling gate control signal and whose amplitude is determined by the magnitude of the input signal at the sampling time.

→ This voltage must be hold till the next sample is taken. This holding operation may be obtained by applying the gate output to charge a capacitor through a diode to the peak value of the sample so that when the sample is completed, the capacitor holds its charge.

→ But the sample is so short in duration that it is not possible to charge a capacitor in this small interval.

→ Therefore, before the sample is applied to the "hold", diode - capacitor combination, it is first passed through an amplifier stage whose output time constant is large.

→ The sample pulse is thereby widened ie; "stretched" and now will have a much broader peak.

→ This stretching and holding operations are performed by the block so labelled in fig(a) before the sample is applied as a vertical-deflection signal to the scope. And before each new sample is to be taken, the hold capacitor must be discharged.

→ The stair-step signal generator produces the horizontal-deflection signal for the scope. Thus the CRT spot moves horizontally across the screen in jumps and at each new position, the spot is deflected vertically by an amount proportional to the sample height.

→ The CRT beam is normally blanked and is un-blanked only at the time of the display of the sample.

→ CRT screen consists of a series of dots which trace out the form of the original signal as shown in fig(a).

→ The sampling principle finds application in a scope used to display very fast periodic waveforms i.e, waveforms with rise times in the nanosecond range.

Logic families

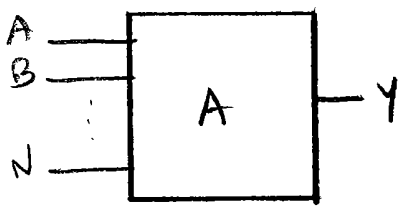
Realization of Logic Gates using Diodes & Transistors

1) Diode AND Gate: AND Gate is also called as Coincidence ckt.

→ An AND gate has two (or) more inputs and a single output.

→ "The output of an AND gate is 1 if and only if all the inputs assume 1 state".

→ The IEEE standard for AND circuit is given in fig (a) together with the Boolean expression for this gate.



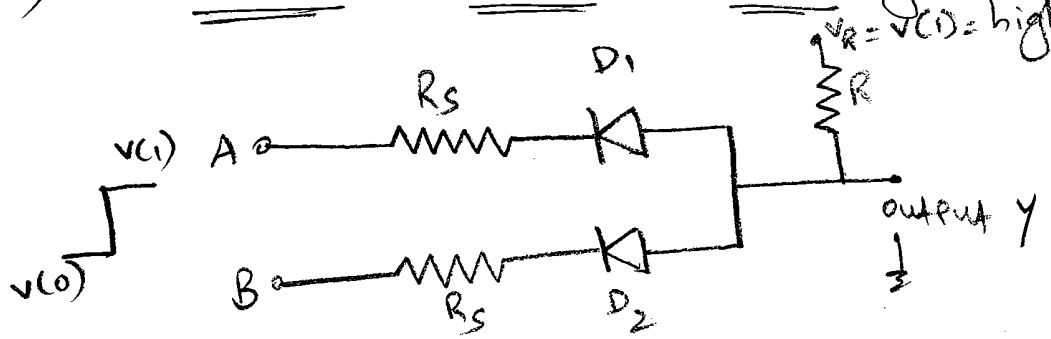
$Y = AB \cdots N$

fig (a): IEEE standard

Input		output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

fig (b): Truth table

a) Diode AND Gate for positive logic



Assume $R \gg R_s$ so that drop across R_s can be neglected.

Let $V(1)$ = voltage corresponding to logic 1 = $+V_{CC}$ = +5V

$V(0)$ = voltage corresponding to logic 0 = Ground or 0 V

V_R = Reference voltage

R_s = Source Resistance

Y = output of gate

D_1, D_2 = Identical diodes

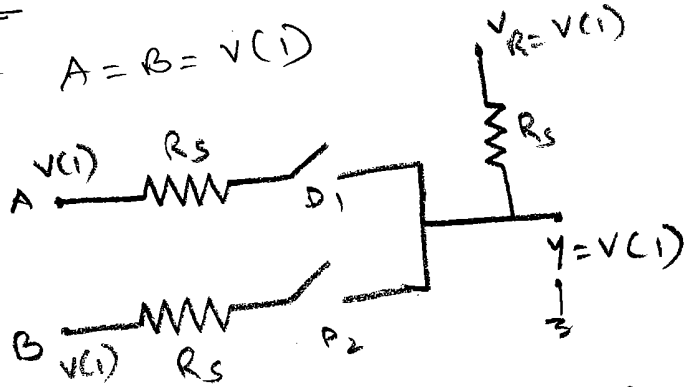
A, B = logic inputs

R = Pull up Resistor

Resistor R is called Pull-up resistor because in some sense it pulls the output from logic low to logic high.

Condition 1:

Let $A = B = V(1)$



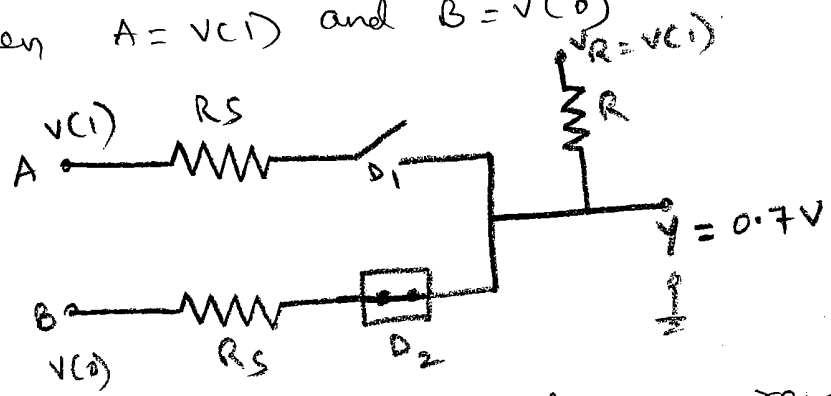
Both diodes are Reverse biased and represents open circuit. Since there is no path for current flow through resistor, it will not have any drop across

it and $V_R = V(1)$ appears at the output.

∴ when A = B = V(1), output Y = V(1).

Condition 2:

when A = V(1) and B = V(0)



Diode D_2 conducts and diode D_1 remains off. since current flows through R, diode D_2 towards V(0) (ground) and we get drop across diode D_2 at output

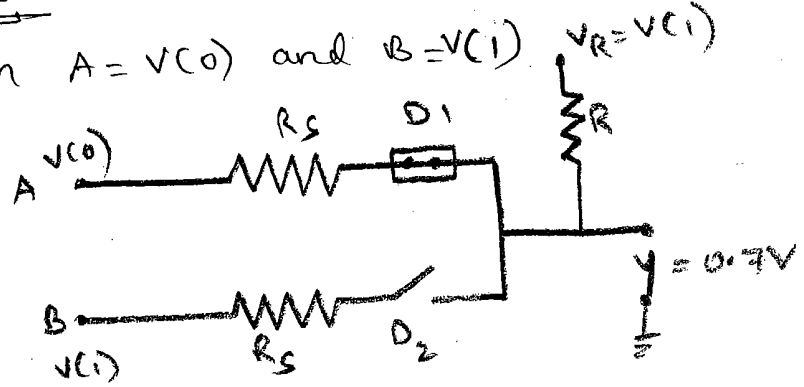
∴ when A = V(1) and B = V(0)

ideally Y = 0

practically Y = 0.7V

Condition 3:

when A = V(0) and B = V(1)



D_1 conducts and D_2 goes off and output again becomes the drop across diode

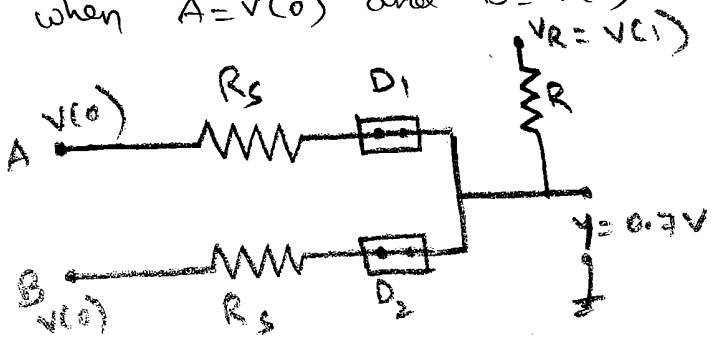
∴ when A = V(0), B = V(1)

ideally, Y = 0

practically, Y = 0.7 V

Condition 4:

when A = V(0) and B = V(0)



Both diodes D_1 and D_2 conducts having a drop of 0.7V. Again this drop appears at output.

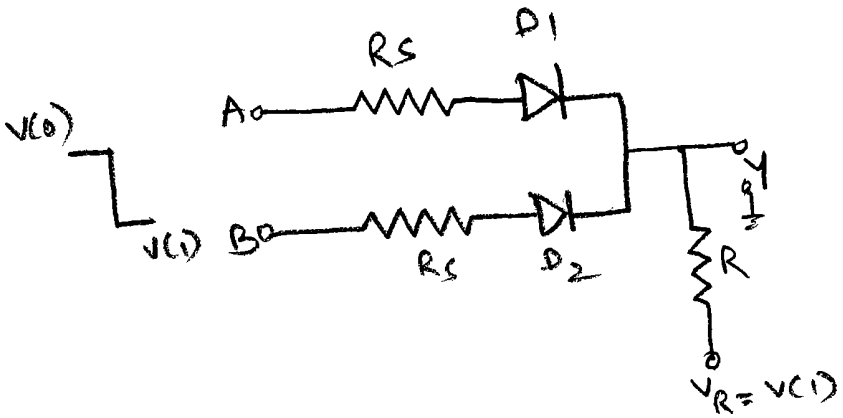
∴ when A = V(0) and B = V(0)

ideally Y = 0

practically Y = 0.7 V

Inputs		output	
A	B	Y	logic state
V(0)	V(0)	0.7V	LOW
V(0)	V(1)	0.7V	LOW
V(1)	V(0)	0.7V	LOW
V(1)	V(1)	V(1)	High

b) Diode AND gate for negative logic :



In this V(0) = ~~high, low high~~ 0

V(1) = ~~low high low~~ +5V

So, if any input is at 0 level V(0), the diode connected to this input conducts and the output is clamped at the voltage V(0)

i) If A = V(0), B = V(0)

$Y = V(0) = 0$

ii) If A = V(0), B = V(1)

$Y = V(0) = 0$

iii) If A = V(1), B = V(0)

$Y = V(0) = 0$

If all inputs are at 1 level V(1) then all diodes are reverse-biased and $V_0 = V(1)$

If A = V(1) and B = V(1)

$Y = V(1) = 1$

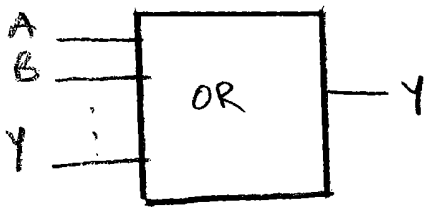
∴ The AND operation has been implemented.

2) Diode OR Gate :

→ It has two (or) more inputs and a single output.

→ "The output of an OR gate is 1 if one (or) more inputs are 1".

→ The IEEE standard symbol for OR circuit is shown in below fig (a) together with the Boolean expression.



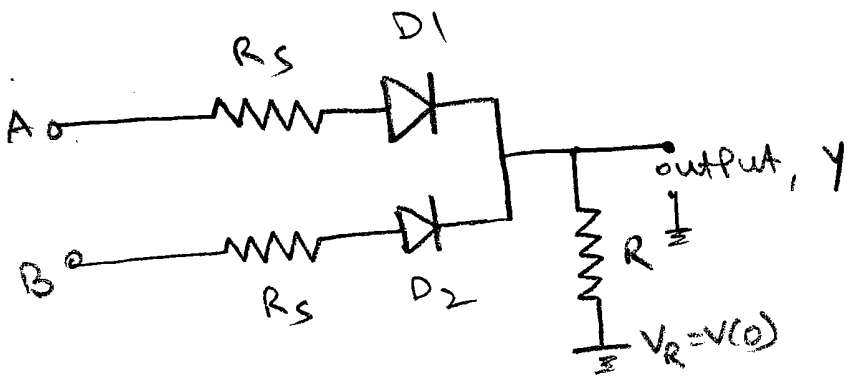
$Y = A + B + \cdots + N$

fig(a) : IEEE standard for OR gate

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

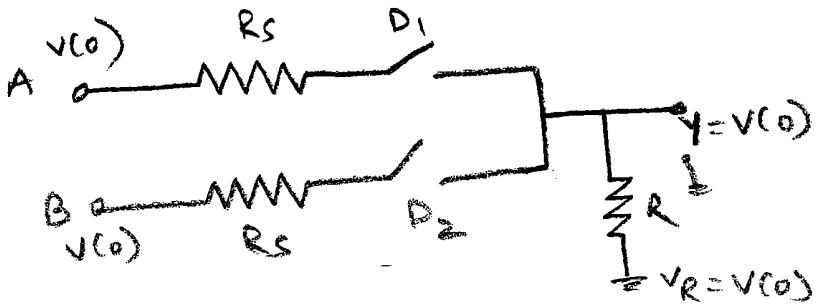
fig (b) : truth table

a) Diode OR gate for positive logic :



Condition 1:

when A = V(0), B = V(0)

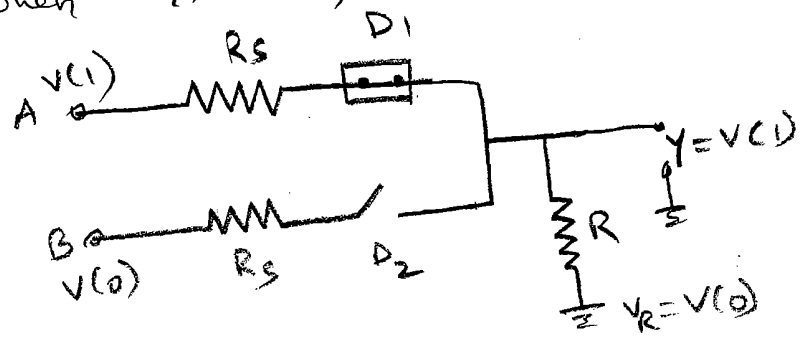


Both the diodes D_1 and D_2 are reverse biased so no current flows through R and output is

$$Y = V_R = V(0) = \text{Low}$$

Condition 2:

when A = V(1), B = V(0)



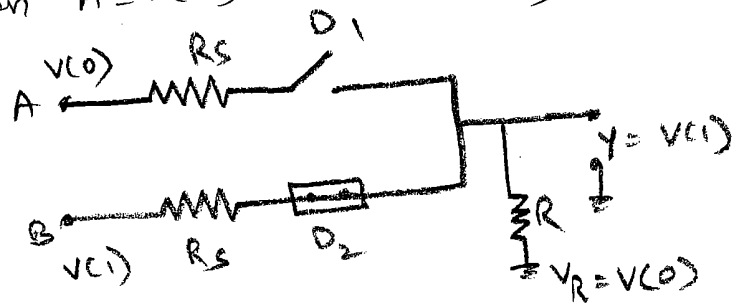
Diode D_1 conducts and D_2 remains off, thus a current flows through resistor R starting from input A through D_1, R to ground.

$V(1) - V_r - Y = 0$, neglecting drop across R_S

$Y = V(1) - V_r = V(1) - 0.7 = \text{high}.$

Condition 3:

when A = V(0) and B = V(1)

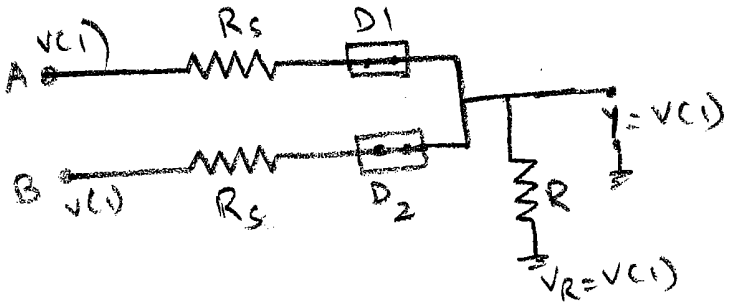


diode D_1 is reverse biased and diode D_2 is forward biased

$\therefore Y = V(1) - V_r = \text{high}$

Condition 4:

when A = V(1), B = V(1)



Both diodes D_1 & D_2 are forward biased

$\therefore Y = V(1) - V_r = \text{high}$

Let V(1) = 5V

$\therefore Y = V(1) - V_r$

$= 5 - 0.7$

$Y = 4.3V$

Inputs		Outputs	
A	B	Y	logic state
V(0)	V(0)	V(0)	Low
V(0)	V(1)	4.3V	High
V(1)	V(0)	4.3V	High
V(1)	V(1)	4.3V	High

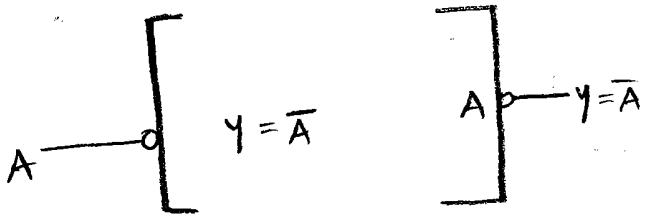
3) NOT gate:

→ It is also called as Inverter circuit.

→ It has single input and single output

→ "The output of a NOT circuit is 1 if and if the input is 0 and vice versa".

→ The IEEE standard with negation at the input of a logic block is shown in fig (a) and negation at the output of a logic block is shown in fig (b) along with the truth table in fig(c).



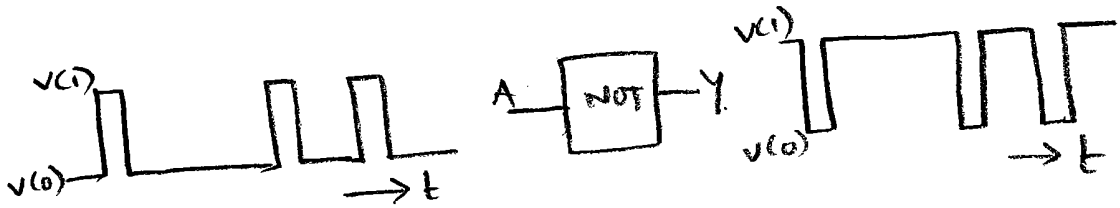
fig(a): Negation at input b) Negation at output

Input	output
A	Y
0	1
1	0

c) ~~Boot~~ Truth table

Equation is $Y = \overline{A}$ or A'

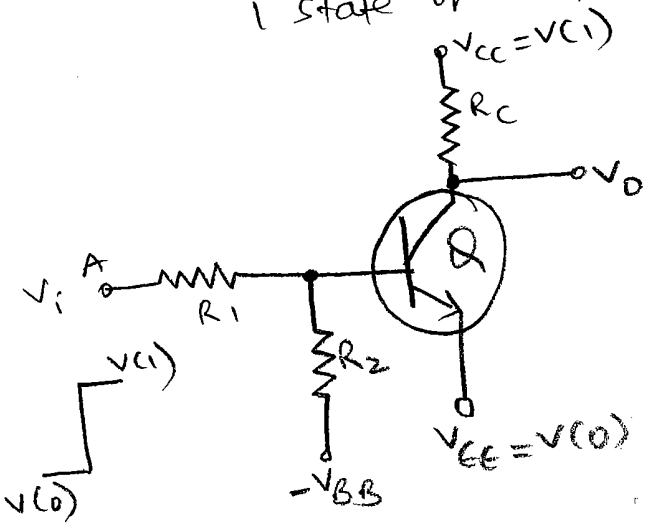
→ Since it inverts the sense of the output with respect to the input, it is also called as inverter.



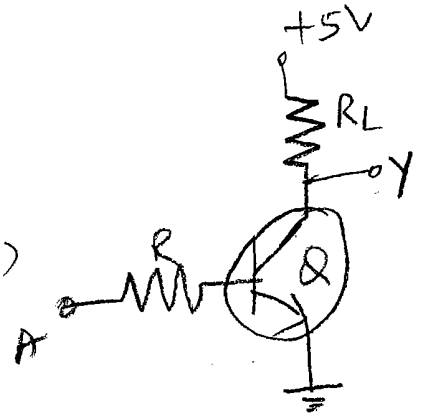
→ The transistor circuit below shows an inverter for positive logic:

0 state of $V(0) = V_{EE}$

1 state of $V(1) = V_{CC}$



(or)



fig(a): An inverter for positive logic

A similar circuit using p-n-p transistor is used for a negative-logic NOT circuit.

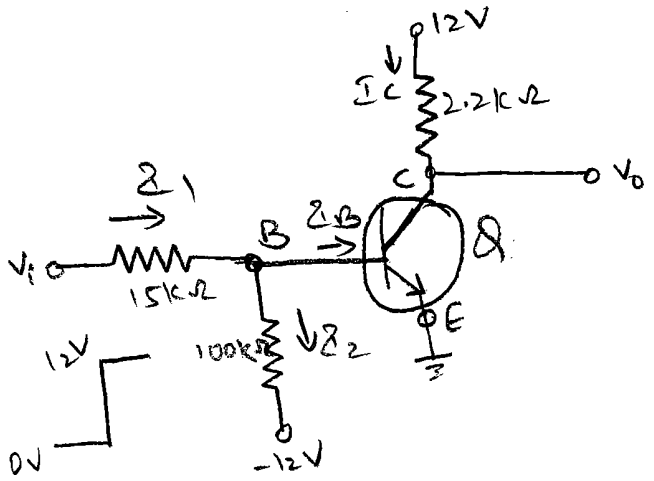
i) If the input is low, $V_i = V(0)$, then the parameters are chosen so that Q is off

$\therefore V_0 = V_{CC} = V(1)$.

ii) If the input is high, $V_i = V(1)$, then the circuit parameters are chosen so that Q is in saturation

$\therefore V_0 = V_{EE} = V(0)$

(7.4) If the silicon transistor in below fig has a minimum value of h_{FE} of 30, find the output levels for input levels of 0 and 12V ?



Sol: Given data

$h_{FE} = 30$

$V_{CC} = 12V$

$V_{EE} = -12V$

$R_1 = 15K\Omega$

$R_2 = 100K\Omega$

$R_C = 2.2K\Omega$

i) If $V_i = V(0) = 0V$

The open-circuited base voltage V_B is

$$V_B = -V_{EE} \times \frac{R_1}{R_1 + R_2}$$

$$V_B = -12 \times \frac{15}{100+15}$$

$$V_B = -1.56V$$

Since V_B is negative, Q is cut-off

$\therefore V_o = 12V$ for $V_i = 0$

ii) If $V_i = V(1) = 12V$

let us verify the assumption the Q is in saturation.

Assume transistor saturation parameters are zero.

$$I_{B(min)} = \frac{I_C}{h_{fe}}$$

$$I_C = \frac{V_{CC}}{R_C} = \frac{12}{2.2k} = 5.45\,mA$$

$$I_{B(min)} = \frac{5.45m}{30} = 0.18mA$$

from fig, $I_1 = \frac{V_i}{R_1} = \frac{12}{15} = 0.80\,mA = \frac{V_i - V_B}{R_1} = \frac{V_i}{R_1}$, $V_B = 0$

$$I_2 = \frac{V_i}{R_2} = \frac{12}{100} = 0.12\,mA = \frac{V_B - (-V_{EE})}{R_2} = \frac{0-(-12)}{R_2}$$

$$I_B = I_1 - I_2 = 0.80 - 0.12 = 0.68mA$$

$I_B > I_{B(min)}$, $\therefore$ Q is in saturation and drop across transistor is zero

$\therefore V_0 = 0$ for $V_i = 12V$

and the circuit has performed NOT operation.

(or)

let us assume transistor junction voltages

for silicon transistor, $V_{BE(sat)} = 0.7V$, $V_{CE(sat)} = 0.3V$

$$I_C = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{12-0.3}{2.2} = 5.31\,mA$$

$$I_{B(min)} = \frac{I_C}{h_{fe}} = \frac{5.31}{30} = 0.18mA$$

$$I_1 = \frac{V_{in} - V_{BE(act)}}{R_1} = \frac{12 - 0.7}{15K} = 0.75mA$$

$$I_2 = \frac{V_{BE(act)} - (-V_{EE})}{R_2} = \frac{0.7 - (-12)}{100} = 0.13mA$$

$$I_B = I_1 - I_2 = 0.75 - 0.13 = 0.62mA$$

since $I_B > I_{B(min)}$ so, Q is in saturation

so, if $V_i = V(0)$, $V_o = 12V$

$V_i = V(1)$, $V_o = 0.3V$

Classification of Logic families:

1) Bipolar Logic families
   a) Direct-coupled transistor logic (DCTL)
   b) Resistor-Transistor logic (RTL)
   c) Resistance capacitance transistor logic (RCTL)
   d) Diode transistor logic (DTL)
   e) Transistor-Transistor logic (TTL)
   f) Current-Mode logic (CML) or ECTL

2) MOS logic families
   a) NMOS
   b) PMOS
   c) CMOS

→ "Logic family is defined as a group of compatible IC's with the same logic levels and supply voltages which perform various logic functions and are fabricated as per a specific circuit configuration."

1) Resistor- Transistor logic (RTL):

→ The Basic RTL gate is NOR gate

→ RTL circuit consist of resistors & Transistors

fig (a) below shows 2-input RTL NOR gate.

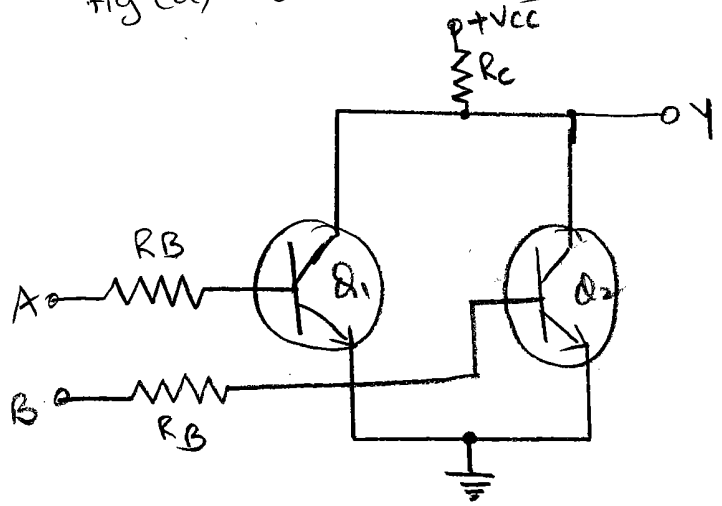


fig (a): 2-input RTL NOR gate

Emitters of both the transistors are connected to a common ground and Collectors of both transistors are tied ~~together~~ through a common Collector resistor Rc to a supply voltage Vcc.

The resistor Rc is known as passive pull-up resistor.

Operation:

→ Inputs representing logic levels are applied at A and B terminals.

→ In RTL gate, the input voltage corresponding to Low level is required to be low enough

for the corresponding transistor to be cut-off.

→ similarly, the input voltage corresponding to HIGH level should be high enough to drive the corresponding transistor to saturation.

Condition 1:

when both the inputs are high.

i.e; $A = V(1)$, $B = V(1)$

Both transistors Q_1 and Q_2 goes to ON state (saturation) and the voltage at collector is $V_{CE sat}$.

$\therefore Y = V_{CE(sat)} = 0.2V = LOW$

Condition 2:

when both the inputs are low

ie; $A = V(0)$, $B = V(0)$

Both transistors Q_1 and Q_2 goes to off state (cut-off). Thus no current flow through R_C and drop across R_C is zero. So, complete V_{CC} will appear at output

$\therefore Y = V_{CC} = High$

Condition 3 :

when only one input goes high

i.e, when $A = V(1)$ and $B = V(0)$ (or)

$A = V(0)$ and $B = V(1)$

The transistor feeded with high input conducts causing a current to flow through ON transistor and the transistor enters into saturation. Thus the output voltage becomes $V_{CE(sat)}$

∴ In both the conditions

$$Y = V_{CE(sat)} = \text{LOW}$$

Inputs		outputs	
A	B	Y	logic state
V(0)	V(0)	Vcc	High
V(0)	V(1)	$V_{CE(sat)}$	LOW
V(1)	V(0)	$V_{CE(sat)}$	LOW
V(1)	V(1)	$V_{CE(sat)}$	LOW

The truth table reveal that RTL circuit functions as NOR gate.

Advantages:

1) low cost
2) improved speed when compared to DTL

Disadvantages:

1) less immunity to noise.
2) poor fan-out capability.
3) overall speed is low.
4) high power dissipation.

which can be avoided in DTL

2) Direct coupled transistor logic (DCTL):

→ Below fig consist of three CE transistors Q_1, Q_2 and Q_3 with collectors tied together.

→ fan-in is 3 and fan out is 2 since the output feeds the two transistors Q_4 and Q_5. The input to Q_1 comes directly from the output Y' of a previous NOR gate.

→ Since no resistors, capacitors or diodes are used between stages, such a system is called direct-coupled transistor logic (DCTL).

→ It also acts as NOR gate.

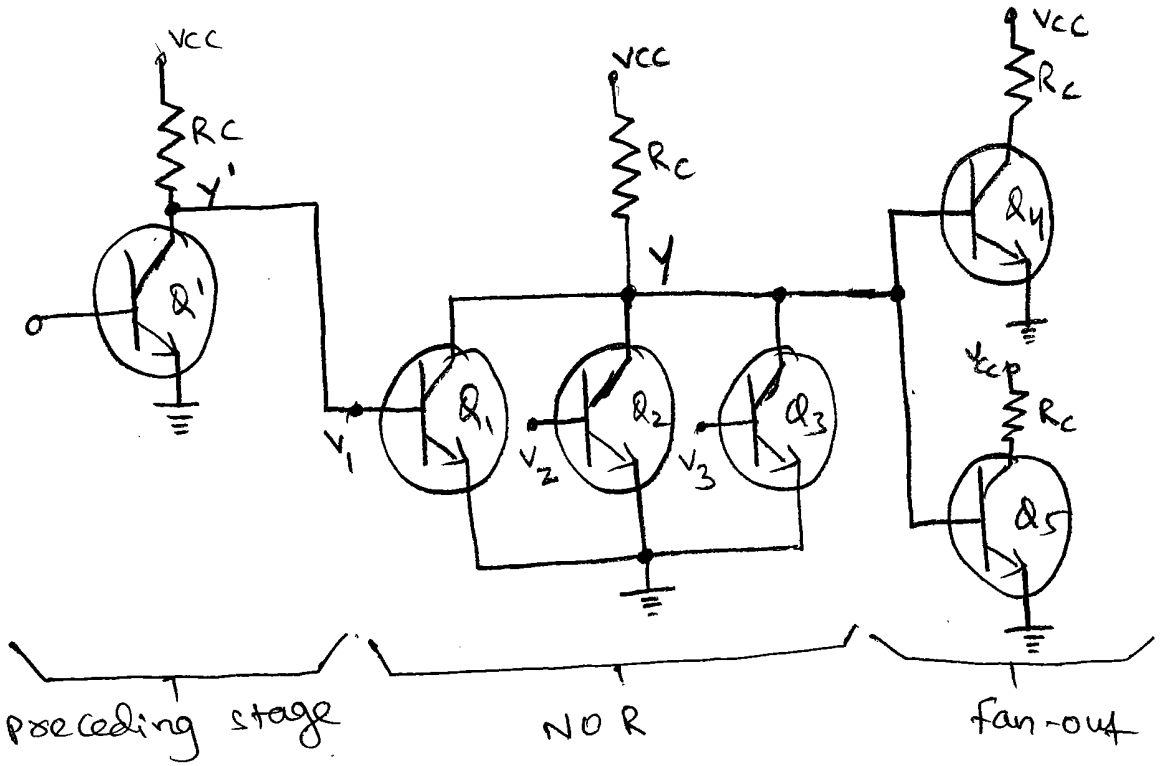


fig: DCTL as NOR gate

Operation:

Condition 1:

All inputs are Low

i.e; $V_1 = V_2 = V_3 = 0$

The low voltage ($V_1 = 0$) to an input to Q_1 comes from saturated ~~sato~~ transistor (Q') of a preceding stage

so, $V_1 = V_{CE(sat)} = V(0)$

since the current in Q_1 is almost zero, the output Y tries to rise V_{CC} and Q_4 & Q_5 go into saturation. Hence the output Y is clamped at

$V_{BE(sat)} = V(1) \simeq 0.7V$. for silicon.

Thus with all inputs in the low state, the output is in high state.

Condition 2:

Atleast one input V_1 is in high state.

i.e; V_1 = high, $V_2 = V_3 = 0$

Since Q_1 is fed from Q', Q' is cut-off and Q_1 is driven into saturation.

Under these circumstances the output Y is

$$Y = V_{CE(sat)} = V(0).$$

Condition 3:

If more than one input is high, then the output will certainly be low.

Hence, the NOR function is satisfied.

Inputs			output	logic state
V_1	V_2	V_3	Y	
0	0	0	Vcc	High
0	0	1	$V_{CE(sat)}$	Low
0	1	0	$V_{CE(sat)}$	Low
0	1	1	$V_{CE(sat)}$	Low
1	0	0	$V_{CE(sat)}$	Low
1	0	1	$V_{CE(sat)}$	Low
1	1	0	$V_{CE(sat)}$	Low
1	1	1	$V_{CE(sat)}$	Low

Advantages:

1) Need for only one low voltage supply (operation with 1.5V is possible).
2) Transistors with low breakdown voltages may be used.
3) The power dissipation is low
4) This configuration is used for integrated-circuit manufacture because transistors are cheaper to fabricate with integrated techniques than are resistors or capacitors.

Disadvantages:

1) The reverse saturation current for all fan-in transistors adds in the common collector-circuit resistor R_C.

So at high temperature, total I_{CB} drop may be large enough so that the output Y is too low to drive the fan-out transistors into saturation.

2) ~~Because of direct connection, the base current is almost equal to the collector current~~

2) It suffers from a problem called current hogging. i.e; The bases of the fan-out transistors are connected together. Since the input characteristics can never be identical.

let us assume Q_4 has a much lower V_{BE} for a given I_B than does Q_5.

Under these circumstances, Q_4 will "hog" most of the base current, and it is possible that Q_5 may not even be driven into saturation.

3) Diode transistor logic (DTL):

→ The basic DTL gate act as NAND gate.

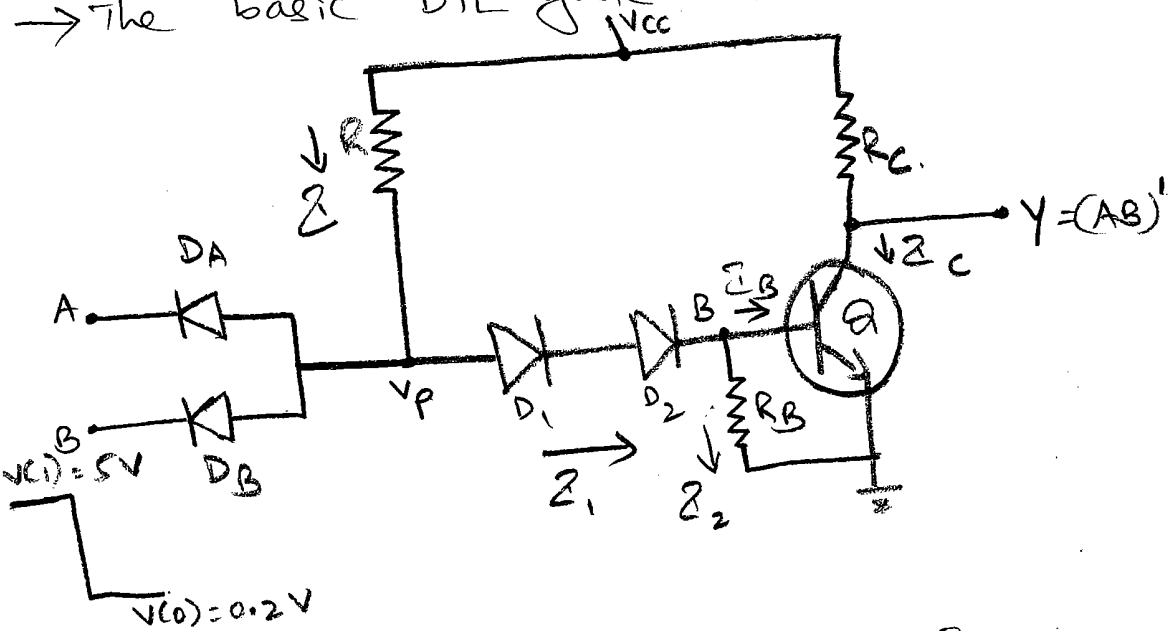


fig: Two input NAND gate as DTL IC

→ The two inputs of the gate are applied through the diodes D_A and D_B which are transmitted to the base of Q through diodes D_1 and D_2. Output of the gate is measured at the collector of Q_D.

→ In this circuit, the input diodes along with resistor R forms a diode AND gate whose

output is available at point P. The transistor acts as inverter, Thus the output of diode AND gate is inverted to give output of DTL gate as NAND gate.

→ The transistor Q at the output can assume either Low (or) HIGH voltage levels depending whether it operates in saturation (or) in Cut-off.

→ $V_{BE(sat)} = 0.9V$ for Silicon transistor to be in saturation and base current $I_B > \frac{I_{C(sat)}}{h_{FE}}$

→ From the figure, it is evident that voltage at point P, V_P is responsible to drive the transistor Q in Cut-off (or) in saturation.

→ Let us calculate the voltage V_P at point P, required to drive transistor Q into saturation is

$$V_{P(ON)} = (V_\gamma)_{D_1} + (V_\gamma)_{D_2} + (V_{BE(sat)})_Q$$

$$V_{P(ON)} = 0.7 + 0.7 + 0.9.$$

$$V_{P(ON)} = \underline{2.3V}$$

Operation :

Condition 1 :

When all the inputs are high

ie; $A = B = V(1) = 5V$

So, when all inputs are high, Diodes D_A & D_B will be in off state.

So, Current(I) flows through diodes D_1 & D_2 through base of Q.

we know voltage at point P = 2.3V and voltage drop across any of the reverse-biased input diodes (D_A or D_B) is $5 - 2.3 = 2.7V$

So, 2.7V is sufficient to keep the input diodes in reverse-biased.

let us calculate the Current I_B of Q

$$I_B = I_1 - I_2$$

$$I_1 = I = \frac{V_{CC} - V_P}{5K} = \frac{5 - 2.7}{5K} = 0.46mA$$

$$I_2 = \frac{V_{BE(sat)} - 0}{5K} = \frac{0.9}{5K} = 0.18mA$$

$$\therefore I_B = I_1 - I_2 = 0.46 - 0.18 = 0.28mA$$

$$I_C = \frac{V_{CC} - V_{CE(sat)}}{2.2K} = \frac{5 - 0.2}{2.2K} = 2.18mA$$

So, transistor Q to remain in saturation

$$I_B > \frac{I_{C(sat)}}{h_{FE}}$$

$$h_{FE(min)} = \frac{I_C}{I_B} = \frac{2.18}{0.28} \simeq 8$$

∴ If the transistor has h_{FE} larger than 8 the NAND circuit functions as expected when all the inputs are High.

$$\therefore Y = V_{CE(sat)} = \text{LOW}$$

Condition 2:

If atleast one input is Low, the output is expected to be High.

let $A = V(0)$, $B = V(1)$

the diode D_A is conducting and D_B is Cut-off.

So, voltage at point P is

$$V_P = V(0) + V_D = 0.2 + 0.7 = 0.9V$$

It is clear that when $V_P = 0.9V$, the output transistor remains in Cut-off and output will be high.

Since to make transistor into saturation, we need $V_P = 2.3V$.

$$\therefore Y = V_{CC} = \text{high}.$$

Inputs		outputs	
A	B	Y	logic state
V(0)	V(0)	Vcc	high
V(0)	V(1)	Vcc	high
V(1)	V(0)	Vcc	high
V(1)	V(1)	VCE(sat)	LOW

Advantages:

1) Improved noise margin.
2) larger fan-out

Disadvantage:

1) speed is slow
   which can be avoided in TTL

4) Transistor - Transistor logic (TTL):

→ TTL works as NAND gate.
→ TTL is named for its dependence on transistors alone to perform basic logic operations.
→ The circuit diagram of 2-input TTL NAND gate is shown below:

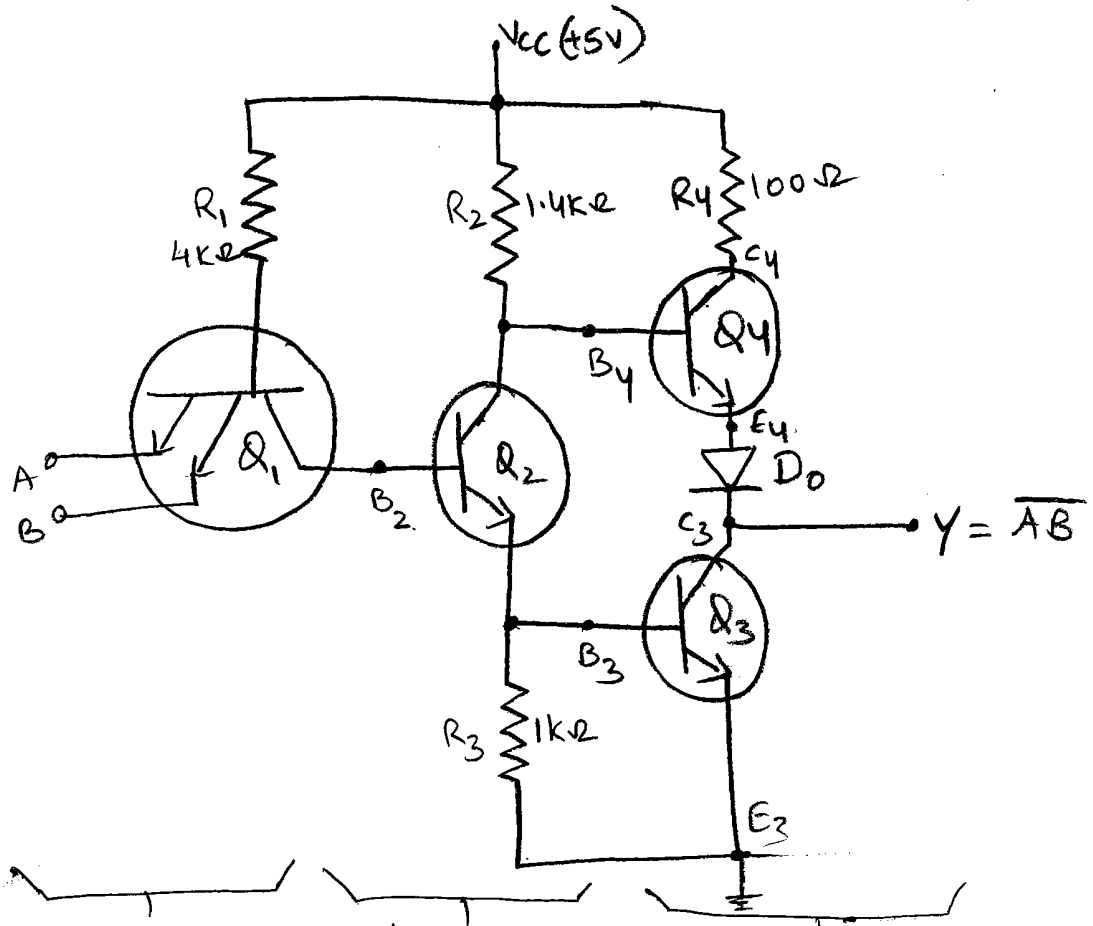


fig: 2-input TTL NAND gate

The transisto Q_1 is an NPN transistor having two emitters, one for each input to the gate. Although this circuit looks complex, we can simplify its analysis by using diode equivalent of multiple-emitter transistor Q_1 as shown below:

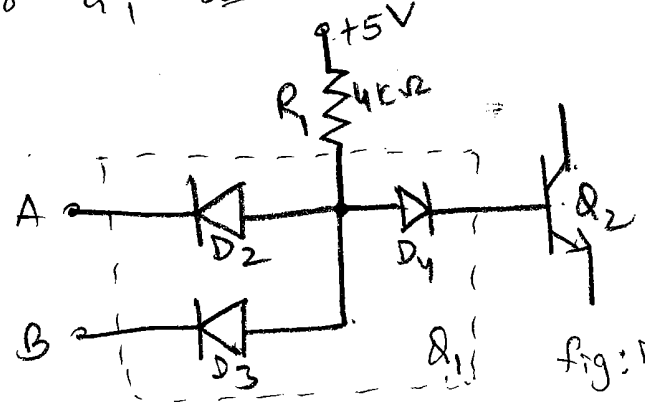


fig: Diode equivalent for Q_1

→ Diodes D_2 & D_3 represent two Emitter-base (E-B) junctions of Q_1 and D_4 is the Collector-base (C-B) junction.

Operation:

Condition 1:

When All inputs are high

i.e; A = B = high

diodes D_2 & D_3 are reverse-biased, Diode D_4 is in forward-biased. The supply voltage V_{CC} forces a current through resistor R_1 and diode D_4 to the base of transistor Q_2. This base drive is sufficient to turn ON Q_2

The Collector current of Q_2 causes voltage drop across R_2 with the result that the potential at the collector terminal of Q_2 is $V_{CE(sat)}$, which is not sufficient to make Q_4 ON

$\therefore Q_4$ = off.

The emitter current of Q_2 supplies necessary base-drive for transistor Q_3 & hence Q_3 = ON

$\therefore$ output Y = $V_{CE(sat)}$ = Low

Condition 2:

When any one input is Low

let A = high, B = low

so diode D_2 is off and D_3 is ON. The supply voltage V_{cc} forces a current through resistor R_1 and diode D_3 to the ground.

The potential at B_2 is 0.7V (cut-in voltage of D_3). This is not sufficient to turn on transistor Q_2, since it must overcome both the potential barrier of D_4 and cut-in voltage of Q_2.

$\therefore Q_2 = $ off

since Q_2 is off, there is no base drive for transistor Q_3

$\therefore Q_3 = $ off

since there is no collector current of Q_2, point B_4 is quite a high potential which is sufficient to overcome the cut-in voltage of Q_4 and barrier potential of D_0.

$\therefore Q_4 = $ ON

$\therefore$ output $Y =$ high

Inputs		output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

5) Emitter-coupled logic (ECL):

→ It is also called as current mode logic (CML).

→ Need:

The TTL family uses transistors operating in the saturation mode. As a result their switching speed is limited by the storage delay time associated with a transistor that is driven into saturation.

Another logic family has been developed that prevents transistor saturation, thereby increasing overall switching speed by using a radically different circuits structure called current mode logic (CML) or Emitter coupled logic (ECL).

Unlike TTL & CMOS families, ECL does not produce a large voltage swing between Low & High levels.

It has small voltage swing less than a volt and it internally switches current between two possible paths depending on the output state.

Advantages:

1) It is the fastest among all logic families.
2) Transistors are not allowed to go into complete saturation and thus eliminating storage delays.
3) switching transients are less because power supply current is more stable than in TTL and CMOS circuits.

Disadvantages:

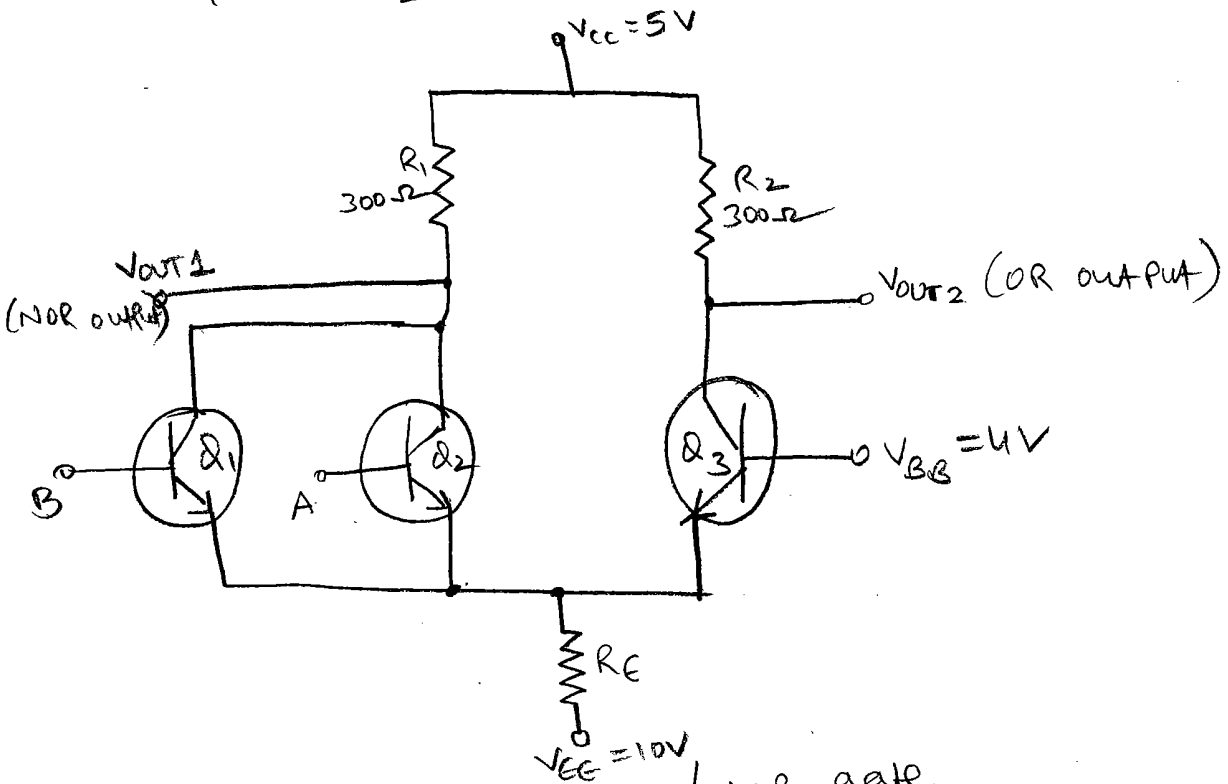
1) As logic levels are kept close to each other noise margin is reduced and it is difficult to achieve good noise immunity.
2) Power consumption is more because transistors are not completely saturated.

→ ECL OR/NOR Gate:

Below fig(a) shows 2-input ECL OR/NOR gate. This has an additional transistor in parallel with Q_1.

i) If any input is High corresponding transistor is active, and V_{OUT_1} is Low (NOR output). At the same time Q_3 is OFF producing V_{OUT_2} High (OR output).

We can connect one more transistor parallel with Q_1 and Q_2 to get 3-input ECL OR/NOR gate.



fig(a): 2-input ECL OR/NOR gate

fig (b) shows the function table, fig (c) shows logic symbol, fig (d) shows truth table of 2-input ECL OR/NOR gate.

A	B	Q_1	Q_2	Q_3	V_{OUT1} NOR	V_{OUT2} OR
0	0	OFF	OFF	ON	1	0
0	1	ON	OFF	OFF	0	1
1	0	OFF	ON	OFF	0	1
1	1	ON	ON	OFF	0	1

fig(b): function table

A	B	V_{out1} (NOR)	V_{out2} (OR)
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

fig (c): Truth table

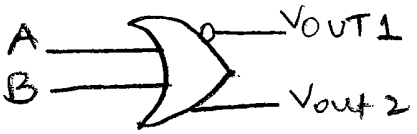
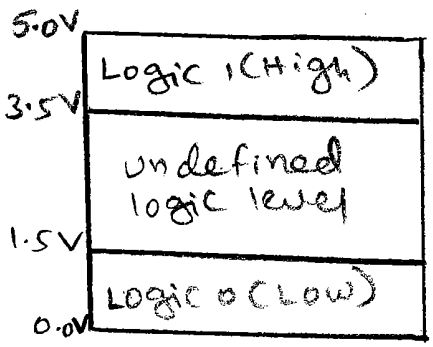


fig (b): logic Symbol

6) CMOS logic families:

→ The basic building blocks in CMOS logic circuits are MOS transistors.

→ CMOS logic levels:



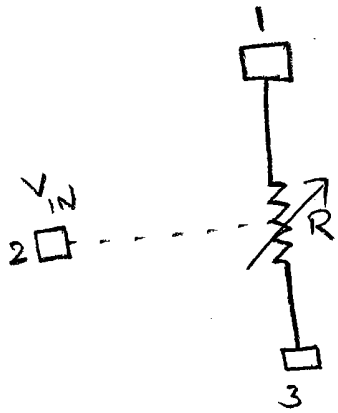
In general, CMOS circuit may interpret any voltage in the range 0 to 1.5V as a logic 0 and in the range 3.5 to 5.0V as a logic 1

The voltages in between 1.5V to 3.5V are not expected to occur except during signal transitions and if they occur, the circuit may interpret them as either 0 to 1.

→ MOS Transistor:

A MOS transistor is a three terminal device that acts like a voltage controlled resistance.

An input voltage applied to one terminal controls the resistance between the remaining terminals.

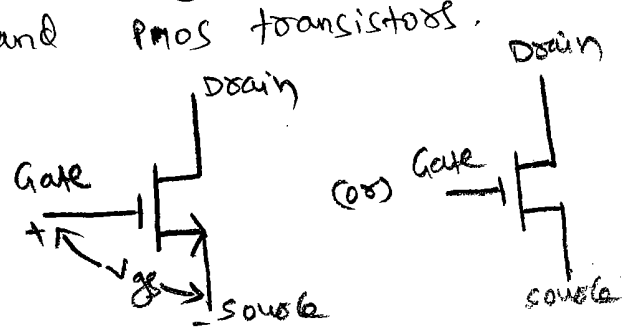


In CMOS logic circuits, MOS transistor is operated so that its resistance is always either very high (or) very low.

Types of MOS transistors:

1) n-channel (NMOS) and
2) P-channel (PMOS)

Below fig shows the circuit symbols of NMOS and PMOS transistors.



a) NMOS transistor

b) PMOS transistor

MOS transistor has three terminals called gate, source and drain.

NMOS transistor:

In this, the voltage from gate to source is normally zero or positive.

If $V_{gs} = 0$, then the resistance from drain to source, R_{ds} is very high. It is of the order of megaohms.

If V_{gs} = positive, then R_{ds} is very low. It is between 0 – 10 ohms.

PMOS transistor:

In this V_{gs} is normally zero or negative.

If $V_{gs} = 0$, then R_{ds} is very high

If V_{gs} = negative, then R_{ds} is very low

→ These characteristics of NMOS and PMOS transistors make them use as a switch in digital IC technology

→ The gate of the MOS transistor is separated from drain and source by an insulating material with a very high resistance. The voltage applied at gate terminal creates an electric field that enhances or retards the

flow of current between source and drain. Due to this effect the MOS transistor is also known as MOSFET (Metal oxide Semiconductor field effect transistor).

→ The NMOS and PMOS transistors are used together in a complementary way to form CMOS (Complementary Metal oxide semiconductor) logic.

Basic CMOS Inverter circuit:

→ fig (a) below shows the basic CMOS inverter circuit.

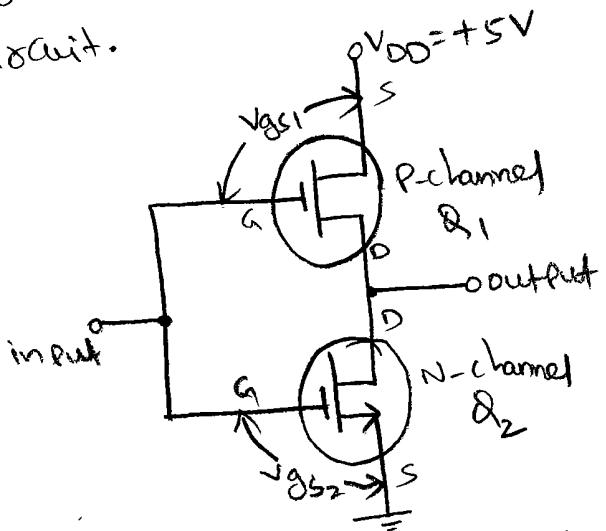


fig (a): CMOS Inverter circuit

→ It consists of two MOSFETs in series in such a way that the P-channel device has its source connected to $+V_{DD}$ (a positive voltage) and N-channel device has its source connected to ground.

→ The gates of the two devices are connected together as the common input and drains are connected together as the common output.

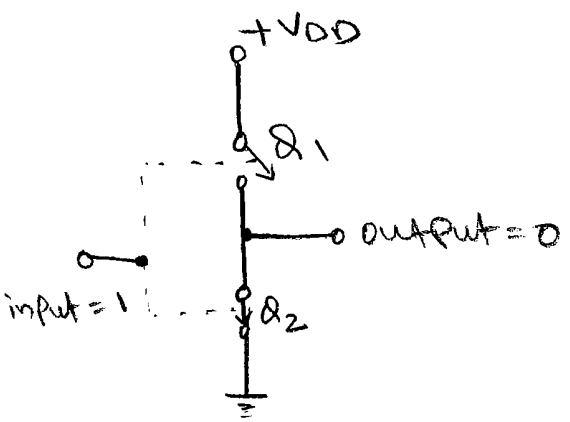
i) when input is HIGH

The gate of Q_1 (P-channel) is at 0V relative to source of Q_1 i.e; $V_{gs_1} = 0V$, Thus Q_1 is OFF.

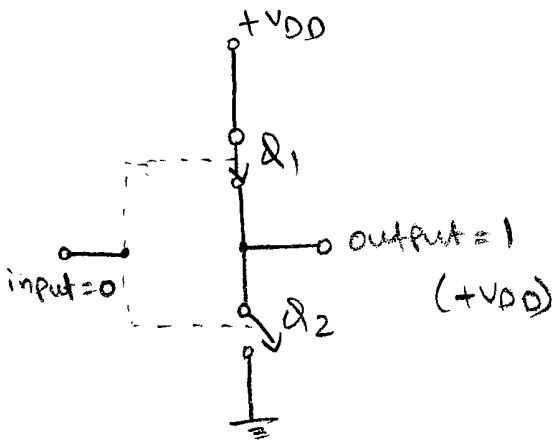
On the other hand, the gate of Q_2 (N-channel) is at $+V_{DD}$ relative to its source i.e; $V_{gs_2} = +V_{DD}$.

Thus Q_2 is ON.

This will produce $V_{OUT} \simeq 0V$ as shown in fig(b).



fig(b): Input = 1



fig(c): Input = 0

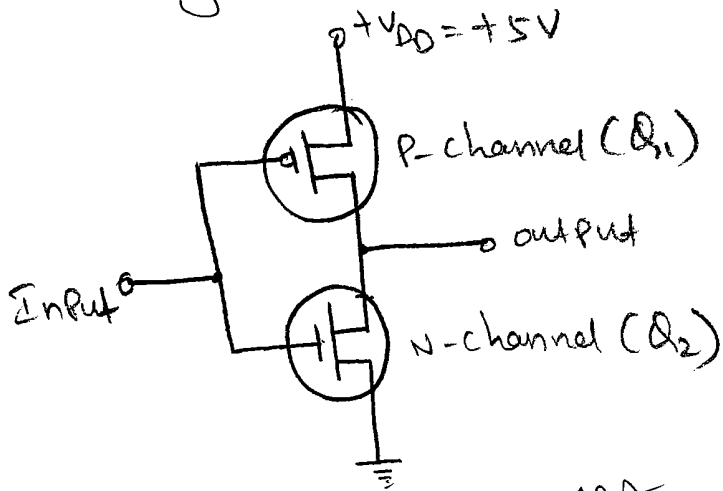
ii) when input is low

The gate of Q_1 (P-channel) is at negative potential relative to its source while Q_2 has $V_{gs} = 0V$. Thus Q_1 is ON and Q_2 is OFF. This produces output voltage approximately $+V_{DD}$ as shown in fig(c).

A	Q_1	Q_2	output
0	ON	OFF	1
1	OFF	ON	0

Truth table

→ fig(d) shows different symbols used for p-channel and n-channel transistors to reflect their logical behaviour.



fig(d): CMOS inverter

The n-channel transistor (Q_2) is switched 'ON' when a HIGH voltage is applied at the input.

The p-channel transistor (Q_1) has the opposite behaviour, it is switched ON when a LOW voltage is applied at the input. It is indicated by placing bubble in the symbol.

CMOS NAND Gate :

→ fig(a) shows CMOS 2-input NAND gate. It consists of two P-channel MOSFETS, Q_1 & Q_2 connected in parallel and two N-channel MOSFETS, Q_3 & Q_4 connected in series.

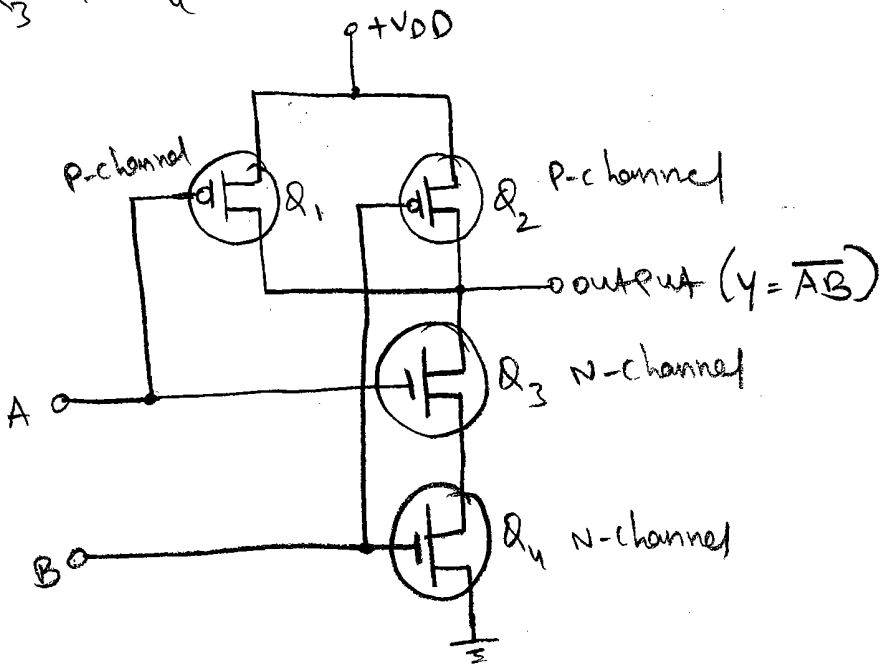
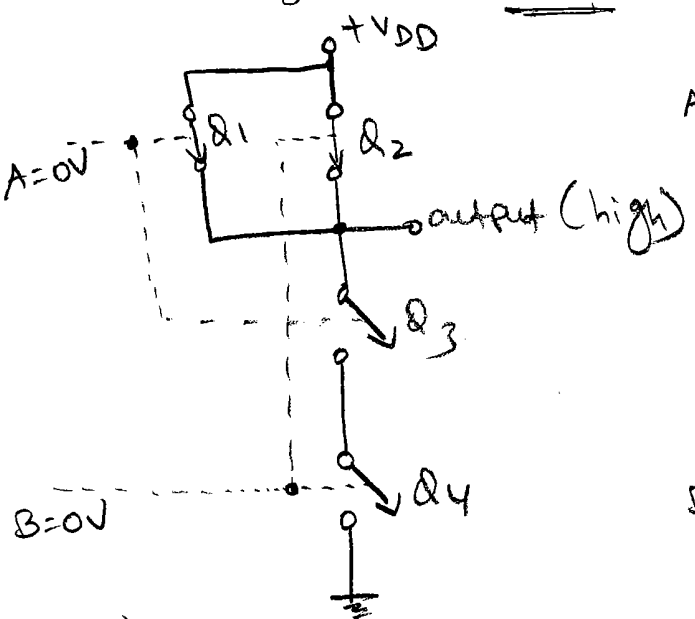
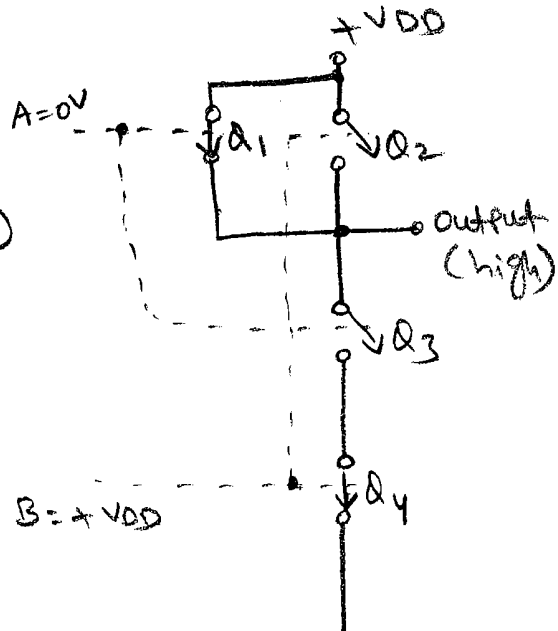


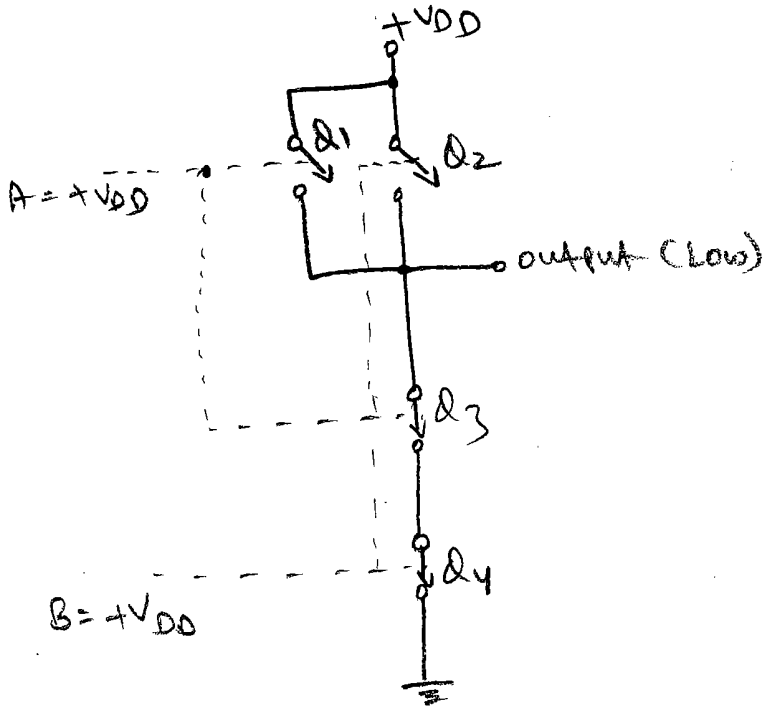
fig (a) : schematic

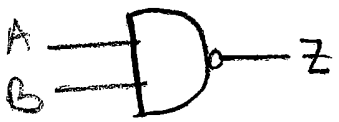


fig(b): A = B = 0V
$V_{GS1} = V_{GS2} = -V_{DD}$
$V_{GS3} = V_{GS4} = 0V$



fig(c): A = 0V, B = +VDD
$V_{GS1} = -V_{DD}$, $V_{GS4} = +V_{DD}$
$V_{GS2} = V_{GS3} = 0V$





Logic symbol.

fig (d): $A = B = V_{DD}$

$V_{GS1} = V_{GS2} = 0V$

$V_{GS3} = V_{GS4} = +V_{DD}$

→ fig (b) shows the equivalent switching circuit when both inputs are low. Here, the gates of both p-channel MOSFETs are negative with respect to their sources, since the sources are connected to $+V_{DD}$. Thus, Q_1 & Q_2 are both ON. Since the gate-to-source voltages of Q_3 & Q_4 (n-channel MOSFETs) are both 0V, those MOSFETs are OFF.

The output is therefore connected to $+V_{DD}$ (HIGH) through Q_1 and Q_2 and is disconnected from ground.

→ fig (c) shows the equivalent switching circuit when $A = 0$ and $B = +V_{DD}$. In this case, Q_1 is ON because $V_{GS_1} = -V_{DD}$ and Q_4 is ON because $V_{GS_4} = +V_{DD}$. MOSFETS Q_2 & Q_3 are off because their gate-to-source voltages are 0V. Since Q_1 is ON and Q_3 is off, the output is connected to $+V_{DD}$ and it is disconnected from Ground.

when $A = +V_{DD}$ and $B = 0V$, the situation is similar, the output is connected to $+V_{DD}$ through Q_2 and it is disconnected from ground because Q_4 is OFF.

→ fig (d) shows the equivalent switching circuit when both inputs are high ($A = B = +V_{DD}$), MOSFETS Q_1 & Q_2 are both OFF and Q_3 & Q_4 are both ON.

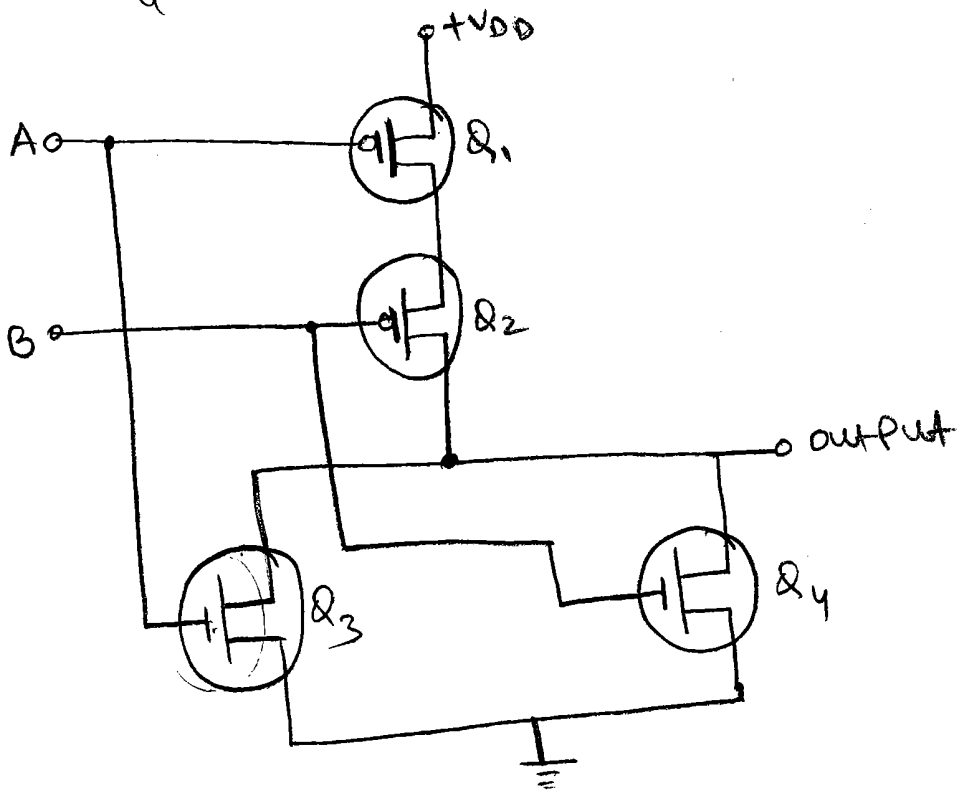
Thus, the output is connected to ground through Q_3 & Q_4 and it is disconnected from $+V_{DD}$.

A	B	Q_1	Q_2	Q_3	Q_4	output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

"P-channel MOSFET is ON when its gate voltage is negative with respect to its source whereas n-channel MOSFET is ON when its gate voltage is positive with respect to its source."

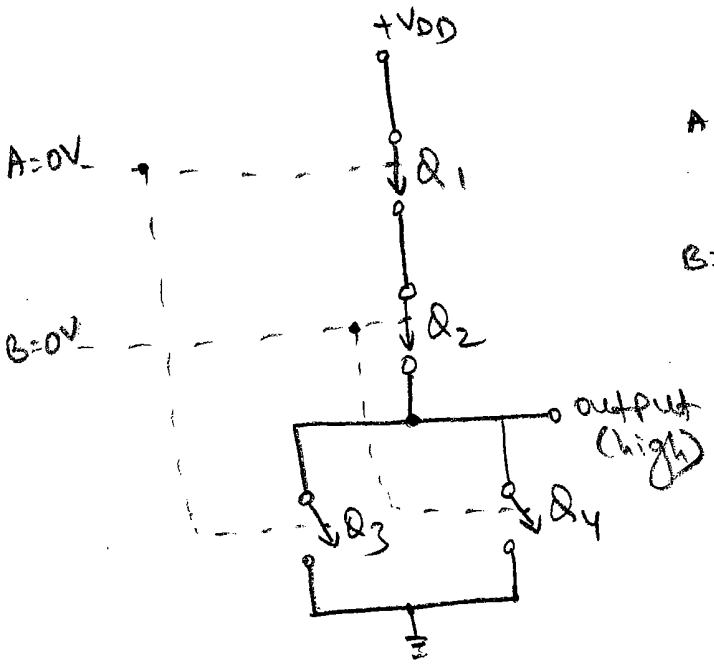
CMOS NOR gate:

→ fig(a) shows 2-input CMOS NOR gate. Here, p-channel MOSFETS Q_1 and Q_2 are connected in series and n-channel MOSFETS Q_3 and Q_4 are connected in parallel.



fig(a): schematic

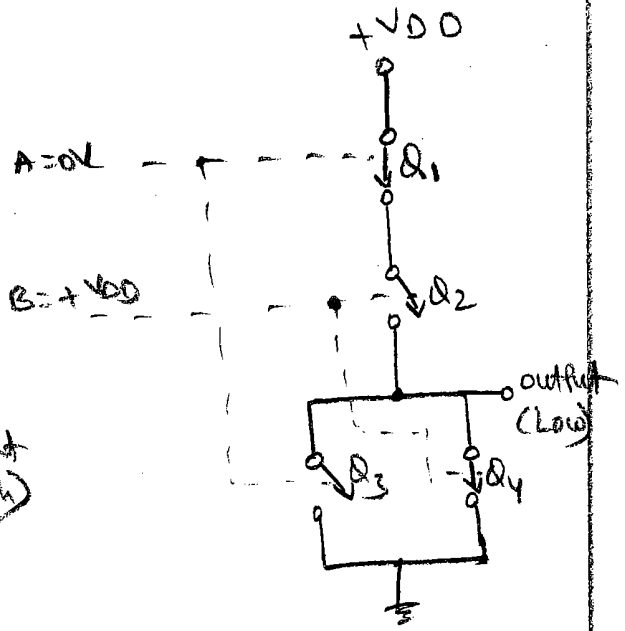
→ Like NAND circuit, this circuit can be analyzed by realizing that a Low at any input turns ON its corresponding p-channel MOSFET and turns off its corresponding n-channel MOSFET and vice versa for a HIGH input. This is shown in below fig:



fig(b): A = B = 0V

$V_{GS_1} = V_{GS_2} = -V_{DD}$

$V_{GS_3} = V_{GS_4} = 0V$



fig(c): A = 0V, B = $+V_{DD}$

$V_{GS_1} = -V_{DD}$

$V_{GS_2} = V_{GS_3} = 0V$

$V_{GS_4} = +V_{DD}$

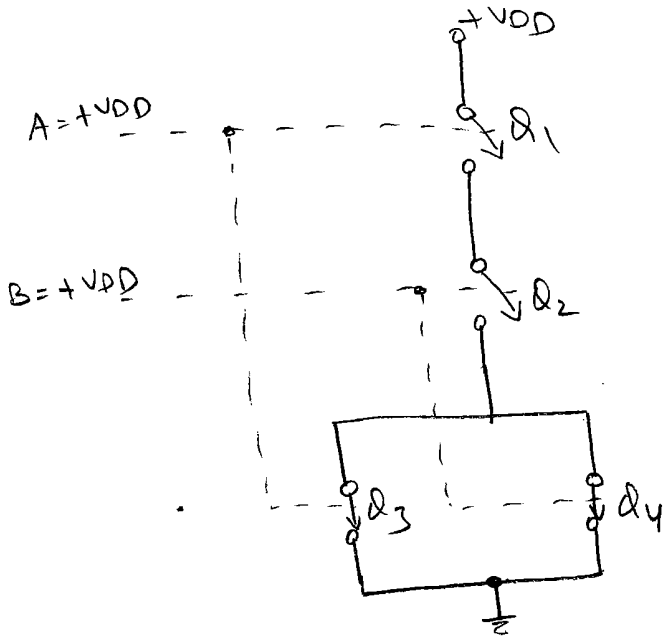


fig (d): $A = B = +V_{DD}$

$V_{GS_1} = V_{GS_2} = 0V$

$V_{GS_3} = V_{GS_4} = +V_{DD}$

A	B	Q_1	Q_2	Q_3	Q_4	output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

Truth table

NAND Vs NOR:

→ CMOS NAND and NOR gates do not have identical performance.

→ for a given silicon area, an N-channel transistor has lower 'ON' resistance than a P-channel

transistor. Therefore, K N-channel transistors connected in series have lower 'ON' resistance than the P-channel transistors connected in series.

→ As a result, K-input NAND gate which uses n-channel transistors in series is generally faster than and preferred over K-input NOR gate.

Unconnected CMOS Inputs:

→ CMOS inputs should never be left unconnected (or floating).

→ All CMOS inputs have to be tied either to a fixed voltage level (0V or V_{DD}) or to another input.

→ This rule applies even to the inputs of extra unused logic gates on a chip.

→ An unused CMOS input is susceptible to noise and static charges that could easily bias both P- and n-channel MOSFETs in the conductive state, resulting in increased power dissipation and possible overheating.

→ An unused AND or NAND input should be tied to logic 1 and an unused OR or NOR input should be tied to logic 0.

Advantages of CMOS family:

1) Consumes less Power.
2) Can be operated at high voltages, resulting in improved noise immunity.
3) fan-out is more.
4) Better noise margin.

Disadvantages of CMOS family:

1) Susceptible to static charge.
2) Switching speed is low.
3) Greater propagation delay.

Comparison of Logic families

Parameter	RTL	DCTL	DTL	TTL	ECL	CMOS
Components used	Resistors & Transistors	Resistors & Transistors	Resistor, Diode & Transistor	Resistor, diode & Transistor	Resistor & Transistor	N-channel & P-channel MOSFET
Circuit	Simple	Simplest	Moderate	Complex	Complex	Moderate
Noise Margin	Poor	Poor	High	Medium	Low	High
Fan-out	Low (4)	Low (4)	Medium (8)	More (10)	High (25)	50
Power dissipation in mW per gate	30	30	8-12	10	40-55	0.1
Basic gate	NOR	NOR	NAND	NAND	OR-NOR	NAND/NOR
Propagation delay in ns	12	10	30	10	2 (ECL 10K) 0.75 (ECL 100K)	70
speed Power Product (PJ)	144	130	300	100	100 (ECL 10K) 40 (ECL 100K)	0.7
Applications	Absolute	Absolute	Absolute	Laboratory instruments	Due to low propagation delay, they are used in high speed switching Applications	Due to low power consumption, they are used in portable instruments where battery supply is used.